EMI Design Guidelines for USB Components

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2. Introduction

These developers notes describe electrical and mechanical guidelines for the design of EMC compatible USB devices. A description of EMI test procedures is given, followed by a brief review of the theory behind EMI phenomena. Design guidelines for electrical, PC layout and mechanical considerations are then presented for low and full speed devices, USB cables, and hubs.

3. EMI Testing Procedures

Current FCC regulations require that class B computing devices meet specified maximum levels for both radiated and conducted EMI. Radiated EMI covers the frequency range from 30 Mhz to 1.0 Ghz. Figure 1 illustrates the test setup for radiated EMI testing. The equipment under test (EUT) is placed on a rotating table approximately 0.8 meter above a conductive floor. At the distance of 10 meters, an antenna is placed. The antenna can be raised and lowered. The conductive floor provides a uniform and EMI reflective surface.

The radiated EMI test consists of sweeping from 30 Mhz to 1.0 Ghz while the EUT is operating. If a spectral peak is within about 15 dB of the limit, it is maximized by means or rotating the EUT, and raising/lowering the antenna. Then the peak value is recorded. Typically, two different antenna types are required, one for below 250 Mhz, and one for above. If the peak falls within about 5 dB of the limit, a quasi peak mode, which averages over a time of many milliseconds, may be used. If the signal has a high peak to average ratio, then quasi peak measurements will show improvement. Quasi peak measurements are not used at other times because of the length of time required to make each measurement.

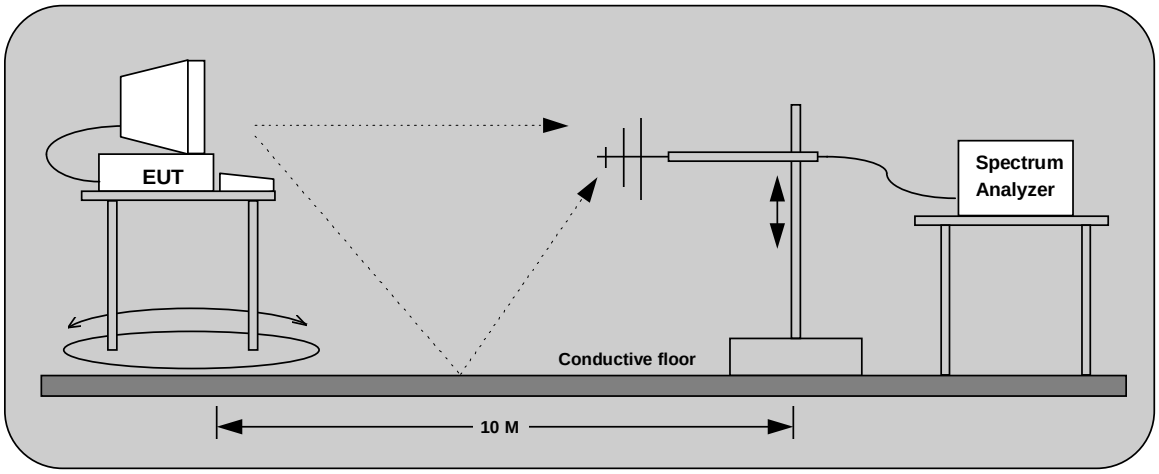

Figure 1: Radiated EMI Test Setup

Conducted EMI covers the 450 Khz to 30 Mhz range. This test is conducted in a shielded room with the EUT operating. The conducted EMI test measures the amount of EMI that is conducted via the power cable. A line isolation stabilization network (LISN) is interposed between the EUT and the spectrum analyzer.

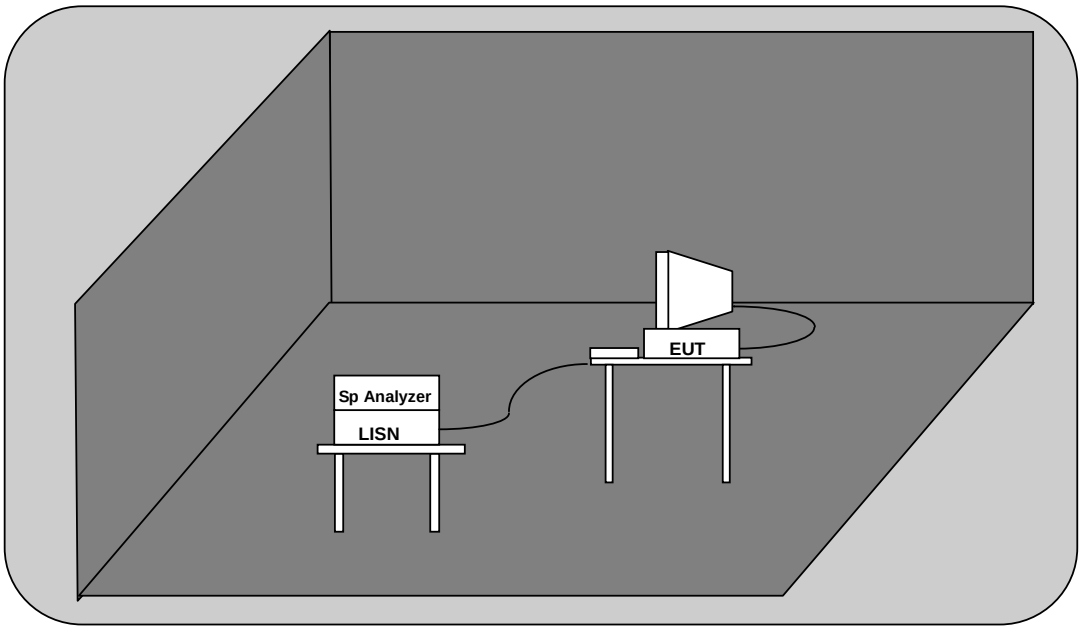

Figure 2: Conducted EMI Test Setup

The LISN is a passive network which improves the repeatability of conducted measurements by presenting a 50Ω load impedance to the noise signals of the EUT and by filtering noise from other non EUT sources. The LISN also contains switches to permit noise to be measured between each power conductor and ground.

In addition to radiated and conducted EMI tests, there is another emerging standard, already in place in Europe, that requires computing devices to be tested for ESD susceptibility. This test requires that a device must tolerate ESD events and remain operational without user intervention. The test apparatus is diagrammed in Figure 3.

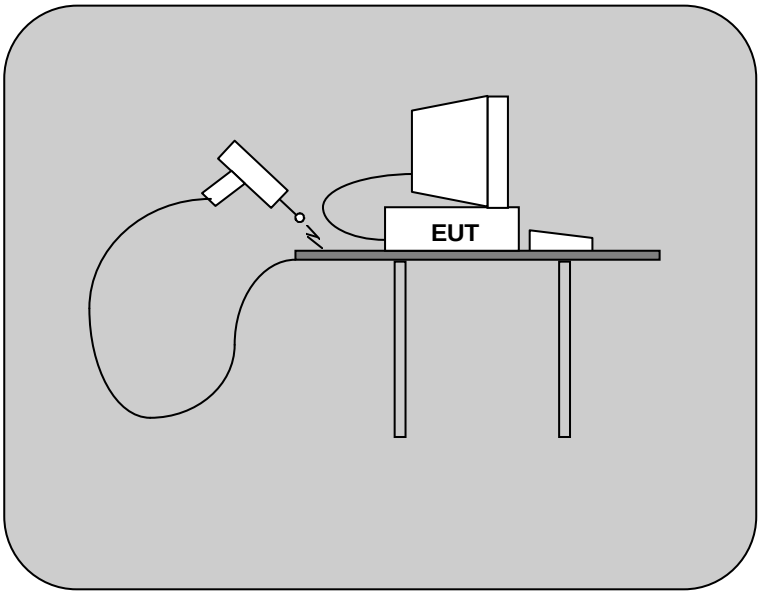

Figure 3: EMI Susceptibility Test

In this test a human body static electricity model is simulated by a high voltage gun that produces up to 8 kV that is discharged either to a conducting surface on which the EUT is operating or to conductive elements of the EUT itself (example: connectors, chassis). The EUT is permitted to experience transient errors, but it must continue to operate without user intervention.

For the types of devices utilizing USB the most difficult test to pass is usually the radiated EMI test. For this reason the analysis that follows focuses on analyzing and minimizing **radiated** EMI.

4. Factors Influencing EMI

EMI arises due to the transfer of energy from one source conducting RF currents to other radiating or conducting elements such as cables or power cords. One of the more troublesome source of EMI is the system clock which is distributed to multiple destinations and has a fast rise time. The following analysis is performed on a continuous duty cycle, symmetric trapezoidal waveform. This case represents a worst case waveform; other waveforms with lower edge density will generate correspondingly less energy and will spread that energy over a greater number of harmonics.

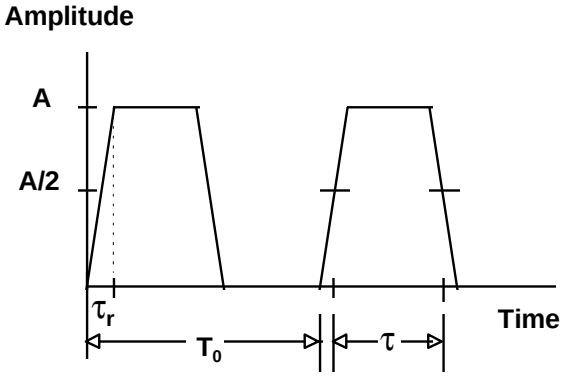

Figure 4: Periodic Trapezoidal Waveform

There are two significant parameters displayed in Figure 4, the period T_0 and the risetime τ_r. The spectral envelope of the above waveform can be obtained via Fourier analysis, and can be represented as shown in Figure 5. The waveform shown in Figure 4 yields a spectral envelope with two break points. The first

corresponds to $1/\pi\tau$ which, for a 50% duty cycle waveform, corresponds to one half the period T_0. The second breakpoint corresponds to $1/\pi\tau_r$, or the reciprocal of risetime.

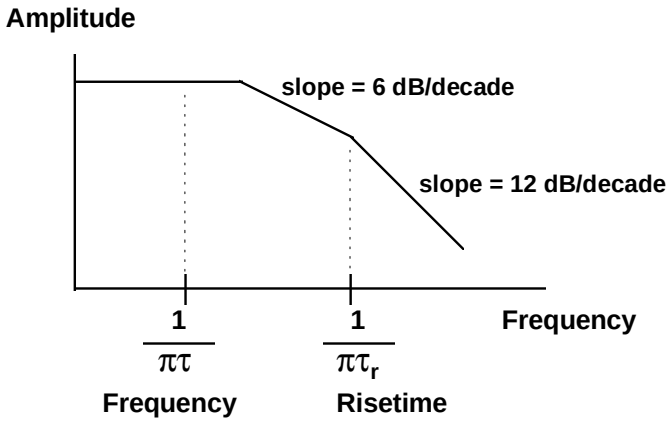

Figure 5: Spectral Envelope of Trapezoidal Waveform

At frequencies above $1/\tau_r$ the amplitude of spectral components falls off at 12 dB/decade or the reciprocal of the square of the risetime. It is desirable, therefore, to use as slow risetime signals as timing margins permit. A rule of thumb in digital design requires that the bandwidth of a digital signal include the first ten harmonics. More than 95 percent of the energy of a trapezoidal waveform is contained in the first 10 harmonics.

Consider the example of low speed USB signaling. By specifying a minimum risetime of 75 nsec the 6 dB to 12 dB break point is located at 4.2 Mhz. All harmonics above this value will be rolled off at 12 dB per decade. From a practical point of view this means that there is no appreciable energy above the 30 Mhz lower limit of FCC B radiated testing. Now consider the same signaling rate but with a 10 ns risetime. This would, of course, represent a violation of the USB specification. Such a signal has a break frequency of 32 Mhz, and this signal would have significant spectral components above 30 Mhz. Field testing of low speed USB signaling has confirmed the sensitivity of radiated EMI to risetime and led to specifying the 75 - 300 ns risetime limits.

The second factor influencing EMI is the mode of propagation for undesirable signals. Signals may propagate via either differential mode or common mode. In the differential mode signals are assumed to exist in pairs with current flowing in equal and opposite directions. Differential mode signaling does not contribute significantly to radiated or conducted EMI. This can be shown by examining the time varying component of the magnetic field surrounding a differential pair of signals. If the distance from the signal pair is large compared to the conductor separation of the pair, then the magnetic field is very small because the fields of the two conductors exactly cancel each other.

Common mode signaling arises due to stray inductances or capacitances and causes current to flow in the same direction in one or more conductors. Common mode signals are the dominant source of EMI failures in the 30 - 300 Mhz range. In the case of common mode noise there is a nonzero time varying magnetic field component which is able to couple to adjacent conductors. When this occurs the conductors generate currents which can radiate.

Another important aspect of EMI control is understanding the efficiency at which conductors radiate. To a first order, a conductor radiates at an efficiency that is a function of the quarter wavelength of the spectral component. For example, a 1.5 meter cable radiates effectively at a wavelength of 4.0 M. This corresponds to a frequency of 75 Mhz, which is well within the radiated EMI test band. A 5 meter cable radiates most effectively at a frequency of 15 Mhz, which is well below the lower frequency test limit. It is therefore possible for a long cable to pass and a short cable to fail radiated EMI testing. When testing for radiated EMI it is necessary to test with a range of cable lengths such as 0.5, 1.0, 2.0 and 5.0 meters.

4.1 EMI Control Strategies

Three strategies may be used in minimizing radiated EMI.

1. Minimize the amount of energy that is available to couple onto critical conductors by minimizing signal frequencies and using the slowest risetimes practicable.
2. Minimize the coupling between noisy signals such as clocks and critical signal lines.
3. Use filtering on those lines, such as power and ground, that cannot be kept clean.

5. USB Component EMI Design Guidelines

The following sections utilize the preceding strategies, applying EMI reduction techniques as warranted, to the design of USB hosts, devices, hubs, and cables.

5.1 USB Host EMI Design Guidelines

Designing the host to meet EMI emissions requirements requires a combination of electrical and mechanical design involving component placement, trace routing, connector placement, and circuit design.

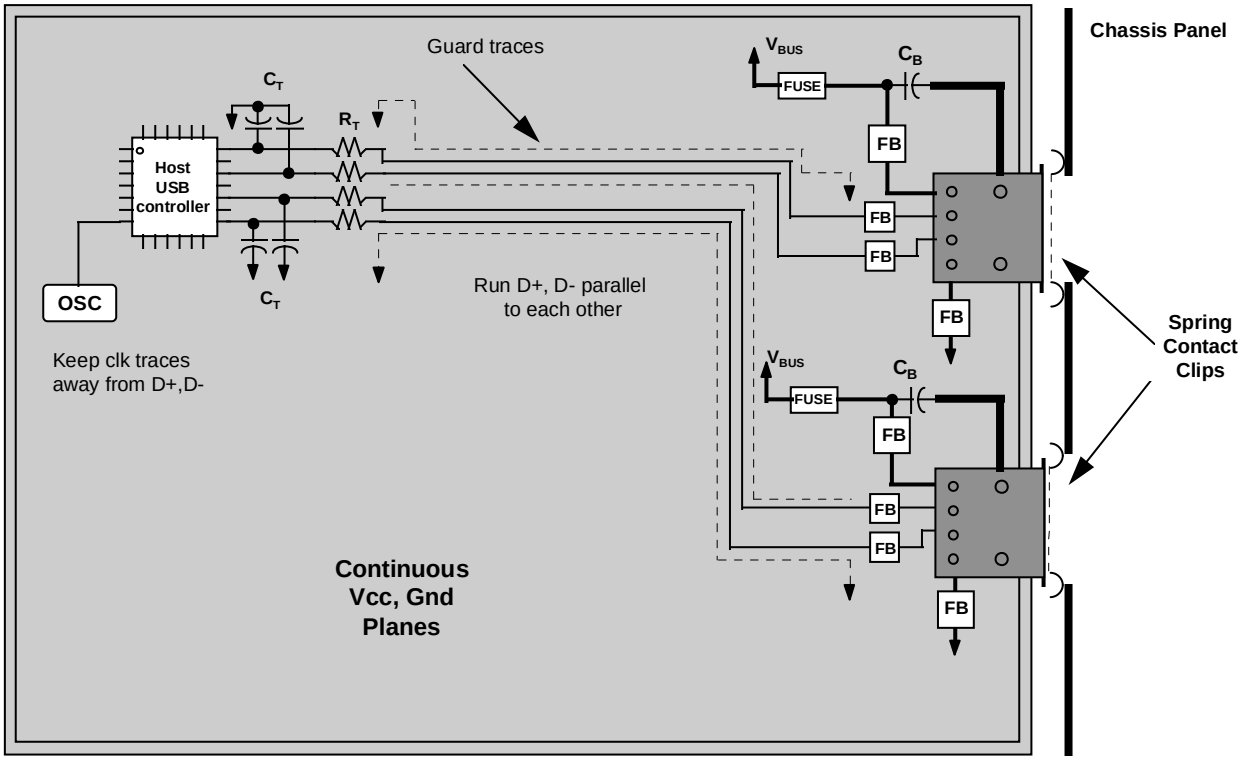

Figure 6: Host EMI Layout Considerations

Figure 6 shows a typical USB installation on a host. The inside of a PC chassis is a very noisy environment, and care must be taken to minimize the noise coupling from sources inside the PC chassis to USB signals. When routing the D+ and D- outputs of the USB controller chip, avoid running the traces near high speed clock lines or other such signals. Induced common mode noise can be minimized by running pairs of USB signals parallel to each other and running grounded guard traces on each side of the signal pair. If possible, locate the USB controller chip physically near to the USB connectors.

EMI can couple not only on the PC board but also inside IC packages. This is a particular problem in high pinout PQFP packages where the leadframe places signals in close proximity and parallel to each other without the benefit of a ground plane. USB signals should be segregated and located as far away from

high speed clocks as possible. The USB D+ and D- pins should not have any other signals (except for power and ground) located between the USB signal pins.

The V_{BUS} and ground in a PC are subject to noise both from on-board sources and also from the switching power supply. Tests have shown that it is necessary to carefully decouple both V_{BUS} and Gnd. This is done with ferrite beads. Separate ferrite beads may be used on each V_{BUS} line to each downstream USB connector. Each ferrite bead on the V_{CC} lines should be rated at 500 ma. Separate ferrites are useful, not only for EMI suppression, but also for their series DC resistance which limits the inrush current during a hot plug event. For a discussion on hot plugging and voltage droop see the *USB Voltage Drop and Droop Measurements* white paper. Ferrites should also be used on the Gnd lines to USB connectors.

If bypassing V_{CC} with ferrite beads still does not provide sufficient attenuation then small (1000 pF) capacitors can be connected on the connector side of V_{CC} to the connector shell through very short traces. If this approach is used care must be taken to insure that the capacitors do not provide a path for ground plane noise to enter via the capacitors.

5.1.1 Host Mechanical Considerations

Figure 6 shows a suggested mechanical layout of USB connectors and associated components. It is important to understand that meeting EMI compliance involves both electrical and mechanical design. The ferrite beads should be placed close to the connectors as shown. The physical placement of the D+ and D- leads with respect to other noise producing sources is also critical. Maintain a continuous ground plane in the vicinity of the USB connectors.

The R_t series termination resistors should be placed close to the USB controller chip. This practice minimizes discontinuities in the USB line impedance. The C_t capacitors provide for bypassing high frequency noise that is generated internally in the USB controller. They need to be placed between the USB controller chip and the R_t termination resistors so that they do not adversely affect the line impedance.

Of particular importance, and often a point of failure, is the electrical connection between the USB connector and the chassis. In order to prevent noise from coupling to the host connector and onto the cable's shield it is important that a good high frequency connection be made between the host connector and the chassis. This can be accomplished by a spring metal EMI gasket clip that makes multiple contacts between the USB connector and the back of the chassis panel. The spring metal clips should have sufficient mechanical compliance to compensate for the cumulative mechanical runout errors that change the distance of the USB connector from the PC chassis. Usually a 50 mil mechanical compliance is sufficient.

5.2 USB Cables and Connectors

When sending full speed signaling, USB cables rely on the shielding integrity of the cable and connector shield. Field tests with 65% braid show no measurable leakage through the shield. However, the shield must be carefully terminated to the connector. Most shielding failures can be traced to improper termination of the cable shield to the connector or connector shell to the receptacle. Full speed USB cables are specified to have a woven or spirally wound copper shield. Such a shield can be crimped to the connector shell yielding 360^0 shield coverage at the connector. The use of a foil shield with a drain wire is not recommended due to the series inductance of the drain wire and the tendency of foil to crack with cable flexing. Low speed USB cables are not required to have shielding or to maintain a specified impedance.

USB receptacles should maintain high quality shielding and a low RF impedance between the receptacle shell and the mating connector on the cable. This may be accomplished by means of multiple wiping contacts on the inside of the receptacle's shell. A minimum of four contact points is recommended. A high degree of shielding may be achieved by enclosing the sides, top, and back of the connector with a metal

shell. The shell should be provided with a low impedance connection to signal ground and, in cases where a metal chassis is present, a means of accepting a metal EMI gasket clip.

5.3 Low Speed Device Design Guidelines

Low speed devices are specified to meet radiated emissions standards without the use of shielded or impedance controlled cables. This requirement places tight restrictions on the rise and fall times of the signaling. The signal edge rate should not be achieved by relying on the cable capacitance. Doing so permits high frequency energy onto the driver end of the cable, causing the cable to radiate. The low speed output driver should generate a 75-300 ns edge that is essentially independent of the cable capacitance. The maximum specified LS device cable length is 3 meters; this limit is imposed by the requirement that the cable's propagation delay must look small compared to the signaling rise time.

Another potential source of emissions for LS devices is the high frequency energy, generated by other components on the LS device, that can couple from the device's PC traces and components to the cable. Particular care should be taken that the device's clock does not couple to the USB cable. It is important to minimize the amount of high frequency energy that the clock circuit generates. This can be done by limiting the highest frequency to 4x the data rate or 6 Mhz. This frequency permits 4x oversampling for a straightforward DPLL implementation.

It is also important to limit the edge rates on all signals that go off chip. Due to the larger capacitance and larger loop area that these signals (as opposed to intra-chip signals) experience, their dI/dt contributes more to emissions. For example, a low current output buffer driving an external crystal or resonator through 1.0KΩ produces less noise than a similar frequency oscillator, which is usually designed to drive high capacitance loads with fast edge rates. For this reason, a crystal or ceramic resonator is preferable to an oscillator.

The efficiency with which a current loop couples to the cable increases with loop area and with its proximity to the D+ and D- lines. Therefore, D+/D- and other signal path loop areas should be minimized, particularly clock lines. Coupling can also be minimized by maintaining a high quality ground plane. Noise will then couple back into the ground plane rather than to the cables.

Power supply noise reduction techniques need to be addressed also. Standard low noise practices such as good V_{BUS} and ground bypassing should be observed; this means using both bulk capacitance and multiple low ESL capacitors. Note that the USB spec places an upper limit on the amount of bulk capacitance of 10 µf. Power supply noise conduction into the USB cable power conductors can be reduced by the use of ferrite beads on both the V_{BUS} and Gnd leads. Due to the large difference between the low speed signal bandwidth (< 4x the bit rate) and the lower limit of class B emissions range (30 Mhz), ferrite beads may also be used on the D+ and D- lines, if necessary. However, the frequency response through the ferrite beads on D+ or D-must not roll off by more than 2.0 dB at 6.0 Mhz..

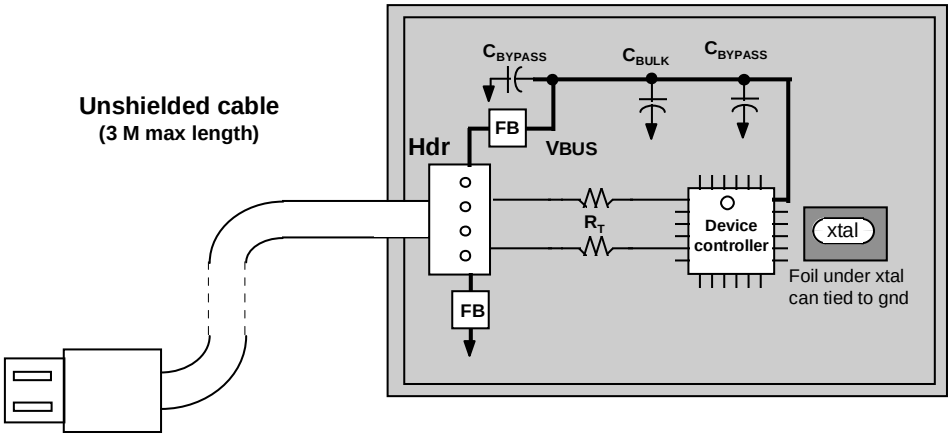

Figure 7: Low Speed Device

Figure 7 illustrates the design recommendations for low speed devices. Low speed devices are limited to a cable length of 3.0 meters, and cannot support a series B connector into which any length USB cable could connect. This example assumes that the device has a cable that is attached via a header. High frequency coupling to the cable is minimized by proper PC layout; the highest frequency device (in this example, the crystal) are located opposite the header. If a 2-layer PC board is used, one layer should be dedicated to a ground plane. Do not split the ground plane, and minimize discontinuities in the plane by limiting the number of traces and vias on the ground plane side of the board. Low speed design guidelines are summarized below:

1. Use as low a frequency crystal as possible, avoid oscillators
2. Off-chip signals should have as slow edge rates as is practicable
3. Keep D+ and D- physically far away from high speed signals
4. Minimize loop areas of signal and clock carrying conductors.
5. Bypass V_{BUS} and Gnd with ferrite beads (if necessary)
6. Maintain ground plane integrity.
7. Use good Vcc/Gnd bypass practices

While not required for impedance matching, the R_T resistors are suggested for protection in the event that both a hub and the LS device attempt to drive the bus simultaneously. The value of R_T must be low enough that it does not cause the rise/fall times to fall out of specification.

5.3.1 Shielded Cables on Low Speed Devices

The USB specification does not preclude the use of shielded cables on low speed devices. A manufacturer may decide that the cost differential for shielded cabling is lower than the additional costs incurred in getting a low speed device to pass EMI testing without shielding. Shielding the cable of low speed devices may also be necessary for meeting ESD and EMI susceptibility requirements. In such a case the EMI guidelines for the LS device are the same as for full speed devices which are described in the following section.

5.4 Full Speed Device Design Recommendations

As defined in the USB spec, full speed devices must be able to send and receive 12 Mbit/sec signaling and must use shielded cabling with a controlled impedance for the signal lines. Field tests have demonstrated that a properly designed cable shield offers a high degree of EMI suppression on conductors inside the shield, i.e. at least 25 2B of attenuation over the class B range for radiated EMI. The principal challenge of full speed device EMI compliance is preventing high frequency energy from coupling to the *shield***.** Many of the design practices utilized for low speed devices are applicable for full speed devices. These include minimizing the amount of high frequency energy on the PC board itself and minimizing the ability of that energy to couple to the shield.

Figure 8 shows a crystal, rather than an oscillator, providing the clock. As explained earlier, a crystal and its driver circuitry typically generates less high frequency noise than an oscillator. The crystal can should be connected to the ground plane, and the area directly under the crystal can should consist of a conductive plane tied to ground. One drawback of crystals is that they are usually limited to frequencies below 25 Mhz. Generating an internal 48 Mhz clock using a crystal may require an on-chip frequency multiplier.

If clock multiplication is not feasible, then a 48 Mhz oscillator may be used. Tests showed that the oscillator was the single largest contributor to EMI coupling to the shield. If an oscillator is used it may be necessary to provide some type of shielding around the oscillator can. One test showed that an oscillator connected only to V_{cc} and Gnd (its output was not connected at all) still generated spectral components near the class B limit in the 40 - 80 Mhz range.

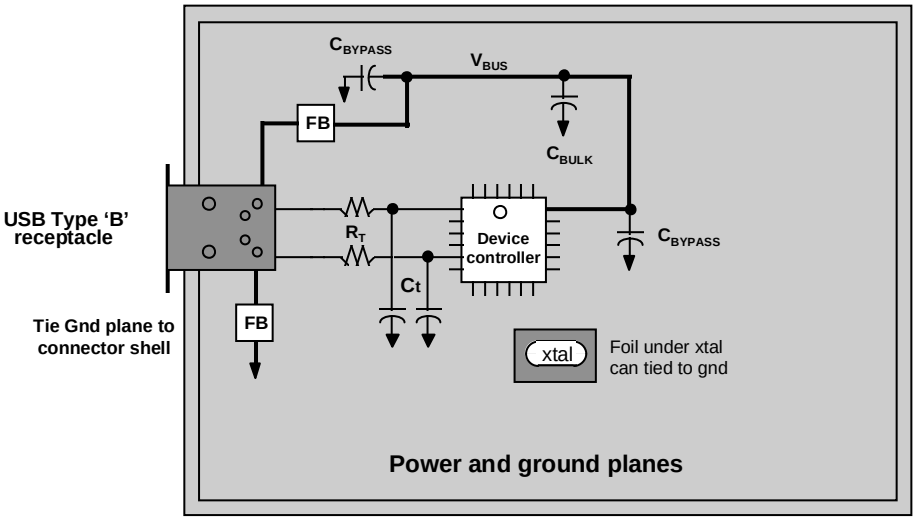

Figure 8: Full Speed Device PC Layout

Full speed devices use a shielded cable which requires that the connector shell be tied to the ground plane. It is important to note that a ground plane does not behave like an equipotential surface at high frequencies. The location of the connector shell's termination to the Gnd plane is critical. The connection needs to be made to the quietest area of the ground plane to prevent noise from the ground plane from coupling to the shield. As shown in Figure 8, the quietest location on the ground plane is on the opposite edge of the board, far away from the crystal and other high frequency signals.

Noise from V_{BUS} and Gnd may be minimized by use of ferrite beads. The beads should be placed between the connector and the on-board circuitry. The C_t capacitors may be used to bypass high frequency energy to ground and for edge rate control, and they should be less than 50 pF each and are placed between the driver chip and the R_t series termination resistors. Both the C_t and R_t resistors should be placed as close to the driver chip as is practicable. Noisy devices should be placed as far from the connector as practicable, and loop areas for noisy signal paths should be minimized. If we assume that a 4 layer board is used, then signal traces may be sandwiched between the power and ground planes. This geometry does cause a decrease in the signal trace impedance, but for short traces this is not a problem.

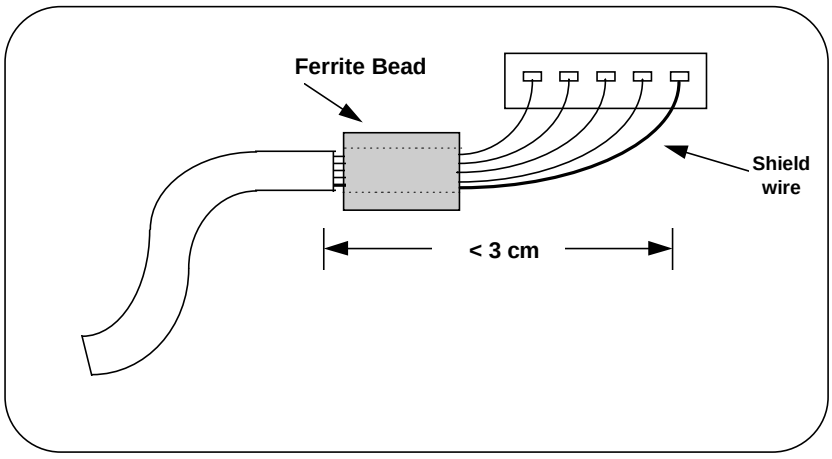

Figure 9: USB Cable Connection to a Header

Full speed devices may use either a type B receptacle or may have a permanently attached cable. In the latter case the cable will most likely be attached to the PC board via a header. Such an arrangement does not yield as good shielding as a USB connector pair and may require additional filtering. This is most

easily accomplished by passing all four conductors, plus the shield wire, through a ferrite bead as shown in the following figure. The length of unshielded cable should be limited to 3 cm or less. If a single ferrite bead is used it is not usually necessary to also have the separate beads as shown in Figure 8. Note: additional filtering may be achieved by winding the 4 wires through the ferrite bead an additional turn. As with the use of ferrite beads in signal paths, care should be taken to insure that the signaling meets rise and fall times, especially the EOP signaling. EOP signaling is single ended and may be strongly affected by a single bead, which acts as a common mode only filter.

5.5 Hub Design Guidelines

Hubs must propagate both full and low speed signaling, and this places particularly stringent requirements on hub downstream ports. From an EMI point of view, a hub can be considered a full speed device which must meet emissions requirements while signaling at 1.5 Mbit/sec over unshielded cabling. Section 5.4 demonstrates that it is possible to meet class B emissions requirements for a host hub type of adapter. Stand alone hubs should be easier to design for EMI compatibility than host hubs due to the fact that their noise sources are more easily characterized than host hubs inside a PC chassis.

5.5.1 Locally Powered Hub

Locally powered hubs obtain their downstream power from a source other than the upstream USB connection. That power source must be bypassed to prevent EMI from coupling upstream. Figure 10 shows the connections and filtering required for a stand alone locally powered hub. A locally powered hub has the option of obtaining all of its power locally or it may draw up to 100 ma from upstream. The hub shown in Figure 10 obtains all of its power locally and therefore does not need a connection from the upstream V_{BUS} to the hub controller's V_{CC}.

Hub downstream ports need to meet EMI standards for both shielded and unshielded cabling. The need to support the latter requires that the signal lines be especially quiet. To meet this requirement it will probably be necessary to bypass the data lines with ferrite beads. If ferrites are used on the data lines be sure to check that the signal edge rates still remain within the 4 ns - 20 ns limits stipulated in the USB spec.

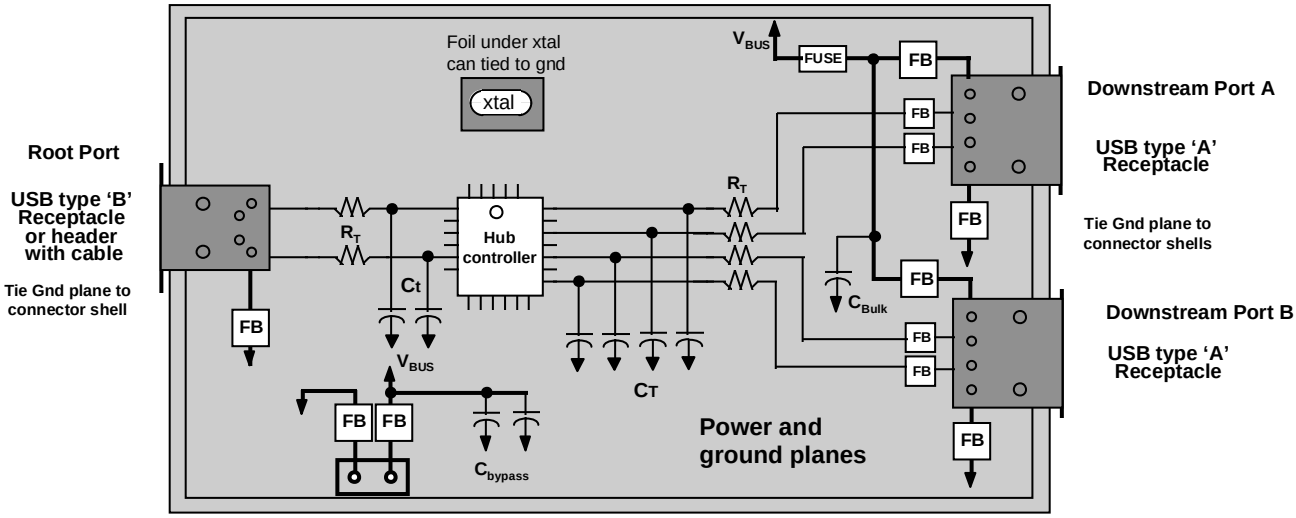

Figure 10: Locally Powered Hub Layout

5.5.2 Bus Powered Hub

Bus powered hubs obtain their power exclusively from the upstream USB port to which they are connected. The PC layout is similar to that of a self powered hub with the exception that a bus powered hub does not have a separate power entry connection, and all downstream ports must have power switching on V_{BUS}. The power switching may be per port or ganged.

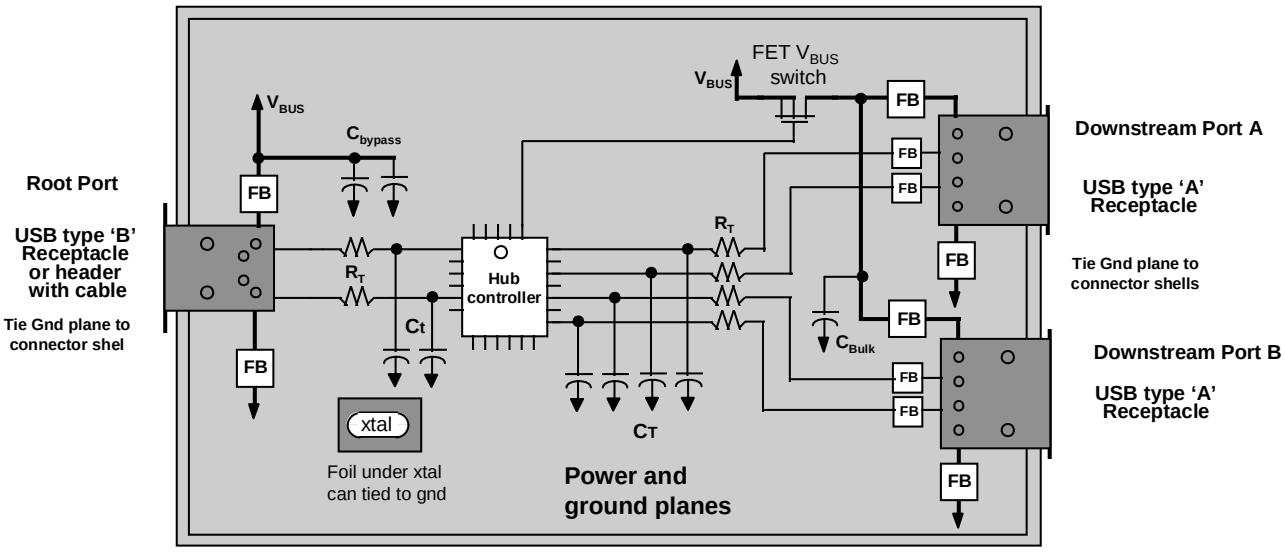

Figure 11: Bus Powered Hub

5.5.3 USB Receptacle Attachment Details

Figure 12 shows the connection details between a USB receptacle and the PC board. V_{BUS} and Gnd from the receptacle are bypassed with ferrite beads and then connected to their respective power and ground planes. D+ and D- connect to series termination resistors and high frequency bypass capacitors to ground. The receptacle attachment is similar for both upstream and downstream connectors. However, hub downstream receptacles are more EMI sensitive since they must operate with LS devices attached which may use unshielded cabling. As a result, hub downstream receptacles will probably require ferrite beads on their D+ and D- lines.

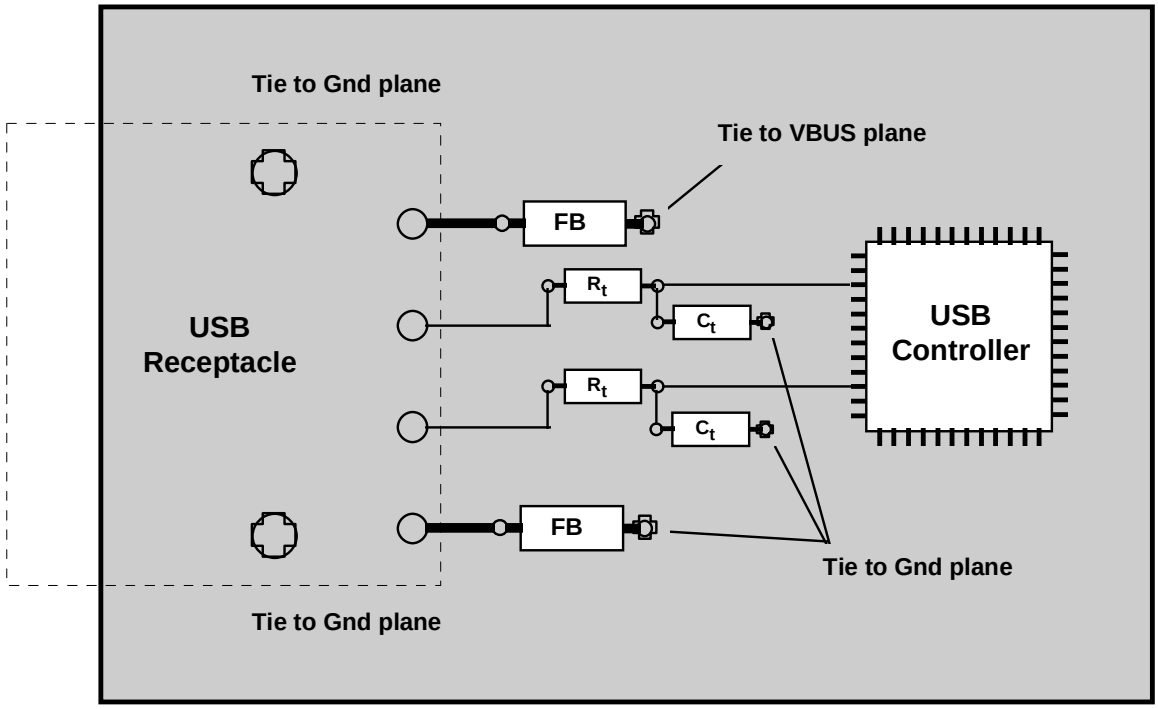

Figure 12: USB Connector to PCB Details

6. Conclusions

The guidelines described in this paper were obtained from empirical field test data. Subsequent test results of peripherals and hosts indicate that EMI standards can be met by application of the guidelines described in this paper. Careful application of established EMC control practices and an understanding of the generation mechanisms for EMI make it feasible to design USB hardware that meets class B standards.

7. Appendix 1: USB Device EMI Checklists

7.1 Checklist for USB Hosts

7.1.1 Edge Rates

EMI 1	Does the host have per-port edge rate control?	yes___	no___
EMI 2	Do ports that are enumerate as low speed shut off full speed downstream signaling?	yes___	no___
EMI 3	Are full speed signaling edge rates between 4.0 and 20.0 ns?	yes___	no___
EMI 4	Are low speed signaling edge rates between 75 and 300 ns?	yes___	no___
EMI 5	Does a hub's upstream port signal at full speed edge rates (4.0 - 20.0 ns) for all traffic?	yes___	no___
EMI 6	Do the D+ and D- lines have 47 pf termination capacitors	yes___	no___

7.1.2 Electrical

EMI 7	Are the V_{BUS} and Gnd lines bypassed with ferrite beads?	yes___	no___	
EMI 8	Are the D+ and D- lines bypassed with ferrite beads?	yes___	no___	
EMI 9	Are the ferrite beads placed as close as possible to the USB connector?	yes___	no___	
EMI 10	Do D+ and D- have series termination resistors such that $Z_{DRIVER} + Z_{TERM} = 45\Omega$?	yes___	no___	
EMI 11	Are the series resistors located as close to the driver chip as is possible?	yes___	no___	
EMI 12	Is the D+ and D- PC trace impedance 90Ω +/- 15%	yes___	no___	
EMI 13	Are the D+ and D- traces routed so that they are not running near to any traces carrying high speed signals, such as clocks?	yes___	no___	
EMI 14	Are the D+ and D- traces routed parallel to each other	yes___	no___	
EMI 15	Do the D+ and D- traces have grounded guard traces around them	yes___	no___	
EMI 16	Are the USB output driver V_{CC} pins bypassed with dedicated capacitor(s)	yes___	no___	
EMI 17	Are there termination capacitors on D+ and D- to Gnd? These are optional but are effective in limiting emissions.	yes___	no___	
EMI 18	Are the termination capacitors located between the USB driver chip and the series termination resistors?	yes___	no___	na___
EMI 19	Does USB V_{BUS} have a .01µf bypass capacitor to Gnd?	yes___	no___	
EMI 20	Is this capacitor connected to Gnd as close to the chassis as possible	yes___	no___	

7.1.3 USB Driver Chip Layout

EMI 21	Are D+ and D- placed such that there are no adjacent pins carrying high speed signals?	yes___	no___	
EMI 22	Does the V_{CC} supplying the USB output drivers have one or more dedicated power pins?	yes___	no___	
EMI 23	Does the Gnd supplying the USB output drivers have one or more dedicated power pins?	yes___	no___	
EMI 24	Do the USB drivers have the necessary number of V_{CC} and Gnd pins to handle ~40 ma for each pair of D+ and D- pins?	yes___	no___	
EMI 25	Does the USB driver chip use as low frequency a clock as is feasible?	yes___	no___	na___

7.1.4 USB Receptacles

EMI 26	Are the USB receptacles located away from other high speed circuitry or traces?	yes___	no___
EMI 27	Does the USB receptacle shell make multiple low impedance connections to the motherboard ground plane?	yes___	no___

EMI 28	Does the receptacle shell make multiple low impedance connections to the chassis?	yes___	no___
EMI 29	Do the USB receptacles provide 360^0 shielding of the D+ and D- signals	yes___	no___
EMI 30	Does the USB receptacle provide multiple low impedance connections between the receptacle shell and the mating connector body?	yes___	no___

7.2 Checklists for USB Cables

7.2.1 Checklist for Detachable USB Cables

EMI 31	Is the cable shielded?	yes___	no___
EMI 32	Is the shield either copper braid or spiral copper wrap?	yes___	no___
EMI 33	Does the shield provide at least 65% shield coverage?	yes___	no___
EMI 34	Does the cable have a twisted data pair impedance controlled to 90Ω +/- 15%?	yes___	no___
EMI 35	Does the cable have a type A connector on one end and a type B connector on the other?	yes___	no___
EMI 36	Is the cable length less than 5.0 meters?	yes___	no___
EMI 37	Is the gauge of the power pair between 20 and 28 Ga? This requirement is to guarantee that the USB connector can be reliable crimped to the cable.	yes___	no___
EMI 38	Is the IR drop through V_{BUS} and Gnd of the cable and connectors less than 250 mV @ 500 ma	yes___	no___
EMI 39	Are the connectors attached in such a manner that a 360^0 crimp can be achieved with the shield?	yes___	no___
EMI 40	Does the connector shell provide multiple low impedance sites for making connections with the shell of the receptacle?	yes___	no___
EMI 41	Does the connector shell provide 360^0 shielding between where the shield terminates and the edge of the connector shell?	yes___	no___

7.2.2 Checklist for non-Detachable Cables to Full Speed Devices or Self Powered Hubs

EMI 42	Is the cable shielded?	yes___	no___
EMI 43	Is the shield either copper braid or spiral copper wrap?	yes___	no___
EMI 44	Does the shield provide at least 65% shield coverage?	yes___	no___
EMI 45	Does the cable have a twisted data pair impedance controlled to 90Ω +/- 20%?	yes___	no___
EMI 46	Does the cable have a type A connector on one end ?	yes___	no___
EMI 47	Does the shield terminate to the ground plane on the device end?	yes___	no___
EMI 48	Is the cable length less than 5.0 meters?	yes___	no___
EMI 49	Is the gauge of the power pair between 20 and 28 Ga? This requirement exists because the standard USB connector will not crimp reliably onto other size conductors,	yes___	no___
EMI 50	Are the connectors attached in such a manner that a 360^0 crimp can be achieved with the shield?	yes___	no___
EMI 51	Does the connector shell provide multiple low impedance sites for making connections with the shell of the receptacle?	yes___	no___
EMI 52	Does the connector shell provide 360^0 shielding between where the shield terminates and the edge of the connector shell?	yes___	no___

7.3 Checklist for Low speed USB peripherals

7.3.1 Cabling and Connectors

EMI 53	Is the cable permanently attached to the device?	yes___	no___
EMI 54	Does the cable have a type A connector on one end?	yes___	no___
EMI 55	Is the cable length less than 3.0 meters?	yes___	no___
EMI 56	Is the gauge of the power pair between 20 and 28 Ga? This requirement exists because the standard USB connector will not crimp reliably onto other size conductors,	yes___	no___

7.3.2 Electrical

EMI 57	Does the low speed device signal with edge rates between 75 and 300 ns?	yes___	no___
EMI 58	Is the capacitance to gnd (including the cable) on D+ and D- less than 350pf?	yes___	no___
EMI 59	Does the device signal with a bit rate of 1.5 Mb/sec +/- 1.5%	yes___	no___
EMI 60	Is the on-board clock source equal to or less than 6 Mhz?	yes___	no___
EMI 61	Is the on-board clock source a crystal or a ceramic resonator?	yes___	no___
EMI 62	Is the crystal or resonator driven with as low energy an excitation that is consistent with reliable operation?	yes___	no___
EMI 63	Is the crystal can tied to ground	yes___	no___
EMI 64	Does the PCB area under the crystal can have a continuous conducting plane tied to ground?	yes___	no___
EMI 65	Are there ferrite beads on V_{CC} and Gnd where they enter the PC board?	yes___	no___
EMI 66	Are there ferrite beads on D+ and D-	yes___	no___
EMI 67	Are on-board devices bypassed with respect to V_{CC} and Gnd?	yes___	no___

7.3.3 Mechanical and PC Layout

EMI 68	Are the ferrite beads placed as close as possible to the USB connector?	yes___	no___
EMI 69	Is the clock source located as far from the USB connector as is possible?	yes___	no___
EMI 70	Are the USB D+ and D- traces located away from traces carrying high frequency signals?	yes___	no___
EMI 71	Does the PC board have a ground plane?	yes___	no___

7.4 Checklist for Non-hub Full Speed Peripherals

7.4.1 Cabling and Connectors

EMI 72	If the cable is permanently attached does it meet the cable requirements shown in Section 7.2.2?	yes___	no___
EMI 73	If the cable is detachable does the device have a USB type B receptacle	yes___	no___

7.4.2 Electrical

EMI 74	Are the V_{BUS} and Gnd lines bypassed with ferrite beads?	yes___	no___	
EMI 75	Do D+ and D- have series termination resistors such that $Z_{DRIVER} + Z_{TERM} = 45\Omega$?	yes___	no___	
EMI 76	Is the D+ and D- PC trace impedance 90Ω +/- 15%	yes___	no___	
EMI 77	Are the USB output driver V_{CC} pins bypassed with dedicated bypass capacitor(s)	yes___	no___	
EMI 78	Are there termination capacitors on D+ and D-? These are optional but useful in limiting emissions.	yes___	no___	
EMI 79	Does the USB controller use a crystal rather than an oscillator	yes___	no___	
EMI 80	Is the crystal can tied to ground	yes___	no___	na___
EMI 81	Is the area under the crystal can a conductive plane that connects to the ground plane?	yes___	no___	na___

7.4.3 Peripheral IC

EMI 82	Are all high speed lines separated by several pins from the D+ and D- USB pins	yes___	no___
EMI 83	Does the V_{CC} supplying the USB output drivers have one or more dedicated power pins?	yes___	no___
EMI 84	Does the Gnd supplying the USB output drivers have one or more dedicated power pins?	yes___	no___
EMI 85	Do the USB drivers have the necessary number of V_{CC} and Gnd pins for ~40 ma per pair of signal pins?	yes___	no___
EMI 86	Does a hub's upstream port signal at full speed edge rates (4.0 - 20.0 ns) for all traffic?	yes___	no___
EMI 87	Does the USB controller use as low frequency a clock as is feasible?	yes___	no___
EMI 88	Is the crystal driven with as low an excitation energy that is consistent with reliable operation?	yes___	no___

7.4.4 PC Layout

EMI 89	Does the PCB have a ground plane	yes___	no___
EMI 90	Is the ground plane unbroken and continuous	yes___	no___
EMI 91	Is the USB connector or cable attachment located away from other high speed circuitry or traces?	yes___	no___
EMI 92	Are the ferrite beads placed as close as possible to the USB connector?	yes___	no___
EMI 93	Are the series resistors located as close to the driver chip as is possible?	yes___	no___
EMI 94	Are The D+ and D- traces run so that they are not routed near to any traces carrying high speed signals, such as clocks?	yes___	no___
EMI 95	Are the D+ and D- traces routed parallel to each other	yes___	no___
EMI 96	Are the termination capacitors located between the USB driver chip and the series termination resistors ?	yes___	no___
EMI 97	Do the D+ and D- traces have grounded guard traces around them	yes___	no___
EMI 98	Does the receptacle or header make a low impedance connection to the ground plane?	yes___	no___

7.5 Checklist for Hubs

7.5.1 Edge Rates

EMI 99	Can downstream ports be configured as low or full speed on a per port basis?	yes___	no___
EMI 100	Do ports that are enumerate as low speed shut off full speed downstream signaling?	yes___	no___
EMI 101	Are full speed signaling edge rates between 4.0 and 20.0 ns on downstream ports?	yes___	no___
EMI 102	Are low speed signaling edge rates between 75 and 300 ns on downstream ports?	yes___	no___
EMI 103	Does a hub's upstream port signal at full speed edge rates (4.0 - 20.0 ns) for all traffic?	yes___	no___

7.5.2 Cabling and Connectors

EMI 104	If the cable is detachable, does upstream port have type B USB receptacle?	yes___	no___	
EMI 105	If the cable is permanently attached does it meet the cable requirements described in Section 7.2.2?	yes___	no___	
EMI 106	Do all downstream ports have type A receptacles?	yes___	no___	
EMI 107	Does the USB receptacle shell make multiple low impedance connections to the motherboard ground plane?	yes___	no___	
EMI 108	Does the receptacle shell make multiple low impedance connections to the chassis?	yes___	no___	na___
EMI 109	Do the USB receptacles provide 360^0 shielding of the D+ and D- signals	yes___	no___	
EMI 110	Do the USB receptacles provide multiple low impedance connections between the connector shell and the mating connector body?	yes___	no___	

7.5.3 Electrical

EMI 111	Are the D+ and D- lines bypassed with ferrite beads?	yes___	no___	
EMI 112	Are the V_{BUS} and Gnd lines bypassed with ferrite beads?	yes___	no___	
EMI 113	Do D+ and D- have series termination resistors such that $Z_{DRIVER} + Z_{TERM} = 45\Omega$?	yes___	no___	
EMI 114	Are the D+ and D- PC trace impedances 90Ω +/- 15%	yes___	no___	
EMI 115	Are the D+ and D- traces routed parallel to each other	yes___	no___	
EMI 116	Do the D+ and D- traces have grounded guard traces around them	yes___	no___	
EMI 117	Are the USB output driver V_{CC} pins bypassed with dedicated capacitor(s)	yes___	no___	
EMI 118	Are there termination capacitors to Gnd on D+ and D-? These are optional but are effective at limiting emissions.	yes___	no___	
EMI 119	Are the termination capacitors located between the USB driver chip and the series termination resistors?	yes___	no___	na___
EMI 120	Does the USB controller use a crystal rather than an oscillator	yes___	no___	
EMI 121	Is the crystal driven with as low energy an excitation that is consistent with reliable operation?	yes___	no___	na___
EMI 122	Is the crystal can tied to ground	yes___	no___	na___
EMI 123	Is the PCB area under the crystal can a continuous conductive plane that is tied to ground?	yes___	no___	na___

7.5.4 Hub IC

EMI 124	Are any high speed lines separated by several pins from the D+ and D- USB leads?	yes___	no___
EMI 125	Does the V_{CC} supplying the USB output drivers have one or more dedicated power pins?	yes___	no___
EMI 126	Does the Gnd supplying the USB output drivers have one or more dedicated power pins?	yes___	no___
EMI 127	Do the USB drivers have the necessary number of V_{CC} and Gnd pins for ~40 ma per pair of signal pins?	yes___	no___
EMI 128	Does a hub's upstream port signal at full speed (4.0 - 20.0 ns) for all traffic?	yes___	no___
EMI 129	Does the USB controller use as low frequency a clock as is feasible?	yes___	no___

7.5.5 PC Layout

EMI 130	Does the PCB have a ground plane	yes___	no___
EMI 131	Is the ground plane unbroken and continuous	yes___	no___
EMI 132	Are the series termination resistors located as close to the driver chip as is possible?	yes___	no___
EMI 133	Are The D+ and D- traces run so that they are not located near to any traces carrying high speed signals, such as clocks?	yes___	no___
EMI 134	Are the USB connectors or cable attachment located away from other high speed circuitry or traces?	yes___	no___
EMI 135	Are the ferrite beads on D+, D-, V_{BUS} and Gnd located as close to the USB connector as possible?	yes___	no___
EMI 136	Does the receptacle or header make a low impedance connection to the ground plane?	yes___	no___