VIT-AP UNIVERSITY	Final Assessment Test – Winter (2024-25) - April 2025	
	Maximum Marks: 100	Duration: 3 Hours
Course Code: ECE 2002	Course Title: Computer Organization and Architecture	
Set No: 04	Exam Type : Closed Book	School: SENSE
Date: 29/04/2025	Slot: A1	Session: FN

Keeping mobile phone/smart watch, even in 'off' position is treated as exam malpractice

General Instructions if any:

1. **"fx series" - non Programmable calculator are permitted : YES**
2. **Reference tables permitted : NO**

PART – A: Answer any TEN Questions, Each Question Carries 10 Marks (10×10=100 Marks)

1. a) Analyze the role of the Program Counter (PC) and Instruction Register (IR) in instruction execution?
   b) Describe the basic instruction cycle (Fetch–Decode–Execute) and explain what happens at each stage. (5+5 M)

2. The IAS computer uses a 40-bit word format, with each instruction being 20 bits long. A word can store either one 40-bit data value or two 20-bit instructions. Assume the instruction format is as follows: (5+5 M)
   | 8 bits (Opcode) | 12 bits (Address) |
   A word in memory contains the following binary value:
   00100100 000000000011 | 00010010 000000000101
   a) Decode the two instructions stored at memory address 200.
   b) Execute the instructions step-by-step and show the final value in the Accumulator (AC)

3. How modern processors detect overflow using flags like the Carry Flag (CF) and Overflow Flag (OF) in systems like x86. **(10 M)**

4. Convert the signed decimal number - 45 into its 32-bit signed magnitude representation. Repeat the process for the number +58. Then, perform binary addition of these two numbers using their signed magnitude format, showing all necessary steps and handling of the sign bit. **(10 M)**

5. Write an 8086 Assembly language Program to Find Reverse of an integer Array. consider the elements of the array as 23, 45, 67, 12, 87. **(10 M)**

6. Explain the following instructions with examples and name the category to which it belongs to in the 8086 microprocessor: **(10 M)**
   i) MOVSB
   ii) SUB
   iii) OR
   iv) IN AL, 80H
   v) NEG

7. List and explain the functions of the major components involved in the instruction fetch sequence. Include the roles of PC, MAR, MBR, IR, and control signals. Describe how these registers interact during the fetch phase using symbolic representation of micro-operations. **(10 M)**

8. Write the micro-operation sequence for the instruction MOV R1, [R2]. Assume three clock cycles are required for execution. Explain how control signals are generated to support each micro-operation during the execute cycle. **(10 M)**

9. A system has the Cache size = 2 KB, Block size = 64 bytes, Address size = 32 bits, and Address = 0x00FF1234. Find the tag, set index, and block offset for address: 0xABCDEF01 using Direct mapping Techniques. **(10 M)**

10. A computer system uses a two-level memory hierarchy: cache and main memory. The cache access time is 5 ns, and the main memory access time is 100 ns. The cache hit rate is 90%.**(10 M)**
(a) Calculate the effective memory access time (EAT).
(b) If the hit rate drops to 80%, by what percentage does the EAT increase?

11. Find the number of clock cycles required to execute 15 instructions with pipeline method and without pipeline method for the following instruction structure? Improve the pipeline structure. **(10 M)**
Fetch - 1 Clock cycle
Decoding - 2 Clock cycle
Execution- 4 Clock cycle

12. What hazards are associated with the pipelining of instructions? Provide examples to illustrate the types of hazards **(10 M)**

QP MAPPING

Q. No.	E/A/T	Module Number	Marks	BL	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped
Q1	E	1	10	1	CO1	1,2,3,4,5	1	1
Q2	A	1	10	1	CO1	1,2,3,5	1	1
Q3	E	2	10	3	CO2	1,2,3,5	1,2	1
Q4	T	2	10	3	CO2	1,2,3,4,5	1,2	1
Q5	A	3	10	2	CO3	1,2,3,4,5	1,2	1
Q6	T	3	10	2	CO3	1,2,3,4,5	1,2	1
Q7	E	4	10	3	CO4	1,2,3,4,5	1,2	1
Q8	A	4	10	2	CO4	1,2,3,4,5	1,2	1
Q9	T	5	10	3	CO5	1,2,3,4,5	1,2	1
Q10	E	5	10	4	CO5	1,2,3,4,5	1,2	1
Q11	A	6	10	4	CO6	1,2,3,4,5	1,2	1
Q12	E	6	10	4	CO6	1,2,3,4,5	1,2	1