VIT-AP UNIVERSITY	Final Assessment Test – Winter (2024-25) Freshers - May 2025	
	Maximum Marks: 100	Duration: 3 Hours
ourse Code: ECE1003	Course Title: Digital Logic Design	
et No: 2	Exam Type : **Closed Book**	School: SENSE
ate: 19/05/2025	Slot: A1	Session: FN

Keeping mobile phone/smart watch, even in 'off' position is treated as exam malpractice

General Instructions if any:

1. **"*fx* series" - non Programmable calculator are permitted : NO**
2. **Reference tables permitted : NO**

PART – A: Answer any TEN Questions, Each Question Carries 10 Marks (10×10=100 Marks)

1. (a) Convert the binary number $(110101001011.101)_2$ to hexadecimal number **(10 M)**
   (b) Convert the decimal number $(1246.225)_{10}$ into octal number **(10 M)**

2. (a). Perform BCD addition $(59)_{10} + (47)_{10}$
   (b). Convert the following
   (i). Binary number $(11001110)_2$ to Gray code number
   (ii). Gray code number (01011101) to Binary number

3. Obtain the minimal product of sum (POS) form expression for the Function using K-MAP **(10 M)**
   $F = \prod M(0,1,2,4,5,9,13,14,15) + d(8,10,11,12)$.

4. Design a 4 X 2 priority encoder, with the inputs in the following order: $D_2 > D_1 > D_3 > D_0$. **(10 M)**

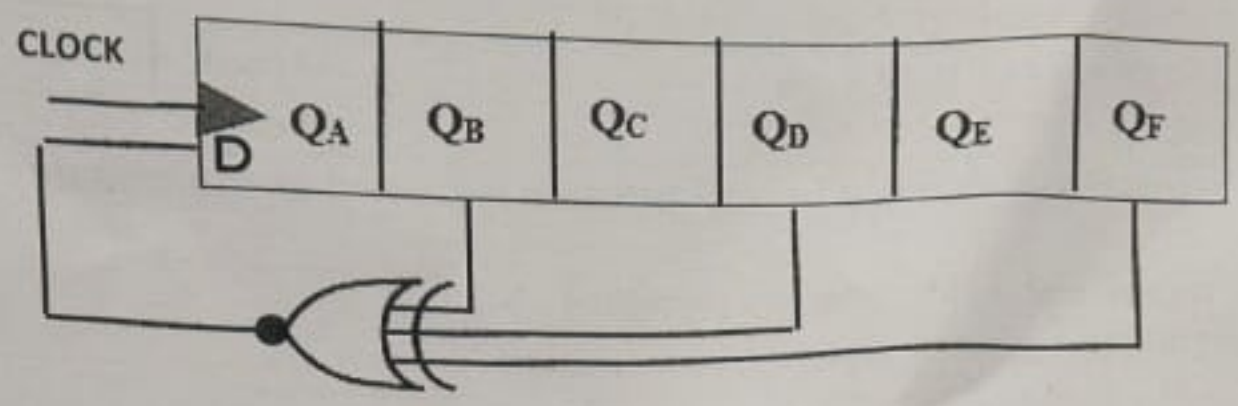
5. Design 5 X 32 decoder using 2 X 4 and 1 X 2 decoders. Note that 2 X 4 decoders should be more than 1 X 2 decoders. **(10 M)**

6. Implement the Boolean function using 8 X 1 Multiplexer $f(A,B,C,D) = \bar{A}BC\bar{D} + AD + \bar{A}BD + \bar{B}\bar{C}$. Note that B, C, D are to be treated as selection line inputs and A is to be treated as data input to the Multiplexer. **(10 M)**

7. Based on the truth-table for the given M N Flip flop, determine the characteristic table and excitation table. Given the necessary logical expressions. In addition, convert M N flip flop to T flip flop. **(10 M)**

CLK	M	N	Q_{n+1}
0	X	X	Q_n
1	0	0	0
1	0	1	Q_n
1	1	0	$\bar{Q}_n$
1	1	1	1

8. A 6-bit serial input parallel output shift register is shown in the figure. If the initial data of the shift register is 110001, then determine the output of the shift register after 5 clock pulses.



(10 M)

9. Design the synchronous counter which goes through the sequence as shown below using T flip-flop

$0 \rightarrow 3 \rightarrow 2 \rightarrow 1 \rightarrow 4 \rightarrow 5 \rightarrow 7 \rightarrow 6 \rightarrow 0$

(10 M)

10. Design a combinational circuit using PROM for the following Boolean expressions: **(10 M)**

$F_1(A,B,C) = \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC$

$F_2(A,B,C) = \bar{A}BC + A\bar{B}C + AB\bar{C}$

$F_3(A,B,C) = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + ABC$

11. (a). Design PLA for the Boolean Functions listed below: **(10 M)**

$X(A, B, C) = \Sigma(2, 4, 5, 6)$

$Y(A, B, C) = \Sigma(0, 1, 3, 7)$

(b). Design PAL for the Boolean Functions listed below:

$X(A, B, C) = \Sigma(1, 6, 7)$

$Y(A, B, C) = \Sigma(0, 2, 3, 5)$

12. Design a CMOS Logic Circuit for the following Boolean function. **(10 M)**

i. $Y = (A + B)(C + D.E)$

ii. $Y = \overline{A(B + C + D) + E}$