VIT-AP UNIVERSITY	Final Assessment Test – Winter (2024-25) Freshers - May 2025	
	Maximum Marks: 100	Duration: 3 Hours
e Code: ECE1003	Course Title: Digital Logic Design	
o: 6	Exam Type : **Closed Book**	
20/05/2025	Slot: A2	School: SENSE
		Session: FN

ing mobile phone/smart watch, even in 'off' position is treated as exam malpractice

al Instructions if any:

"*fx* series" - non Programmable calculator are permitted : NO

Reference tables permitted : NO

Answer any TEN Questions, Each Question Carries 10 Marks (10×10=100 Marks)

a) Convert $(67AC.B)_{16}$ to octal. **(05 M)**

b) Convert $(342.54)_8$ to decimal. **(05 M)**

a) Perform BCD addition 167+482. **(05 M)**

b) Simplify the Boolean Function F = (A+B+C) (A+B'+C) (A+B+C') to a minimum number of literals using Boolean postulates. **(05 M)**

Simplify the following Boolean function *F*, together with the don't care conditions *d*, and then express the simplified function in sum-of-minterms form: **(10 M)**

$F(w,x,y,z) = \sum(4,5,7,12,13,14)$

$d(w,x,y,z) = \sum(1,9,11,15)$

a) Write the truth table for an 8x3 priority encoder with a valid bit output indicator. Consider the priority order as follows: $D_2 > D_6 > D_1 > D_5 > D_0 > D_7 > D_3 > D_4$. **(05 M)**

b) Implement a 16x1 multiplexer with two 8x1 and one 2x1 multiplexer. **(05 M)**

Using a suitable decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

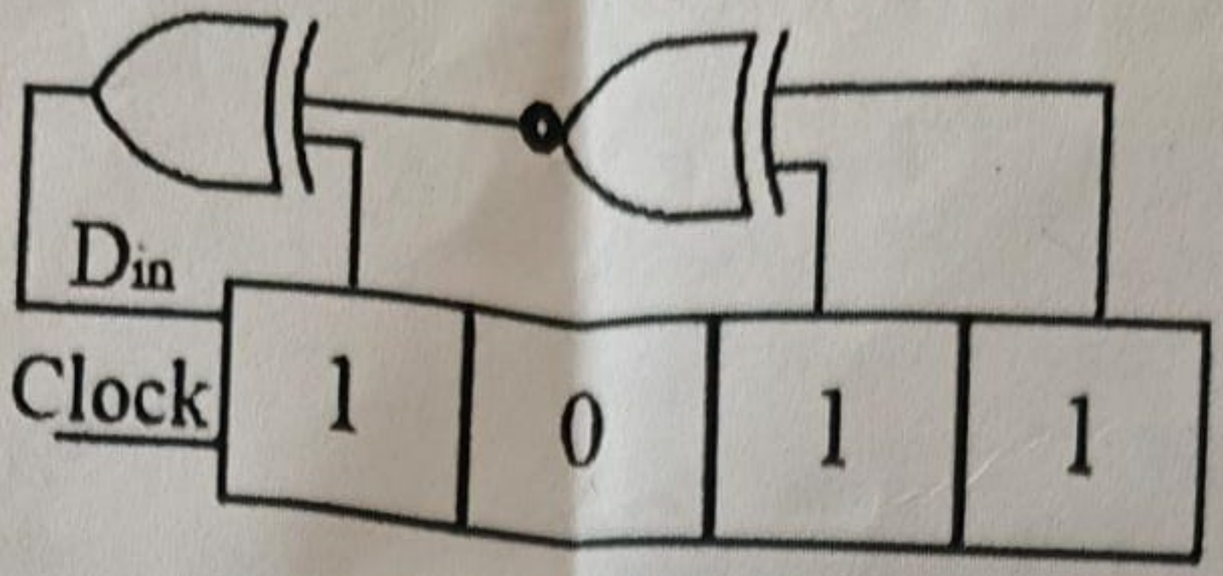
$F_1 = (y'+x)z$; $F_2 = y'z'+xy'+yz'$; $F_3 = (x'+y)z$ **(10 M)**

Implement the following Boolean expression using 4x1 multiplexer and external gates. Connect inputs A and B to the selection lines. The input requirements for the four data lines will be a function of variables C and D. **(10 M)**

$F(A,B,C,D) = \sum(0,1,5,7,8,13,14)$

An AB flip-flop has four operations: complement, clear to 0, set to 1, and no change, when inputs of A and B are 00, 01, 10, and 11 respectively. Convert the AB flip-flop to D flip-flop. **(10 M)**

A 4-bit shift register, which shifts one bit to the right at every clock pulse, is initialized to values 1011 as shown below. Determine the pattern after seven clock pulses and write down the logic table.



9. Design a 3-bit synchronous counter using T flip flop going through the states 0,3,1,7,6,4,0. **(10 M)**

10. Design a combinational circuit using a PROM to convert 3-bit Gray code to binary code. **(10 M)**

. Implement the following Boolean function using PAL logic. **(10 M)**

$X(A,B,C) = \sum m(2,3,5,7)$, $Y(A,B,C) = \sum m(0,1,5)$, $Z(A,B,C) = \sum m(0,2,3,5)$

Implement the following Boolean functions using CMOS logic **(10 M)**

a) $F = \overline{(A + B + C) \cdot D}$

b) $F = \overline{A + B \cdot (C + D)}$

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