VIT-AP UNIVERSITY	Final Assessment Test – Winter (2024-25) Freshers - May 2025	
	Maximum Marks: 100	Duration: 3 Hours
Course Code: **ECE1003**	Course Title: **Digital Logic Design**	
Set No: 7	Exam Type : **Closed Book**	School: **SENSE**
Date: 21/05/2025	Slot: B1	Session: FN

Keeping mobile phone/smart watch, even in 'off' position is treated as exam malpractice

General Instructions if any:

1. **"fxseries" - non Programmable calculator are permitted : NO**
2. **Reference tables permitted : NO**

Answer any TEN Questions, Each Question Carries 10 Marks (10×10=100 Marks)

1. a. Convert 723_{10} to its equivalent hexadecimal.
   b. Given two numbers $X=35_{10}$ and $Y=28_{10}$. Calculate X-Y and Y-X using 2's complement method **(5+5=10 M)**

2. a. Add 389_{10} and 799_{10} using BCD arithmetic.
   b. Convert 48_{10} to corresponding Gray code. **(5+5=10M)**

3. Given a Boolean function $F(A,B,C,D) = \sum(0,1,3,6,7,8,9,13,14,15)+d(2,12)$, implement the system using minimum number of NAND gates only. **(10 M)**

4. Design a 4×2 priority encoder with priority order D1>D2>D0>D3, using basic logic gates. **(10 M)**

5. Realize $F1(A,B,C)=AB+AC+A'B'$, $F2(A,B,C)=\sum(0,2,6,7)$, and $F3(A,B,C)=AC+A'C'+BC'$ using one decoder and 3 OR gates. **(10M)**

6. Implement the logic function $F(A,B,C,D) = C'D+ABC+BCD'+A'B'D$ using one 8×1 multiplexer with ABC as select lines. **(10 M)**

7. Convert a T flip-flop to an AB flip flop which has the functionality as provided below. AB=00 sets the flip flop, AB=01 will reset the flip-flop, AB=10 will toggle and AB=11 will keep the previous value. **(10 M)**

8. A sequential circuit shown in Figure 1 has an initial value Q1Q2Q3Q4 = 1010 after how many clocks the register content comes back to its initial value. **(10 M)**

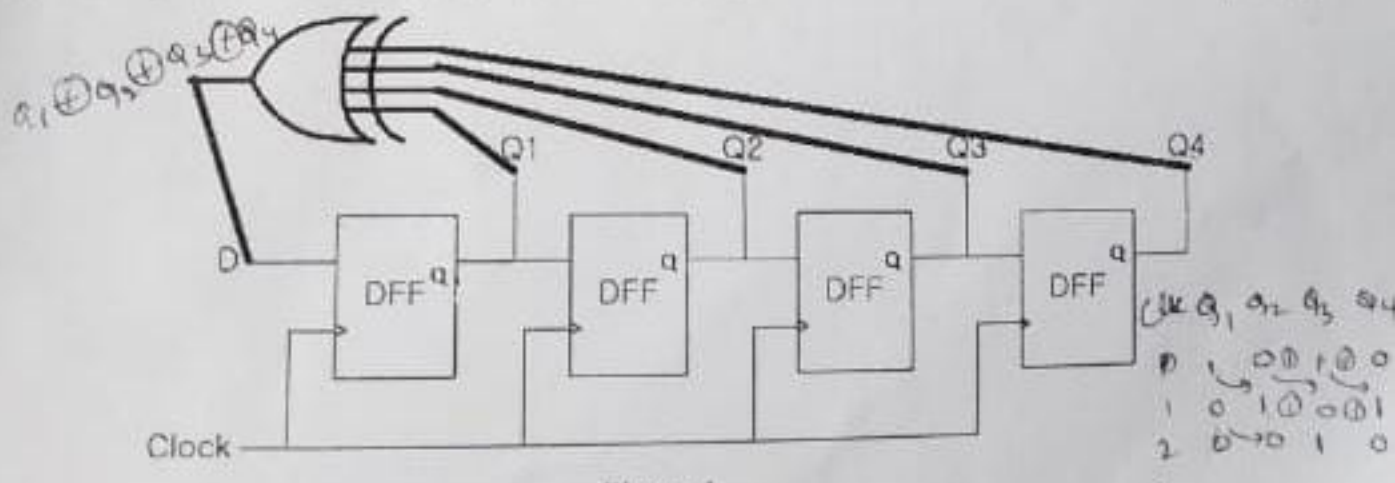

Figure 1

9. Design a synchronous circuit to obtain following sequence of numbers 1,3,5,7,0 using D flip flops and logic gates. **(10M)**

10. Design a BCD to excess 3 code converter using programmable read only memory. **(10M)**

11. a. Implement the Boolean function F1(A,B,C)= A'BC'+B'C+A'B'+AB' and F2(A,B,C)= A'BC'+A'B'C'+AC' using PLA.
    b. Implement F1(X,Y,Z)= $\sum(0,1,2,3,6)$ and F2(X,Y,Z)= $\sum(1,4,5,6,7)$ using PAL. **(5+5=10M)**

12. Design a CMOS circuit to implement
    a. F1= ABC+A'B'
    b. F2=(AB'C'+ AC')' **(5+5=10M)**

QP MAPPING

Q. No.	E/A/T	Module Number	Marks	BL	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped
Q1	E	1	10	1	1	1, 2, 3	1	
Q2	A	1	10	1	1	1, 2, 3	1	
Q3	A	1	10	4	1	1, 2, 3	1	
Q4	T	2	10	3	2	1, 2, 3	1,2	
Q5	E	2	10	4	2	1, 2, 3	1,2	
Q6	T	2	10	4	2	1, 2, 3	1,2	
Q7	A	3	10	3	3	1, 2, 3	1,2	
Q8	T	3	10	2	3	1, 2, 3	1,2	
Q9	A	3	10	5	3	1, 2, 3	1,2	
Q10	E	4	10	5	4	1, 2, 3	1,2	
Q11	T	4	10	2	4	1, 2, 3	1,2	
Q12	A	5	10	5	5	1, 2, 3	1	