TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2083 Baishakh

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic (*EX 401*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Write down the advantages of digital system over analog system. Define BCD and EBCDIC code. [2+4]
2. Explain the positive and negative logic of digital system. Show that positive logic XNOR gate is equivalent to negative logic XOR gate. [2+3]
3. Perform the following code conversions. [4×1]
   a) $(419.52)_{10} = (?)_{16}$
   b) $(BA.3D)_{16} = (?)_{8}$
   c) $(01110101)_{Gray} = (?)_{2}$
   d) $(1001\ 0111)_{BCD} = (?)Ex\text{-}3$
4. Simplify the given function using K-map. $Y = \sum_m(0,1,2,3,8,9,10,11,14) + d\sum_m(5,12,15)$. Realize 2-input XNOR gate using only NAND gates. [4+2]
5. Realize a full-adder using a single 4:1 MUX and logical gates. Design the BCD to seven segment decoder, in which obtain the simplest logic expressions for the segments "b" and "f" also draw their circuits. [4+5]
6. What is an encoder? Design an 8×3 line priority encoder with truth table and circuit diagram. [2+6]
7. Explain the operation of 4-bit parallel-in-serial-out (PISO) shift register with timing diagram for the given data pattern of 1011 in the input up to 10^{th} clock system cycles. [3+3]
8. Construct an asynchronous decade counter with positive-edge triggering clock system. [6]
9. Differentiate between synchronous and asynchronous counters. Design a mod-5 synchronous counter using SR flip-flops. [2+7]
10. Design a sequential machine that detects 1101 serial sequence of message from the input, X which makes output, Z high (1). Use T flip-flops only. [11]
11. What is a ROM? Distinguish between PAL and PLA memory devices. [2+4]
12. With the help of functional block diagram, explain the operation of frequency counter circuit. [4]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2082 Shrawan

Exam.	Batch Out		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic (*EX 401*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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- ✓ *Assume suitable data if necessary.*

1. Explain a positive logic and the negative logic with suitable examples. [3]
2. Perform the following code conversions. [4×1]
   i) $(41A.2D)_{16} = (?)_8$
   ii) $(37.85)_{10} = (?)_8$
   iii) $(19)_{10} = (?)_{Gray}$
   iv) $(1100\ 0011)_{Excess\text{-}3} = (?)_{BCD}$
3. a) State the De-Morgan's theorems. [2]
   b) Realize 2 inputs XOR gates using NOR gates only. [3]
4. What are the minterms and the maxterms? Simplify the following logic function using K-map and implement the result using NAND gates only. [2+4+2]
   $$Y(A, B, C, D) = \Sigma m\ (0, 1, 2, 4, 5, 9, 12, 15) + d\ (7, 10, 13)$$
5. Implement 16:1 multiplexer using only 8:1 multiplexers. [4]
6. Realize a full-subtractor circuit using a single 2×4 decoder and necessary logic gates. [4]
7. Define an ASCII code. Design a binary to excess-3 code converter circuit using basic gates. [2+6]
8. Differentiate between synchronous and asynchronous sequential logic circuits. How to convert SR flip-flop into JK flip-flop? [2+6]
9. How does serial-in parallel-out (SIPO) shift register function with neat circuit diagram? Show the 1010 data shift mechanism in the timing diagram with up to 9^{th} clock cycles. [3+4]
10. Design a mod-6 synchronous up counter having negative edge triggering clock system using-T-flip-flops in your design. [7]
11. Using Mealy circuit with JK flip-flops design a synchronous sequence detector that produces output Z = 1 when it detects the serial input X = 110. [10]
12. Differentiate between RAM and ROM. How does an EEPROM cell work? [2+3]
13. What is a BCD-to 7 segment display decoder? Explain the frequency counter with necessary diagrams. [2+5]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2082 Baishakh

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic (*EX 401*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. Define digital system and logic level. What is the difference between BCD and binary codes? [1+1+3]
2. Convert the following numbers:
   a) Octal (623.77) to decimal, binary and hexadecimal. [3]
   b) Design a combinational circuit whose input is 4-bit number and output is 2's complement of input number. [5]
3. Define the positive and negative logic. State and verify 3-bits De Morgan's theorem. [2+4]
4. Define the minterm and maxterm. Simplify the boolean function $F = \sum m(2, 4, 5, 13, 14) + d \sum m (0, 1, 8, 10)$ and draw its logic diagram of the simplified boolean function using universal gates only. [2+6]
5. a) Design a 5×32 line decoder using 3×8 line decoder and necessary logic gates only. [5]
   b) Design a circuit that compares two 4-bit numbers, A and B, to check if they are equal. The circuit has one output X, so that X = 1 if A = B and X = 0 if A ≠ B. [5]
   c) Implement the following function with 8:1 multiplexer
   $F (A, B, C, D) = \sum m (0, 1, 3, 4, 8, 9, 15) + d \sum(2, 6, 13)$. [4]
6. Explain the operation of J-K flip-flop with logic diagram, graphic symbol, characteristics table, characteristic equation and state diagram. [8]
7. a) Explain operation of the 4-bit bidirectional shift register with truth table and timing diagram. [6]
   b) Design of mod – 12 asynchronous up counter with positive edge trigger and also draw its timing diagram. [5]
8. Design a sequential machine that has a single input 'X' and single output 'Z'. The machine is required to give high output when it detects the serial sequence of 1110 message. Use T-flip-flops only. [10]
9. Implement the circuit with a PLA of the following Boolean function: $F1 = \sum m (3, 5, 6, 7)$ and $F2 = \sum m (0, 2, 4, 7)$. [6]
10. Explain operation of the basic frequency counter with the block diagram. [4]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2081 Bhadra

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic (*EX 401*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. What are the advantages of digital signals over analog signals? [3]
2. Convert the following number system. [6]
   i) $(21)_8 = (?)_2$ (ii) $(671)_{18} = (?)_{BCD}$ (iii) $(110101.011)_2 = (?)_{10}$
3. State De Morgan's Laws. Construct 2 input XNOR gate using only NOR gates. [2+3]
4. Define minterms and maxterms. Simplify the following using k-map.
   F(A, B, C, D): $\sum$m (0, 1, 2, 4 ,6, 8, 9, 12, 13, 14) [2+4]
5. Design half adder and half subtractor in a single circuit. Perform following operation: [5+4]
   a) $(47)_{10} - (26)_{10}$ subtraction using 2's complement method.
   b) $(10010)_2 - (10011)_2$ using 1's complement method.
6. Design and explain two bit magnitude comparator with necessary diagrams. [5]
7. Realize logic circuit for segment "b" and "d" of the seven segment display decoder. [3+3]
8. Design a full subtractor circuit using half subtractors and one OR gate. [5]
9. Describe the operation of 4 bit SISO shift register, with timing diagram. Consider the input 1011 to be entered into the register. [2+3]
10. Design a synchronous mod-6 up counter using T flip-flops. [7]
11. Build the design of an asynchronous mod-12 up –counter with positive edge triggering clock and use JK flip-flops. [6]
12. Design a sequential machine that produces output Y = 1 when it detects the serial message X = 110 using JK flip-flop. [12]
13. With the help of block-diagram explain the operation of time measurement circuit. [5]

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2081 Baishakh

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Subject: - Digital Logic (*EX 401*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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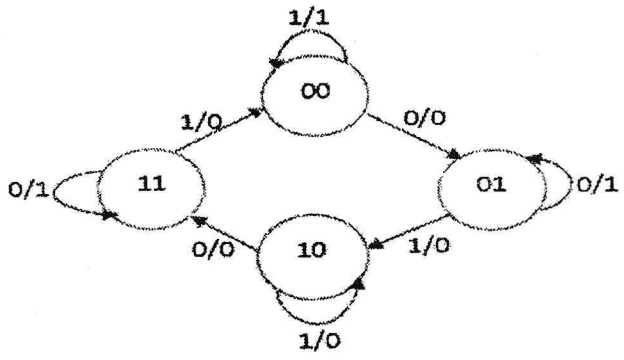
1. Differentiate between discrete and continuous signal with necessary figures and example. Convert $(25.25)_{10}$ to binary and octal equivalent. [2+4]
2. Define min-terms and max-terms. Simplify the function using K-map, $F = \sum(1, 3, 5, 8, 10, 11, 12)$ and $D = \sum(2, 9, 15)$ and also realize the simplified logic circuit. [2+4]
3. Differentiate between encoder and decoder. Design an 8 to 3 encoder with diagrams. [2+5]
4. Explain the applications of de-multiplexer. Subtract 011 from 010 using 2's complement method. [2+4]
5. Differentiate between de-multiplexer and decoder. Construct 4×16 line decoder using 2×4 line decoders with enable. [2+5]
6. Write down the advantages of JK flip-flop over SR flip-flop. Explain the operation of D flip-flop with necessary diagrams, truth tables and timing diagram. [2+5]
7. Explain the operation of 4 bit serial –in-serial out (SISO) register with timing diagram for the given data pattern 1101. [6]
8. Convert T flip-flop into JK flip-flop. [6]
9. Find out characteristic equation for SR flip-flop. Design a mod-5 synchronous counter using D flip-flops with negative edge triggering clock system. [3+7]
10. Design a synchronous sequential machine from the given state diagram. Use SR flip-flops for realization. [10]



11. Briefly describe the operation of frequency counter with necessary diagrams. [5]
12. Write short notes on: (Any Two) [2×2]
    a) Negative logic
    b) PROM
    c) ASCII code
    d) MUX tree

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2080 Bhadra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic (*EX 401*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Describe the advantages of digital system over analog system. [3]
2. Perform the following code conversions. [1.5×4]
   i) $(26.75)_{10} = (?)_2$
   ii) $(36.735)_8 = (?)_{10}$
   iii) $(10101)_{gray} = (?)_{10}$
   iv) $(1001\ 1010)_{excess\text{-}3} = (?)_{BCD}$

3. State and prove De 'Morgan's theorems. Construct 2-input XOR gate using NAND gate. [2+3]
4. Simplify the function using K-map $F = \sum (1, 3, 7, 11, 15)$ and $D = \sum (0, 2, 5, 8, 14)$. Also realize the simplified circuit using NAND Gates. [4+2]
5. Realize a full-adder circuit using a single 1:4 demultiplexer and necessary logic gates. [5]
6. What is meant by a decoder? Construct 3×8 decoder using two 2 ×4 decoders and additional gates if required. [1+4]
7. Draw logic diagrams with truth table of D and T Flip-flops. Convert T flip-flop into JK flip-flop. [4+5]
8. Explain the operation of edge triggered S-R Flip-Flop with necessary diagram and truth table. [6]
9. Compare synchronous and asynchronous counter. Design a 3 bit up synchronous counter using T – flip flop. [2+6]
10. Differentiate between combinational and sequential circuits. Explain the operation of asynchronous decade counter with timing diagrams. [1+6]
11. You are provided with a bit sequence 1001 to operate with serial in parallel out shift register. Draw the circuit diagram and timing diagram to illustrate the procedure for storing and retrieving those bits. [6]
12. A asynchronous state machine has one bit serial input. The Y of the machine is set to be high when the input contains the message 011. Draw the state diagram for this machine and design the circuit. Use T Flip-Flop. [10]
13. Write a brief on multiplexing displays. [4]

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TRIBHUVAN UNIVERSITY
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Examination Control Division
2080 Baishakh

Exam.	Back		
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Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic (*EX 401*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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- ✓ *Assume suitable data if necessary.*

1. What is importance of coding? Explain about ASCII code briefly. [1+2]
2. Convert the following number system.
   a) $(101101.011)_2 = (?)_{10}$
   b) $(110111)_{gray} = (?)_2$
   c) $(524)_8 = (?)_{16}$
   d) $(125.25)_{10} = (?)_2$ [1.5×4]
3. Describe positive and negative logic with an example. Construct Ex-NOR gate using only NOR gates. [2+3]
4. Simplify the following expression using K-map. Expression it in SOP format and realize it using NAND gate only.
   $Y = F(M,N,O,P) = \Sigma m(0,1,2,8,12,14,15) + d(5,10,11)$ [4+2]
5. Realize a full-adder circuit using a single 1:4 demultiplexer and logic gates. [5]
6. What is a priority encoder? Find out logic expressions and draw the logic circuit of 4 to 2 priority encoder. [2+4]
7. How can we use flip-flop as a state machine? Convert SR flip-flop to JK flip-flop. [2+5]
8. Differentiate between combinational and sequential logic circuits. Explain the operation of a synchronous decade counter with timing diagrams. [2+6]
9. Describe the logic operation of 4-bit parallel-in serial out shift register with timing diagram of 1011 input data. [6]
10. Design a synchronous mod-5 up-counter using SR flip-flops and draw its timing diagram. [6+2]
11. Design a synchronous machine which has one input, x and one output, z. The output is required to give high when input contains 110 serial message. Implement only JK flip-flops. [10]
12. What is a ROM? Explain it how one bit memory is stored as '1' or '0', based on BJT circuit. [2+4]
13. With the help of block diagram explain the operation of multiplexing display circuit. [4]

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TRIBHUVAN UNIVERSITY
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Examination Control Division
2079 Bhadra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic (*EX 401*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Write down the advantages of digital systems. Define BCD and excess-3 codes. [2+4]
2. Perform the following code conversions. [4×1.5]
   a) $(329.54)_{10} = (?)_{16}$
   b) $(BD.1A)_{16} = (?)_{10}$
   c) $(01010111)_{gray} = (?)_2$
   d) $(1010\ 0111)_{excess\text{-}3} = (?)_{BCD}$
3. Explain the positive and negative logic level of digital system. Show that positive logic level XOR gate is equivalent to negative logic level XNOR gate. [2+3]
4. Simplify the given function using K-map. $F = \sum_m (1,2,3,8,9,10,11,14) + d\sum_m (0,4,12)$. Realize the simplified Boolean function using NAND Gate. [4+2]
5. Realize full-adder using a single 4:1 MUX and logical gates. Design the BCD to seven segment decoder. Obtain the simplest logic expressions for segments "a" and "e" also draw their circuits. [4+6]
6. What is an encoder? Explain 8 to 3 line encoder with circuit diagram and truth table. [1+5]
7. Explain the operation of D flip-flop with necessary diagrams truth tables and make its excitation table. [6]
8. Explain the operation of 4-bit serial-in-parallel out (SIPO) register with timing diagram for the given data pattern 1101. [6]
9. Differentiate between synchronous and asynchronous counters. Design a mod-6 synchronous counter using JK flip-flops. [2+7]
10. A synchronous machine has 1-bit input 'X'. The output 'Y' goes high when input contains the massage '101'. Draw the state diagram, derive the transition table (state table), excitation table and design circuit. Use only T flip-flops. [10]
11. What is a memory device? Distinguish between PAL and PLA memory devices. [2+4]
12. With the help of block diagram explain the operation of frequency counter circuit. [4]

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TRIBHUVAN UNIVERSITY
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2078 Bhadra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic *(EX 401)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. Define analog and digital signal. What are the advantages of digital system over analog system? [2+2]
2. Explain BCD, Excess-2 , Gray and ASCII Code with examples. [4×1.5]
3. a) Define SOP and POS form and convert F = A + BC + ABC into its canonical form. [2+2]
4. Simplify Σm (0, 1, 2, 8, 10, 14, 15) d =(3, 7, 11, 13) using k-map, write its standard product of sum expression and realize it using NOR gates only. [4+3]
5. Implement the given function F = Σ (0, 2, 3, 5, 8, 12, 14) using only one 8:1 MUX. Add the binary numbers 1011 and 1101 by using Full adders. [4+3]
6. Design a 3 bit binary multiplier using binary parallel adder (BPA). [6]
7. Find out the simplest logic circuit as far as possible for the 'e' segment of the seven segment display decoder. [6]
8. Convert SR flip-flop to T filp-flop and draw the timing diagram of SR flip flop. [4+2]
9. Describe the operation of 4-bit parallel in serial out shift register with its truth table and timing diagram for a given data sequence 1101. [6]
10. Design a 3-bit Asynchrounous up/down counter with its truth table and explain it working principle. [6]
11. Design a sequential circuit with T flip-flop and two inputs X and Y. If X=1 and Y=0 the circuit goes through 00 to 01 to 11 to 10. When X=Y=1, the circuit goes through the transition from 00 to 10 to 01 to 11. When X = 0 and Y=1, the circuit goes through 00 to 11 to 10 to 00. When X = Y = 0, the circuit 00 to 01 to 10 to 11 and repeats. [12]
12. Define PLA (Programmable Logic Array). Implement the full substractor using PLA. [2+3]
13. Design and describe 24 hr digital clock. [5]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2078 Kartik

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic *(EX 401)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. List out the advantages of digital signal over the analog signal. [3]
2. Explain ASCII and EBCDIC codes with example. [1.5+1.5]
3. Convert the following number system. [2×2]
   a) $(5A.B)_{16}=(?)_{Excess-3}$
   b) $(1011011)_2=(?)_{BCD}$
4. Define universal gates with example. Explain positive and negative logic. [2+2]
5. Design three input exclusive NOR gate using NOR gates only. [3]
6. Given function F=A(B'+C)+BD, change into its canonical form. Define max term and min term. [3+2]
7. Simplify the given function using K-map $F=\Pi(0,1,4,7,8,10,11,12)$ and $D=(2,3,6,9,15)$ and implement the final expression using NAND gate only. [4+2]
8. Define and design 2-bit binary fast adder. Draw the circuit diagram of full substractor using half substractor. [5+2]
9. Implement the given function $F=\Sigma(0,1,3,6,10,12,14)$ using 8×1 MUX only. [4]
10. Define race around condition. What are the limitation of SR flip flop? Convert JK flip flop to SR flip flop. [2+2+4]
11. Mention the application of shift Register. Explain the circuit diagram of 3-bit switched tail ring counter. [2+4]
12. Design the synchronous MOD-6 counter using –ve edge triggered JK flip flop. [6]
13. Design a sequential machine that detects three consecutive zeros from an input data stream x by making output y=1. (Use SR flip flop in your design) [10]
14. Differentiate between PROM and PLA. Implement the following boolean functions using PAL. [2+2×2]
    a) $A(x,y,z) = \Sigma(2, 4, 5, 7)$
    b) $B(x,y,z) = \Sigma(0, 2, 6)$
15. Explain the operation of digital clock with neat and clean diagram. [5]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2076 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic *(EX 401)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
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1. Write the basic difference between analysis and digital signals with examples. [3]
2. Perform the following code conversions. [1.5×4]

   (i) $(430.25)_8=(?)_{16}$
   (ii) $(39.75)_{10}=(?)_8$
   (iii) $(17)_{10}=(?)_{gray}$
   (iv) $(17)_{excess\text{-}3}=(?)_{BCD}$

3. a) State and prove De-Morgan's laws. [2]
   b) Realize 3 inputs XOR gates using NAND gates only. [3]
4. Define minterms and maxterms. Simplify the following using k-map and implement the result using NOR gates only. [2+4+2]

   $F(A,B,C,D) = \Sigma m\,(0,1,2,5,8,14) + d(4,10,13)$
5. Implement 1:16 demultiplexer using 1:2 demultiplexer. [4]
6. What is hazard? Explain types of hazards with hazard cover techniques used in K-map simplification. [1+4]
7. Define excess-3 code with examp. Design a binary to excess-3 code converter circuit using basic gates. [2+5]
8. Differentiate between combinational and sequential circuit. Explain working principle of master slave JK flip-flop. [2+4]
9. Define shift registers with its application. Explain the working principle of 4 bit Ring counter with its timing diagram. [2+5]
10. Design a 3 bit synchronous up counter where the bit combination of each states are in gray system. (Use T-flip-flop in your design.) [8]
11. Using melay circuit with J-K flip-flops design a synchronous sequence detector that produces output Z=1 when it detects the serial input X=010. [10]
12. Differentiate between RAM and ROM. Implement $F1=\Sigma(1,2,4,6)$ and $F2=\Sigma m(0,2,3)$ using PROM. [2+4]
13. What are the applications of digital devices? Explain frequency counter. [1+4]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2076 Ashwin

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic *(EX 401)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt <u>All</u> questions.*
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1. Differentiate between edge and level triggering system with example.
2. Define Gray Code and convert $(11101)_{\text{Gray code}}$ to binary. When $(FF)_H$ is ANDed with $(CA)_H$ what will be the resulting number.
3. Simplify $F(A, B, C, D) = \Sigma(2, 3, 6, 7, 9, 10, 11)$ and $d = \Sigma(5, 8, 12)$ using K-map. Result in SOP and POS form.
4. Define encoder. Design 4×16 Decoder using 2×4 Decoder only.
5. Explain 2-bit fast Adder with its logical diagram and write the advantage of fast Adder.
6. Explain the operation of J-K flip flop with its logical diagram characteristics table, characteristics equation, excitation table and timing diagram.
7. Explain the 4-bit SISO shift Register with its timing diagram.
8. Design Mod-5 synchronous counter using JK flip flop.
9. Design sequential machine that has one input x and one output z. The machine is required to give output 1 when it contains message 1101 using S-R flip flop.
10. Design 12-Hr. digital clock.
11. Write short notes: (Any two)
    a) Ring counter
    b) Binary parallel Adder
    c) PLA

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2075 Chaitra

Exam.	Regular/Back		
Level	BE	Full Marks	80
Programme	BEI	Pass Marks	32
Year / Part	I / I	Time	3 hrs.

Subject: - Digital Logic *(EX 401)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt <u>All</u> questions.*
- ✓ *The figures in the margin indicate <u>Full Marks</u>.*
- ✓ *Assume suitable data if necessary.*

1. Write down the advantages and disadvantages of digital signals over analog signals. [4
2. Convert the following: [1.5×4
   a) $(53.125)_{10} = (?)_2$
   b) $(615)_8 = (?)_{BCD}$
   c) $(10011)_{Gray} = (?)_8$
   d) $(11001001)_{excess\text{-}3} = (?)_8$
3. State and prove De Morgan's theorem. Design X-NOR gate using anyone of universal gate. [4+2]
4. Simplify the following expressions using K-map and also draw the logical circuit.
   $Y(A, B, C, D) = \Sigma (0, 2, 3, 4, 7, 8, 10, 13)$ and
   $d = \Sigma (5, 6, 12)$ [4+2]
5. Construct the 3-bit magnitude comparator circuit. [5]
6. Implement the following function using 8×1 MUX.
   $F (A, B, C, D) = \Sigma (0, 2, 3, 6, 7, 8, 12, 13, 15)$ [5]
7. Construct Full Adder using half Adder. [4]
8. Explain operation of S-R flip-flop with its logical diagram characteristics table, characteristics equation excitation table and timing diagram. [8]
9. Convert J-K flip flop to S-R flip flop. [6]
10. Explain the working principle of 4-bit parallel in serial out shift register with its timing diagram. [6]
11. Construct an Asynchronous Decade counter. [5]
12. Design a sequential machine that detects 101 from input stream X by making Y is 1. Using J-K flip-flop. [10]
13. What is ROM? Implement given functions $F_1 (A,B, C) = \Sigma (2, 3, 5, 6)$ and $F_2 (A, B, C) = \Sigma (0, 1, 5)$ using ROM. [1+4]
14. Draw the circuit diagram of frequency counter. [4]

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