TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2083 Baishakh

Exam.	Back (New Course)		
Level	BE	Full Marks	60
Programme	BEI, BCT	Pass Marks	24
Year / Part	I / II	Time	3 hrs.

Subject: - Digital Logic (*ENEX 152*)

- ✓ *Candidates are required to give their answers in their own words as far as practicable.*
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Convert the following gray codes to binary codes. [2+2]
   a) 10011
   b) 110001
2. Differentiate between analog and digital signal. Convert 159 to excess-3 code. [1+2]
3. Show that NAND and NOR gates are universal gates. [3]
4. Minimize the function F (A, B, C, D) = $\sum$ m (1, 2, 4, 5, 6, 8, 10, 11, 13, 15) using K-Map and realize it with suitable logic gates. [5]
5. Differentiate between encoder and decoder. Design octal to binary encoder with necessary diagrams. [2+4]
6. Implement a full subtractor circuit using multiplexer. [4]
7. Differentiate between latch and flipflop. Modify a D flip-flop such that it functions as a JK flip-flop. [2+5]
8. Explain the working of 4-bit SIPO register with timing diagram of 1010 data input. [5]
9. Describe the operation of asynchronous BCD (decade) counter with necessary diagrams. [5]
10. Design the synchronous mod-10 up counter using T flip-flop and draw its timing diagram also. [7]
11. Design a synchronous sequential machine that has 1bit serial input X and output Z which will be high when the input contains the message 011 (Use T Flip Flop). [7]
12. Explain about the main characteristics of digital logic families. [4]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2082 Bhadra

Exam.	Regular (New Course)		
Level	BE	Full Marks	60
Programme	BEI, BCT	Pass Marks	24
Year / Part	I / II	Time	3 hrs.

Subject: - Digital Logics (*ENEX 152*)

- ✓ *Candidates are required to give their answers in their own words as far as practicable.*
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Convert the following binary codes to gray codes. [2+2]
   a) 101101
   b) 110001
2. What is 2's complement representation? Perform BCD addition of 23 + 48. [1+2]
3. State and explain De Morgan's Theorem with truth table and necessary diagrams. [4]
4. Minimize the function F (A, B, C, D) = $\sum$ m (0,1,2,4,7,8,9,10,12,15) +d (5,11,13) using K-Map and realize it with suitable logic gates. [5]
5. What is magnitude comparator? Design a 3-bit magnitude comparator. [1+5]
6. Implement a full adder circuit using Multiplexer. [4]
7. Differentiate between combinational circuit and sequential circuit. With necessary steps and implementation, Convert SR flip flop into JK flip flop. [2+5]
8. Write briefly about different types of shift registers. With necessary circuit and timing diagrams, explain the operation of how the shift register is used as a Johnson's Counter. [2+3]
9. Describe the operation of 3-bit ripple up counter with positive edge triggered clock. [5]
10. Design the synchronous mod- 6 counter using S R flip-flop and draw its timing diagram also. [7]
11. Design a synchronous sequential machine that has 1bit serial input X and output Z which will be high when the input contains the message 110 (Use SR Flip Flop). [7]
12. Write a short note on frequency counter. [3]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2082 Baishakh

Exam.	**Back (New Course)**		
Level	BE	**Full Marks**	60
Programme	BCT, BEI	**Pass Marks**	24
Year / Part	I / II	**Time**	3 hrs.

Subject: - Digital Logic (*EX 152*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Define an ASCII code. Use 2's complement method to perform the following addition $(-28 + 12)_{10}$ in 8-bit signed number representation. [1+3]
2. Prove the following: [2×2]
   a) $AB + \bar{A}C + BC = AB + \bar{A}C$
   b) $AB + C(A \oplus B) = BC + A(B+C)$
3. What is a decoder? Design an octal priority encoder with neat circuit diagram. [2+6]
4. Realize the following Boolean function using a single 3×8 decoder. Also simplify the logic function implementing K-map method. [3+3]
   $X(A,B,C,D) = \sum_m (0,2,3,7,8,10,11,14,15)$
5. Design a synchronous 2-bit up/down counter using T flip-flops. [7]
6. Explain the operation of 4-bit parallel-in serial-out (PISO) shift register with necessary circuit and timing diagram for 1101 input data. [3+2]
7. Sketch the circuit diagram of mod-12 asynchronous counter having positive-edge triggering clock system implementing JK flip-flops with neat timing diagram. [3+3]
8. Design a sequential machine that consists of one input, X and one output, Z. The machine is required to give output high (Y=1), whenever it detects the serial sequence of 010 from its input data stream X. Implement only D flip-flops for the designed circuit realization. [10]
9. Draw the circuit diagram of two-input CMOS NAND gate and explain its logic operation briefly and list the characteristics of TTL logic family. [4+2]
10. With the help of functional diagram explain the operation of time measuring circuit. [4]

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TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2081 Ashwin

Exam.	**Regular (New Course-2080 Batch)**		
Level	BE	**Full Marks**	60
Programme	BEI, BCT	**Pass Marks**	24
Year / Part	I / II	**Time**	3 hrs.

Subject: - Digital Logic (*EX 152*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Mention merits and demerits of digital signal over analog signal. [2]
2. Perform the following as indicated: [2×1.5]
   a) (6E.2C)16 = (?)8
   b) (10110110)Gray = (?)2
3. Design the simplest logic circuit for 'f' segment for the BCD-to-seven segment display decoder. [4]
4. Implement Y (A, B, C) = $\sum_m$ (0, 2, 3, 5, 7) using only a single 1:4 MUX. Design a circuit which can realize both the half-adder and the half-subtractor in a single circuit. [3+7]
5. Design a mod-6 synchronous down counter using JK flip-flops. [7]
6. Explain the operation of 4-bit serial-in parallel-out (SIPO) shift register with necessary circuit and timing diagram for input data of1011. [3+3]
7. Describe briefly the operation of 3 bit up/down asynchronous counter having negative edge triggering clock system with neat circuit diagram and timing diagram. [4+3]
8. Design a sequential machine that consists of one input, X and one output, Z. The machine is required to give output high (Y=1), whenever it detects the serial sequence of 101 from its input data stream X. Implement only SR flip-flops for the designed circuit realization. [10]
9. Draw the circuit diagram of two-input TTL NOR gate and explain its logic operation briefly and list the characteristics of CMOS logic family. [5+2]
10. With the help of functional diagram explain the operation of frequency measurement. [4]

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