TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2083 Baishakh

Exam.	Back (New Course)		
Level	BE	Full Marks	60
Programme	BEI	Pass Marks	24
Year / Part	II / II	Time	3 hrs.

Subject: - Computer Organization and Architecture *(ENEX 253)*

- ✓ *Candidates are required to give their answers in their own words as far as practicable.*
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Describe the methods of bus arbitration. Explain the instruction cycle state diagram. [4+4]
2. Write a code for V = $(M + N - O/P) / ((Q - R) \times S/T)$ using three, two, one and zero address instruction. [8]
3. Explain the function of control unit. Give the differences between hardwired control unit and microprogrammed control unit. [4+4]
4. Explain set associative mapping technique with suitable example. Describe the First in First out (FIFO) page replacement algorithm with example. [5+5]
5. Explain Booth's Multiplication algorithm with its hardware design implementation. Multiply 8 × -6 = -48 using Booth's Multiplication algorithm. [5+5]
6. Explain the different types of pipeline hazards with example. [5]
7. How does DMA overcome the problems of programmed I/O and interrupt-driven I/O in computer organization. [5]
8. Explain about how multicore processors improve the software performance issues. [6]

***

TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2082 Bhadra

Exam.	Regular (New Course)		
Level	BE	Full Marks	60
Programme	BEI	Pass Marks	24
Year / Part	II / II	Time	3 hrs.

Subject: - Computer Organization and Architecture *(ENEX 253)*

- ✓ *Candidates are required to give their answers in their own words as far as practicable.*
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Comparison between computer architecture and computer organization. Explain CPI, MIPS rate, MFLPOS rate and Amdahl's law. [4+4]
2. How effective address is calculated in different types of addressing modes? Explain with an example. [8]
3. Differentiate between hardwired control unit and microprogrammed control unit. Describe address sequencing with the help of block diagram. [4+4]
4. Explain associative cache mapping technique with suitable example. Describe the Least Recently Used (LRU) replacement algorithm with case example of miss and hit. [5+5]
5. Write down the flowchart of Booth's Multiplication algorithm. Multiply 7× -5=-35 using Booth's Multiplication algorithm. [5+5]
6. Formulate 4 segment instruction pipeline with branching and interrupts. [5]
7. Comparison between Programmed I/O, Interrupt-Driven I/O and Direct Memory Access (DMA). [5]
8. Explain about how multicore processors improve the hardware performance with respect to parallelism and power consumption. [6]

***