22320

11819

3 Hours / 70 Marks Seat No. | | | | | | | | |

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. Attempt any FIVE of the following: **10**

a) Write the radix of binary, octal, decimal and hexadecimal number system.

b) Draw the circuit diagram for AND and OR gates using diodes.

c) Write simple examples of boolean expression for SOP and POS.

d) State the necessity of multiplexer.

e) Draw logic diagram of T flip-flop and give its truth table.

f) Define modulus of a counter. Write the numbers of flip flops required for Mod-6 counter.

g) State function of preset and clear in flip flop.

Marks

2. Attempt any THREE of the following: **12**

a) Draw the block diagram of Programmable Logic Array.

b) Convert -

(i) $(255)_{10} = (\ ?\ )_{16} = (\ ?\ )_{8}$

(ii) $(157)_{10} = (\ ?\ )_{BCD} = (?\ )_{\text{Excess3}}$

c) Draw the symbol, truth table and logic expression of any one universal logic gate. Write reason why it is called universal gate.

d) Minimize the following expression using K-Map.
$f(A, B, C, D) = \Sigma m\ (0, 1, 2, 4, 5, 7, 8, 9, 10)$

3. Attempt any THREE of the following: **12**

a) Compare TTL and CMOS logic families on the basis of following:

(i) Propagation delay

(ii) Power Dissipation

(iii) Fan-out

(iv) Basic gate

b) Describe the function of Full Adder Circuit using its truth table, K-Map simplification and logic diagram.

c) Realize the basic logic gates, NOT, OR and AND gates using NOR gates only.

d) Describe the working of JK flip-flop with its truth table and logic diagram.

4. Attempt any THREE of the following: **12**

a) Draw and explain working of 4 bit serial Input parallel Output shift register.

b) Draw 16:1 MUX tree using 4:1 MUX.

c) Calculate analog output of 4 bit DAC for digital input 1101. Assume $V_{FS} = 5V$.

d) State De Morgan's theorem and prove any one.

e) Design one digit BCD Adder using IC 7483.

Marks

5. Attempt any TWO of the following: **12**

a) Subtract using 2's compliment method

$(35)_{10} - (5)_{10}$

b) Design a 4 bit synchronous counter and draw its logic diagram.

c) Describe the working of successive Approximation ADC. Define Resolution and conversion time associated with ADC.

6. Attempt any TWO of the following: **12**

a) Design 4 bit Binary to Gray code converter.

b) Compare the following (Any three points)

(i) Volatile with Non-volatile memory

(ii) SRAM with DRAM memory

c) Give block schematic of decade counter IC 7490. Design Mod-7 counter using this IC.