BTCS404

II Semester Examination, June 2019

B.Tech/ B.Tech + M.B.A. / B.Tech + M.Tech. (CSE / IT)

Computer System Organization

Choice Based Credit System (CBCS)

Time: 3 Hrs. **Maximum Marks : 60**

Minimum Pass Marks: 24

Note: (1) All questions carry equal marks, out of which part 'A' and 'B' carry 3 marks and part 'C' carries 6 marks.

(2) From each question, part 'A' and 'B' are compulsory and part 'C' has internal choice.

(3) Draw the neat diagram, wherever necessary.

(4) Assume suitable data, wherever necessary.

Q.1(A) What is meant by von-neumann model? Explain. **03**

(B) What is meant by micro instruction? Explain. **03**

(C) What is meant by addressing modes? Explain its types with certain examples. **06**

OR

Draw the functional block diagram of 8085 microprocessor. Explain in detail.

Q.2(A) What is meant by control unit? Explain. **03**

(B) What is meant by micro programme sequencer? Explain. **03**

(C) Differentiate between hardwired and micro programmed control unit. **06**

OR

Write short note on:

(a) Microcode (b) Micro operation

Q.3(A) What is meant by Instruction set? Explain. **03**

(B) Define the term serial and parallel data transfer. **03**

(C) Define Simplex, Half Duplex and Full Duplex with examples. **06**

OR

Draw the block diagram of direct memory access and explain in detail.

Contd....

Q.4(A) What is meant by virtual memory? Explain.

(B) Explain associative mapping?

(C) What is meant by memory hierarchy? Explain in detail.

OR

Define memory management unit? Explain the significance of it.

Q.5(A) What is meant by multiprocessor? Differentiate it from distributed system.

(B) What is meant by pipelining? Write advantages of pipelining.

(C) Differentiate between instruction and arithmetic pipelining.

OR

Explain vector processing. Differentiate it from array processing.

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IV Semester Examination, May 2018

B.Tech. / B.Tech. + M.Tech. / B.Tech. + MBA [CCE / CSE]

Computer System Organization

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Q.1.(A) Describe general register organization. 03

(B) Draw and label Von-Neumann architecture of computer. 03

(C) Explain various addressing modes of basic computer. 06

OR

Explain 8085 microprocessor organization.

Q.2.(A) Explain fixed point and floating point representation of numbers. 03

(B) Draw the flowchart of Booth's multiplication algorithm. 03

(C) Write down the control signals for completely executing an instruction "ADD R1, M" (where, M is a memory location) with direct addressing mode, for a CPU with single bus organization. 06

OR

Explain IEEE-754 floating point standard.

Q.3.(A) What do you mean by Asynchoronous data transfer? 03

(B) What are major functions of I/O module? 03

(C) Explain the working of Direct Memory Access with diagram. 06

OR

Explain Daisy chaining priority for data transfer.

Contd.....

Q.4.(A) Explain Direct mapping Techniques for cache memory block placement. 03

(B) Explain the concept of virtual memory. 03

(C) Consider a memory system that uses a 32-bit address to addressing at the byte level, plus a cache that uses a 64-byte line size.

a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

b. Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

c. Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag. 06

OR

Explain the various replacement algorithms of cache memory.

Q.5.(A) What is parallel processing? How parallel processing is advantageous. 03

(B) What are the advantages of pipelining? Explain. 03

(C) What are the pipeline hazards? How do they affect the speedup? 06

OR

A non-pipeline system takes 50 ns to process a task. The same task can be processed in six segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for tasks. What is the maximum speedup that can be achieved?

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BTIT 205

B.Tech. / B.Tech. + MBA / B.Tech. + M.Tech.

II Semester Examination, June 2017

[IT / ICT]

Computer System Organization

Choice Based Credit System (CBCS)

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(3) Draw the neat diagram, wherever necessary.
(4) Assume suitable data wherever necessary.

Q.1.(A) Draw & Explain Von-Neumann architecture? What is meant by Von-Neumann bottleneck? **03**

(B) Explain the FLAG structure of 8085 Microprocessor? **03**

(C) What is the function of the following in computer system?

(a) Accumulator (b) Program counter
(c) Instruction register (d) Memory data register **06**

OR

Write short note on Register transfer language (RTL)?

Q.2.(A) What is Hardwired Control Unit? **03**

(B) Define Micro Program? Explain Nano programmed control unit? **03**

(C) Explain working principal of Micro Program Sequencer with the help of diagram? **06**

OR

Explain Micro Instruction Formats? How are they associated with control unit. Explain?

Q.3.(A) What do you understand by serial/parallel & synchronous/Asynchronous transfer?

Contd.....

(B) Differentiate between programmed I/O & Interrupt initiated I/O? 03

(C) Explain DMA in detail? 06

OR

Explain the classification of Instruction set of 8085 Microprocessor with suitable example?

Q.4.(A) Explain memory hierarchy? 03

(B) Write a note on Memory Management Hardware. 03

(C) What is Cache Memory? Enlist different characteristics of cache memory & explain importance of cache memory in computer system? 06

OR

Explain associative memory with its hardware organization. How the data is read and write in the associative memory? Explain.

Q.5.(A) Explain Parallel & vector Processing? 03

(B) Explain four segment Pipeline? 03

(C) Explain Arithmetic pipeline in detail? 06

OR

Explain instruction pipeline.

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BTCS404

IV Semester Examination May-June 2019

B.Tech./B.Tech+M.B.A/B.Tech+M.Tech.

[CCE/CSE/CSE-CC/CSE-CMC/CSE-BDA/CSE-CYFS]

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(3) Draw the neat diagram, wherever necessary.

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Q.1.(A) Draw the block diagram of Von Newman model? **03**

(B) Explain the data transfer between register and memory. **03**

(C) What is the difference between a direct and indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? Give at least three examples of each type. **06**

OR

Draw the functional block diagram of microprocessor 8085 and explain in brief.

Q.2.(A) What is meant by Hardwired control unit? **03**

(B) What is microprogramming and micro programmed control unit? **03**

(C) Explain Booth's algorithm for multiplication of two fixed point numbers. Illustrate the same with a sample multiplication of two numbers of your choice. **06**

OR

With neat block diagram, explain the working process and concept of micro program sequencer?

Q.3.(A) What do you mean by programmed I/O? **03**

(B) Differentiate between Following: 03

i) Serial / Parallel Data Transfer ii) Synchronous / Asynchronous Data Transfer

(C) Describe interrupt I/O and programmed I/O? Discuss completely how the various signals are exchanged during I/O? 06

OR

Classify the Instruction Set of 8085 Microprocessor and explain 8085 I/O Structure?

Q.4.(A) What is cache memory? Describe process and concept of Cache Memory. 03

(B) Draw and explain the virtual memory organization. 03

(C) Explain associative memory with its hardware organization. Explain how the data is read and write in the associative memory. 06

OR

What are the various mapping methods used with cache memory organization? Explain any one in detail.

Q.5.(A) Explain the basic structure of Vector processor? 0

(B) Explain execution process of Instruction and arithmetic pipelines? 0

(C) Write short notes: 0

i) Inter process Communication ii) Hypercube interconnection

OR

Explain and draw the model and crossbar switch organization for establishing an interconnection network in multiprocessor system.

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