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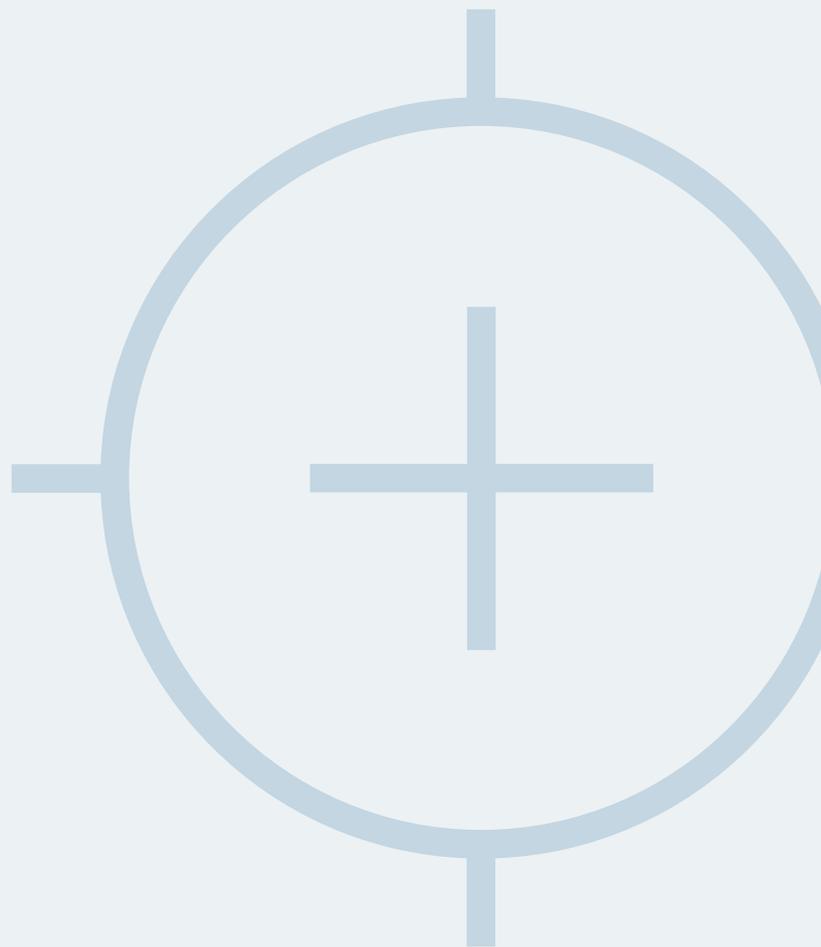
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ABSTRACT

Temporary wafer bonding for thin wafer processing is one of the key technologies of 3D system integration. In this context we introduce the polyimide material HD3007 which is suitable for temporary bonding of silicon wafers to carrier wafers by using a thermo compression process. Coating and bonding processes for 200 mm and 150 mm wafers with and without topography as well as two de-bonding concepts which are based on laser assisted and solvent assisted release processes are presented.

Based on tests with temporary bonded 200 mm wafers, we found a very high compatibility of the bonded compound wafers with standard WLP process equipment and work flows suitable for backside processing of "via first" TSV wafers. Processes like silicon back grinding to a remaining thickness of 60 μm , dry etching, wet etching, CMP, PVD, spin coating of resists and polymers, lithography, electro plating and polymer curing were evaluated and are described in detail. Even at high temperatures up to 300 $^{\circ}\text{C}$ and vacuum levels up to 10-4 mbar, the temporary bond layer was stable and no delamination occurred. 60 μm thin wafers could

be processed and de-bonded without any problems using both release methods. De-bonding times of less than a couple minutes can be realized with laser assisted de-bonding and several minutes with a solvent based release. Compared to glues of other temporary handling systems, the proposed material offers the highest temperature budget for thin wafer backside processing as well as fast and easy de-bonding at room temperature.

1. INTRODUCTION – REQUIREMENTS IN TEMPORARY WAFER BONDING TECHNOLOGY

The fabrication of ultra-flat devices and stacked architectures is becoming more important than ever. Thus, technologies for extreme wafer thinning, thin wafer handling and thin wafer backside processing as well as assembly strategies for thin components are imperative to enable three-dimensional system architectures based on through silicon vias (TSVs) and stacked ICs. ^[1, 2, 3]

Today, due to technological and economic reasons typical TSV depths are in the range of less

than 100 μm with declining tendency. Thus, the fabrication flow of such devices involves thinning of the wafers in order to match their thickness to the TSV depths. After thinning, the wafers need to be further processed to connect the TSVs with routing and contact structures which is highly sophisticated and challenging since wafers with less than 100 μm thickness cannot be handled using standard semiconductor fabrication and handling equipment. To enable processing of the thin wafers they need to be mechanically stiffened by temporary carriers, which can be easily released after the processing is finished. Based on the broad variety of different boundary conditions for thin wafer processing like process type, wafer type to be processed and final device application, there are a lot of different requirements which temporary carrier solutions need to fulfil. In order to reveal these different requirements, Figure 1 shows two generalized work flows of thin wafer processing.^[4, 5]

In step 1, the device wafer is bonded onto the carrier wafer creating a compound wafer. The bonding process needs to be compatible with the properties of the device wafer like surface topography, surface material, restrictions in process temperature etc. Most important is that the temporary adhesive planarizes the topography of the device wafer and that a void free bond interface can be established.

Step 2 involves the thinning and subsequent backside processing of the device wafer. Depending on the particular application, a lot of different processes can be necessary to create the backside structure. In the case of typical TSV backside preparation, besides back grinding, processes like CMP, dry etching, CVD, lithography, PVD, wet etching and electro plating are performed. Thus, it is absolutely mandatory that the compound wafer is fully compatible with all these processes and remains stable even under severe process conditions such as high temperature, high vacuum and immersion into solvents or acids.^[6, 7]

Step 3 includes the de-bonding of the carrier wafer from the processed thin device wafer. The de-bonding process should be fast and as gentle as possible for the device wafer. Residues from the temporary adhesive should be easily removable from the device wafer without long and severe cleaning procedures.

In some process scenarios it is required that the processing ends at the top side of the wafer (step 2b). Therefore, a wafer flipping is required which is realized by transfer bonding and shown in step 2a. Based on that, the temporary bonding and de-bonding concept should enable that a second support wafer can be bonded onto the backside of the device wafer and that the first support wafer can be subsequently removed from the front side.

In recent years, some different thin wafer handling and temporary wafer bonding approaches have been proposed which fulfil more or less the above mentioned requirements and which all have their specific pros and cons. Usually, not all requirements can be fulfilled by one and the same approach, but it seems to be especially hard to combine high temperature stability with broad process compatibility and fast and easy de-bonding capability. With respect to this, we propose a new temporary bonding technology based on polyimide adhesive HD3007 from HD Microsystems which is a competitive alternative to the existing approaches.^[8-12]

The coating and bonding process are discussed in section 2 of this manuscript. Two different de-bonding concepts are discussed in sections 3 and 4. In section 5 we present an evaluation where HD3007 bonded compound wafers were processed according to a typical TSV backside preparation scheme.

The proposed material can also be used for the preparation and flip chip assembly of thin ICs. Corresponding evaluations are discussed in section 6.

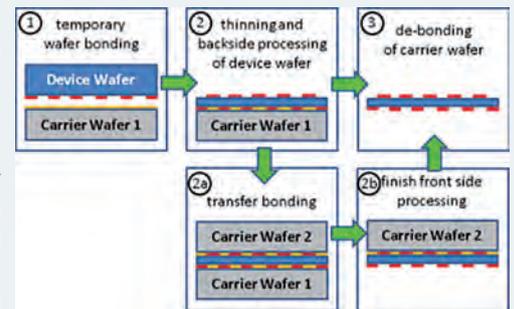


Figure 1. Generalized work flows for wafer thinning and thin wafer processing

Finally, we present a modified version of the material which can planarize higher surface topographies. The corresponding evaluations and results are presented in section 7.

2. TEMPORARY WAFER BONDING USING HD3007

All discussed evaluations in this chapter were performed on 200mm wafers. The material HD3007 is a solution of a polyamic acid in butyrolactone/PGMEA with a liquid viscosity is 9-11 Ps. The solution contains 24-26% non-volatile contents. The cure condition is 250°C-300°C for 60 min. The cured films have a glass transition temperature of 180°C and a CTE of 50ppm/K. The weight loss after 10 min at 350°C accounts for 0.2%. [13-16]

Firstly the coating was optimized using a fully automated coater system ACS200 from SUSS MicroTec. In the final process we used a center dispense of the liquid material followed by a spread spin at 1000rpm for 10s. After spread spin, the material was spun off at 1400rpm for 60 s. After a two-step prebake at 90°C for 90s and 120°C for 90s the material was cured for 60min at 290°C under nitrogen atmosphere. Figure 2 shows a typical thickness distribution of a cured HD3007 film on a 200mm wafer. Excluding the edge bead, the film thickness has a mean value of 4.1µm with a deviation of +/-0.4µm. The edge bead zone has a width of 5mm with a maximum increase of the film thickness of 7µm at the rear edge.

After the coating optimization was finished the wafer to wafer bonding tests were performed using a fully automated wafer to wafer bonder from EVG. In these tests the coated silicon wafers were bonded to 500µm thick glass wafers of type Schott B33.

For handling inside the machine, the wafers were placed onto a rigid bond tool with the coated silicon wafer as bottom wafer and the glass wafer as top wafer. Three distance holders of 200µm thickness were used to ensure a separation gap between the two wafers before

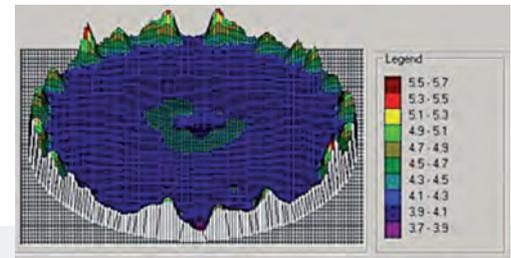


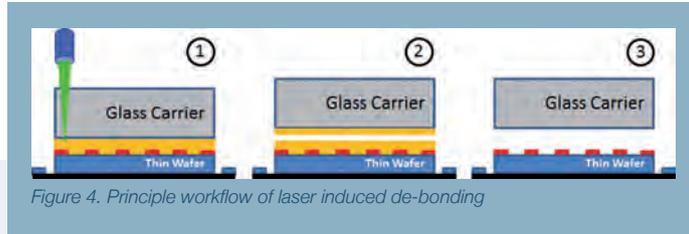
Figure 2. Thickness deviation of cured HD3007 film at 200mm wafer

the bonding sequence was started whereas the bonding sequence is defined as a set of recipe commands performed inside a bond chamber after the bond tool with the wafers was loaded into the bond chamber.

For the first trials we alternated three main parameters of the bonding sequence which are bond temperature, bond pressure and bond time within a range of three set points each. Temperature was alternated between 200°C, 275°C and 350°C, pressure was alternated between 0.07MPa, 0.14MPa and 0.22MPa and time was alternated between 10min, 35min and 60min. The value 0.22MPa represents the maximum pressure of the used bond chamber by using 200mm wafers.

After the bond chamber had been closed, the bond tool remained for 8min on the bottom chuck of the bond chamber which was preheated to 125°C. This was done to enable the bond tool and wafers to heat up and drive out water from the HD3007 film. Then, the chamber was evacuated to a vacuum level better than 1*10⁻³mbar and the temperature of the bottom heater was increased to the corresponding bonding temperature of the particular experiment. After the temperature had been reached, the separation flags were moved out between the wafers so that the surfaces could touch each other and the corresponding bond force was applied for the specified bonding time.

Based on these first screening tests, we found that HD3007 could be well bonded at 350°C independent from the chosen bond force and bond time of the test matrix. The samples bonded at 200°C showed severe bond defects, whereas the samples bonded at 275°C displayed only a few bonding defects. In later experiments with a finer mesh between the evaluated process conditions, we found bonding processes working from 275°C by using a pressure of 0.22MPa and a bonding time between 1 and 10 minutes. It was also found that the prebake inside the bond chamber could be skipped if the chamber is immediately evacuated after



the wafers were loaded. Figure 3 shows some plots of the major bond parameters of typical bonding processes for HD3007.

After bonding process optimization, some tests regarding the characterization of the bond strengths were performed. First tests by insertion of a razor blade between the two wafers showed that the bond interface appears to be very strong. Later, die shear tests were performed. However, at room temperature HD3007 shear failure never occurred since the silicon or glass always failed due to fractures before. A repetition of the test at approximately 150 °C showed shear strength of the adhesive of 40MPa.

3. LASER INDUCED DE-BONDING OF HD3007

A de-bonding of the silicon and glass carrier wafer can be obtained by irradiation of the HD3007 bond layer through the glass wafer using a 248nm excimer laser. The absorption spectrum of HD3007 shows, that wavelengths <248nm are fully absorbed within a 200nm thick film of HD3007. Thus, above a certain value of energy fluence the material is decomposed within this zone so that the bond layer is opened. Due to that, the de-bonding zone is always located 200nm behind the glass wafer surface and never closer to the customer wafer.

Results show no adverse effects of the excimer laser debond process. The de-bonding mechanism itself is not dependent on the thickness or thickness deviation of the HD3007 bond layer. Figure 4 shows the principle workflow of the excimer laser induced de-bonding approach.

The de-bonding tests were performed with 200mm wafers at Tamarack Scientific (USA) using its M42X high speed excimer laser system featuring an x-y moving stage and on-the-fly laser processing as shown in Figure 5. The compound wafers were either mounted onto a film frame carrier or directly chucked with the glass side up onto the stage which drove the wafer under the laser beam (picture 1 in Figure 4). The movement of the stage was controlled a

way that the exposed laser spots overlap each other by ~50µm. With an appropriately sized laser, a complete 200mm wafer could be laser irradiated in < 30s. After the laser irradiation, the glass wafer could be easily removed from the silicon wafer by using some vacuum tweezers (picture 2 in Figure 4).

After excimer laser detach, both the device and carrier wafer need to be cleaned to remove the remaining HD3007 film, which is roughly 200nm thick at the glass side and in the range of several micrometers at the silicon side (picture 3 in Figure 4). For the cleaning procedure we used EKC865TM remover which is an excellent stripping agent for HD3007 and has a proven compatibility with metals and cured polymers. By immersion of the wafer into a 60 °C warm remover bath, the remaining 4-5µm thick HD3007 layers could be removed within less than 30s. Even the 200nm thin layers on the glass wafers could be removed by this method.

4. SOLVENT BASED DE-BONDING OF HD3007

Figure 6 shows the principle workflow of solvent based de-bonding. To enable a fully solvent based release process, perforated carrier wafers are required. Due to that, a suitable remover can dissolve the glue directly at the bond interface and release the carrier from the thin wafer. For the release process the compound wafers are mounted on a film frame with the perforated carrier facing up (picture 1 in Figure 6). Following, the sample is immersed into a tank with tempered EKC865TM remover to dissolve the HD3007 bond layer (picture 2 in Figure 6). For the evaluations we used bath temperatures between 60 °C, and

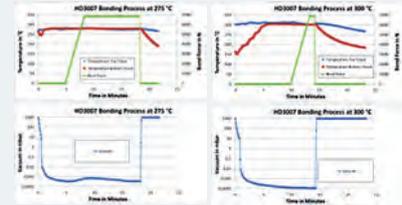


Figure 3. Two optimized processes regimes for HD3007 wafer to wafer bonding at 275 °C and 300 °C



Figure 5. setup of laser de-bonding with 248 nm UV excimer laser and x-y moving stage

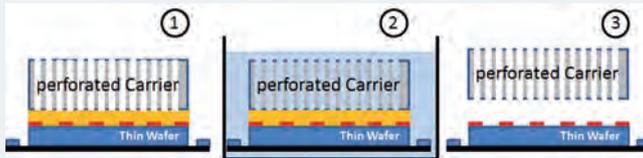


Figure 6. Principle workflow of solvent based de-bonding

80 °C and obtained a detach time for the carrier between 16.5 min and 6.5 min. After the release was done, a further cleaning and rinse process was performed to remove the remaining glue residues from both carrier and device wafer (picture 3 in Figure 6).

In the described experiments perforated glass carrier wafers by Schott Advanced Optics (Germany) were used. The used wafers had a thickness of 500 μm and perforations all over the whole wafer area. The perforations had round shape with a diameter of up to 370 μm and a pitch of 500 μm. Figure 7 shows an example of a bonded compound wafer composed of a silicon wafer and a perforated carrier wafer. The perforated carrier wafer is facing up. As can be seen in the picture, the holes are distributed over the entire surface of the carrier wafer except in a 5 mm wide edge exclusion zone. Due to this edge zone, the HD3007 cannot properly be dissolved here which prevents a full wafer release. To solve this issue, we had to cut away the edge zone for our experiments. But to make this a feasible approach for industrial use, the edge zone should shrink to a width of 1 mm which could be bridged by solvent diffusion along the bond interface.

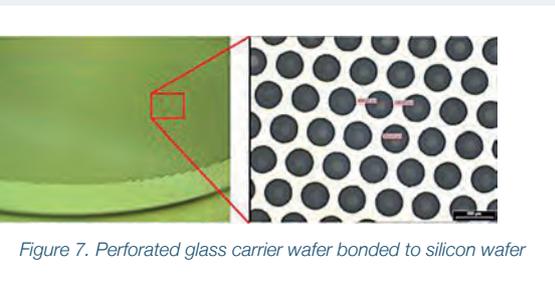


Figure 7. Perforated glass carrier wafer bonded to silicon wafer

Due to the reduced surface area of the perforated glass carrier wafers which is approximately 50% of the regular wafer surface the bond pressure during wafer bonding was also reduced by the same percentage. Apart from this change the optimized bond processes for HD3007 could be used as described above.

5. EVALUATION OF HD3007 TEMPORARY BONDING FOR WAFER THINNING AND PROCESSING OF THIN WAFERS

After the evaluation and optimization of wafer to wafer bonding and de-bonding had been finished, we ran setup lots to evaluate the whole process chain including wafer thinning and backside processing. All experiments were done using 200mm monitor wafers without TSVs or front side topography. In a first step, the silicon wafers were bonded onto perforated and non-perforated glass carrier wafers by using the process described above. Then the silicon wafers were thinned and subsequently processed based on a standard TSV backside processing scheme as shown in Figure 8. After support wafer bonding (Figure 8/ picture 1), the silicon wafers were back ground to a target thickness value of 70 μm using a DISCO wafer grinder. Following, a silicon dry etch was performed to remove additional 10 μm from the silicon using an advanced silicon etcher from SPTS. So a final silicon thickness of 60 μm was reached with a TTV of around 5 μm (Figure 8/ picture 2) which corresponds to the TTV of the carrier wafers themselves.

In a next step, a 1 μm thick PECVD oxide was deposited onto the backside of the thin silicon wafers (Figure 8/ picture 3). For oxide deposition we

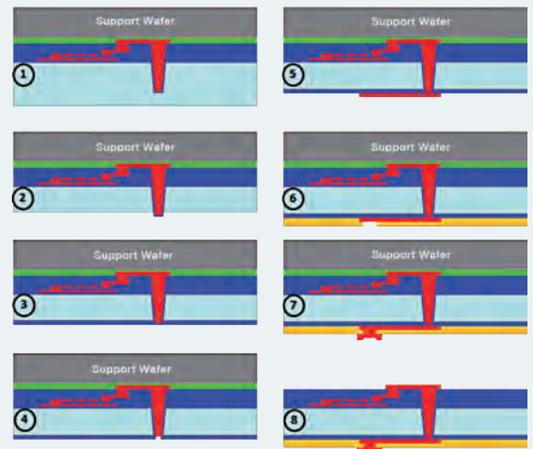


Figure 8. Process flow for TSV backside processing

used both a low temperature PECVD process with 140°C as well as a deposition process with 300°C. Even at a process temperature of 300°C, no fails or deterioration in the temporary bond layers between carrier and silicon wafers could be observed.

In a next step, the deposited oxide was structured by oxide dry etching using a resist mask. This step usually opens the oxide inside the TSV plug diameter. To create the resist mask, a photo resist (AZ series) was spin coated, baked and exposed using fully automated lithography equipment from SUSS MicroTec. The resist development was done by immersion into a developer tank. For etching of the 1 µm thick oxide resist an advanced oxide etcher from SPTS was used. After the oxide was structured, the photo resist was removed by a combination of O₂ plasma ash and wet stripping. An example of the created oxide openings is shown in picture 1 of Figure 9. The sample condition corresponds to the schematic drawing in Figure 8 / picture 4.

After the isolation oxide had been deposited and structured, the redistribution layer was fabricated by semi additive technology using copper electro plating (Figure 8/ picture 5). In a first step a seed layer was sputtered onto the thin wafer backside using standard DC magnetron sputtering. In order to define the routing structure a further lithography was done using AZ photo resist as described above. The copper deposition was done with a sulfuric plating bath and a fountain plater setup using a fully automated electro plating tool from Semitool. Picture 2 in Figure 9 shows an example of the created copper redistribution structure.

In the next process sequence (Figure 8 / picture 6), an isolation layer was deposited and structured to cover and passivate the copper routing. For that, a polymer precursor was spin coated onto the wafer and subsequently structured by lithography and puddle development using fully automated lithography equipment. The polymer was cured

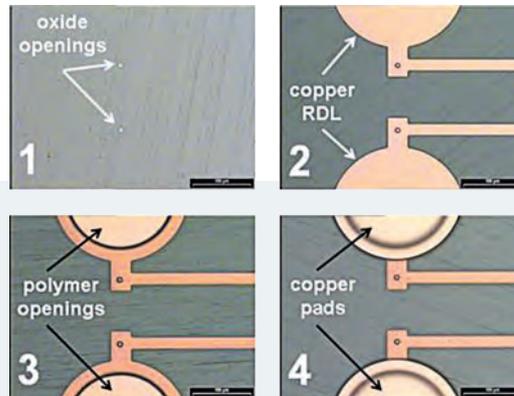


Figure 9. Thin silicon wafer after different steps of backside processing

for 90min at 250°C. Picture 3 in Figure 9 shows an example of the created copper redistribution structure with polymer passivation. The polymer openings are located on top of the large copper pads.

As a final step of the backside processing test, thick copper pads were fabricated as UBM for a subsequent assembly (Figure 8/ picture 7). The used process steps correspond to those used for the copper RDL processing. An example of the final processed structures including copper UBM pads is shown in picture 4 of Figure 9.

Figure 10 shows two cross sectional views of a thin wafer with the processed thin film structures mounted on non-perforated or perforated carrier wafers. In the case of the perforated carrier wafer, which is shown in the right picture, a slope underneath the thin silicon indicates the border between hole area and support area of the perforated carrier.

After completion of the backside processing, the bond layers were inspected carefully. After passing the whole process sequence of backside processing, no delamination or fails could be observed in the HD3007 temporary bonding layers.

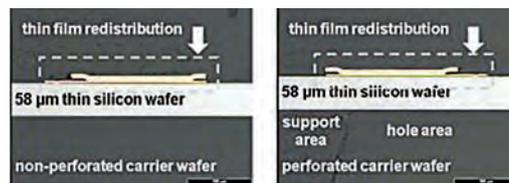


Figure 10. Cross sectional view of processed thin wafers mounted at non-perforated (left) and perforated (right) carrier wafers

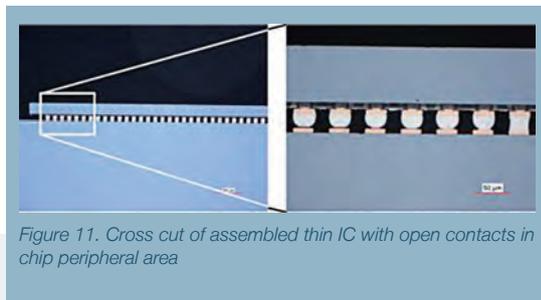


Figure 11. Cross cut of assembled thin IC with open contacts in chip peripheral area

As a final test in this experiment, the de-bonding of the carrier wafers was performed. For that, we used the setup for laser and solvent based de-bonding as described above. The compound wafers were mounted with the side of the thin wafer on film frame carriers. Based on the initial experiments, non-perforated and perforated carrier wafers could be easily removed from the thin wafers. After subsequent cleaning of remaining residues, we obtained thin single side processed wafers mounted on film frame.

6. EVALUATION OF HD3007 TEMPORARY BONDING FOR THIN WAFER BUMPING AND ASSEMBLY OF THIN ICs

Many applications require thin ICs to be assembled in standard flip chip technology by pick & place and reflow. But due to the decreasing

silicon thickness, bow effects induced by the CTE mismatch between the ICs BEOL layers and the bulk silicon lead to severe bending of the devices during reflow soldering. Due to the missing stiffening effect of the bulk, silicon of thinned ICs, these bending effects become more severe with decreasing silicon thickness. Figure 11 shows an example of an assembly issue that occurred with 100µm thin CMOS chips. The chips were fabricated at 200mm CMOS 130nm technology having a 22µm thick BEOL stack comprising 8 routing layers. As preparation for flip chip assembly, the wafers were bumped with AgSn solder on copper UBM and subsequently thinned and diced. The

applied bump height is 25µm/bump pitch is 50µm. As can be seen in the picture due to the bending effects during reflow soldering, the peripheral bumps were not touching their corresponding landing pads at the substrate side. As a consequence, contacts in the peripheral chip area could not be closed and remained electrically open.

To overcome this bending issue, the thin ICs need to be stiffened during the reflow cycle. Therefore, a special process sequence was developed which enables bumping and thinning of IC wafers including subsequent dicing and flip chip assembly by using a temporary chip level support. The corresponding process flow is shown in Figure 12. The process evaluation was performed with the same CMOS wafer material as already described above. The surface topography of these wafers was 0.8µm-1µm and the initial wafer thickness was 725µm (picture 1/ Figure 12).

In a first step, the thick IC wafer was bonded with the active side to a temporary carrier wafer (picture 2/ Figure 12). Following, the IC wafer was back ground to thicknesses in the range of 90µm-50µm using a DISCO wafer grinder. In order to provide a stress relief of the mechanically back ground silicon, another 8-10µm silicon were removed by dry etching using an advanced silicon etcher form SPTS (picture 3/ Figure 12).

Then, as the wafer had reached its target thickness a transfer bonding was performed. For that, glass wafers were prepared with HD3007 coating and cure and subsequently bonded onto the backside of the IC wafer using the 275°C bonding process as already shown in Figure 3 (picture 4/ Figure 12). Now, the carrier wafer was released from the front side of the IC wafer. After that process, we had created a compound wafer composed of glass support wafer and thin IC wafer with active side facing up (picture 5/ Figure 12).

Following, an AgSn bumping process was done

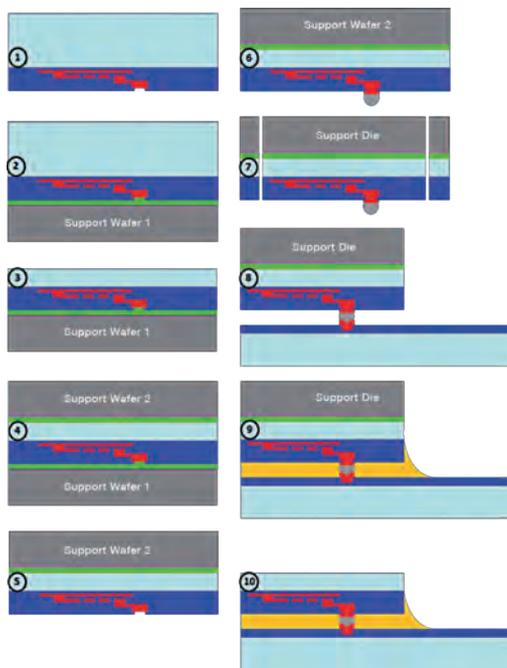


Figure 12. Process flow for preparation and flip chip assembly of thin ICs

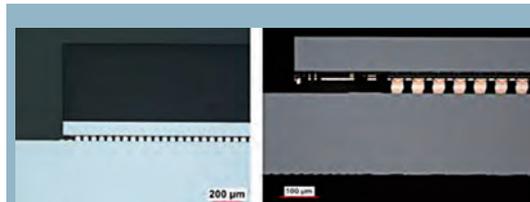


Figure 13. Assembled thin IC before glass carrier release (left) and after glass carrier release (right)

on the active side of the thin IC wafer. Due to the high thermal stability of the HD3007 glue, the bumping process could be done without changing the standard process including sputtering, lithography, electro plating, resist removal, differential etching and solder reflow (picture 6/ Figure 12). Now the sandwich of thin bumped wafer and bonded glass carrier wafer is diced which transforms the carrier wafer into carrier dice located at the backside of each individual thin bumped IC (picture 7/ Figure 12). Due to the stiffening effect of the carrier dice, the thin ICs could be easily assembled by using a standard pick/place and reflow procedure (picture 8/ Figure 12). After IC assembly and under filling, the HD3007 bond layer was exposed through the glass carrier dices and the carriers are removed from the backside of the thin ICs (picture 10/ Figure 12).

Figure 13 shows cross cuts of an assembled thin IC. The left picture shows the condition after reflow assembly. Here, the support chip is still present at the backside of the thin IC. The right picture shows the condition after release of the support die. As can be seen in the pictures, because of the stiffening effect of the support die during the reflow assembly even the peripheral contacts are closed now.

7. EVALUATION OF NEW MATERIAL FORMULATION HD3007HS FOR HIGH TOPOGRAPHY COMPLIANCE

To overcome the thickness limitation of the regular HD3007 material, which is 4-5 µm with single side coating and 8-10 µm if both wafers are coated, a new material version for higher topography compliance was evaluated. The new material is named HD3007HS and gives approximately 30 µm adhesive thickness with one single coating process. All experiments were performed with 150mm wafers.

For the coating we used a fully automated coating tool from SUSS MicroTec with a Gyrset coater. After a spiral dispense a spread spin was

done at 1200 rpm for 4 s followed by a main spin at 1300 rpm for 30s with closed cover. After a prebake of 100 s at 90 °C and 200s at 120 °C a 1 mm wide edge bead removal was done using NMP. After NMP spin off and final bake, the wafers were cured for 4 hour at 200 °C. After cure, that film has a mean thickness of 28-30 µm with a thickness deviation of +/-1.5 µm. With this coating process we evaluated the topography planarization properties of the material. For this, we prepared wafers with copper topography of different heights between 5 and 40 µm. As pattern we have chosen a typical IO pad array design with 90 µm pad diameters and 300 µm spacing in between. The results of this evaluation are shown in the diagram in Figure 14 where the degree of planarization (DOP) is shown as a function of the topography height. The DOP is calculated by subtracting the ratio of adhesive thickness increase over topography and the topography height from 1. So the DOP will be 100%, if there is no adhesive thickness increase on top of topography compared to the surrounding area. The DOP would be 0%, if the adhesive thickness increased on top of topography by the same value as the topography height. As can be seen in the diagram, up to a topography height of 15-20 µm, the DOP is in the range of 80%. With higher topography, the DOP drops steadily down to 40% at 40 µm topography height. The diagram shows furthermore that there is no significant difference between the behavior of the DOP at wafer center and edge.

The measurements were taken at the wafer center and wafer rim (15mm from edge) for each evaluated topography thickness. For that, we did cross cuts after HD3007HS coating and cure and measured the corresponding thickness values by using an optical microscope. For better contrast, the wafers were sputtered with a thin metal film before cross cut preparation. Figure 15 shows two examples of taken cross cuts for the evaluation of the planarization properties. The left picture shows a 20 µm high

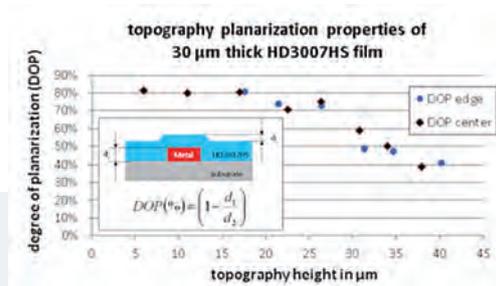


Figure 14. Planarization properties of 30μm thick HD3007HS films

topography and the right picture a 40μm high topography coated with HD3007HS. The left picture represents a DOP of 75% and the right picture a DOP of 41%.

After the coating process was optimized and topography planarization properties were determined, we started to evaluate the bonding performance of the new material. All bonding experiments were performed with non-perforated 150mm glass wafers. On blank wafers without topography we found that the already established bonding processes are also working with the new material. By using the wafers with topography, we found bond defects around the topography, when the topography was higher than 20μm. To enable the bonding of wafers with higher topography, we coated the glass support wafer with the same coating recipe to gain a further 28-30μm adhesive thickness.

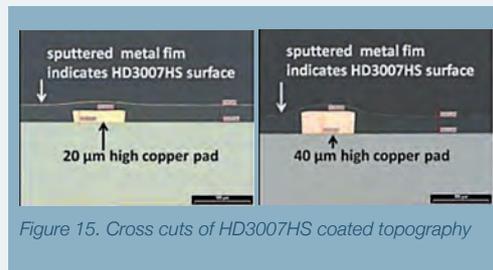


Figure 15. Cross cuts of HD3007HS coated topography

With the additional coating also at the glass wafers, we could bond even the wafers with 40μm topography without any topography related bonding defects. Figure 16 shows cross sectional views of wafers with topography bonded with HD3007HS. The left picture shows 20μm topography at the bond interface. Here, a single coating was used giving a 30 μm thick adhesive bond interface. The right picture shows 40μm topography at the bond interface. To establish this bond, the glass wafer was also coated with HD3007HS which results in a 60μm thick bond interface.

Figure 17 shows the optimized bond process

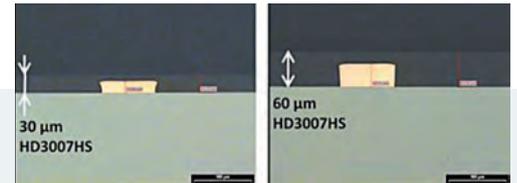


Figure 16. Cross cuts of HD3007HS bonded wafers with topography

for the HD3007HS wafer to wafer bonding. The bond tool with the clamped wafer is load into the chamber with top and bottom chuck preheated to 250°C. After a 3 min wait which is required to enable the bond tool with the wafers to heat up the chamber is pumped down to a vacuum value better than $1 \cdot 10^{-3}$ mbar. Now, the force of 7 kN is applied for 5 min. In order to shorten the overall process time, the cooling inside the bond chamber was skipped. This process is well suited for bonding wafers with HD3007HS coating at both wafers. For wafers with coating only at the silicon side, we recommend a slightly higher bond temperature in the range of 275 °C.

After bonding, the topography wafers were back ground to a target thickness of 100μm. The measured TTV values were in the range between 5-8μm. Furthermore, the wafers were exposed to a similar backside processing as described in section 5 and subsequently de-bonded by laser release. All processes could be run without any restrictions. Due to the thicker adhesive layer, the removal time of the remaining HD3007HS after excimer laser release was increased. When using EKC remover at 70°C, it took 4 min to clear off the 30μm thick films residue free.

CONCLUSION

HD3007 was successfully evaluated as an adhesive material for temporary wafer to wafer bonding. The material can be applied in a thickness of 5-10 μm and bonded in a broad process window at temperatures between 275 °C and 350 °C by using pressures between 0.07 and 0.22 MPa. As carrier wafers non-perforated and perforated glass wafers were used which enable a laser induced or solvent based de-bonding. Both de-bonding methods are working forceless and very fast. For the laser induced de-bonding, which is done at room temperature, we obtained a de-bonding time of less than 1 min per wafer. For the solvent based de-bonding, a minimum

de-bonding time of 6.5 min could be shown at elevated solvent temperature of 80°C. To be compliant with higher topographies at the bond interface HD3007HS was evaluated which can be applied with 30µm thickness in one coating step. A single coating of the material can be used to bond topographies with up to 20µm height. With an additional coating at the carrier wafer topographies of up to 40µm height can be bonded.

The bonded compound wafers are fully compatible to standard equipment and processes used for 3D wafer level packaging such as wafer thinning and thin wafer backside processing for through silicon via fabrication. In detail, the bonded wafers passed processes as back grinding, CMP, dry etching, PECVD oxide deposition, sputtering, lithography, electroplating, wet etching and thermal cure without weakening of the bond interface.

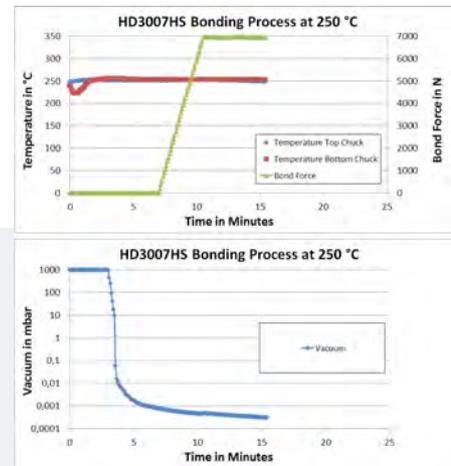


Figure 17. Optimized bond processes for HD3007HS



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Matt Souter graduated in 1992 from CSULB in California with a BS in Mechanical Engineering. He joined Tamarack Scientific in 2001 and has been active in the role of VP of Sales and Marketing for both the Laser Ablation and Photolithography product lines. Much of his focus as of late, has been in the research and development of alternative patterning techniques using Excimer laser ablation as a means to not only meet next generation Advanced Packaging requirements, but also address a means to lower manufacturing costs. Matt has recently authored an exciting new laser process for the removal of metal seed layers in lieu of standard processing approaches addressing both technical limitations as well as a reduction in manufacturing costs. This process is currently patent pending. With the recent acquisition he currently works as Global Sales Director and Laser System Product Manager for SUSS MicroTec.

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