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1. INTRODUCTION

In contrast to IC manufacturing where layers are thin and substrates are planar, MEMS, IC packaging, 3D IC, interposer and display application exhibit a strong 3D topography, typically requiring thick resists to cover the topography. Major lithography challenges of 3D topography are:

- Variation of effective distance of mask (proximity gap) and substrate surface
- Resist thickness variations
- Reflectivity and absorption variation of layer below resist
- Complex reflection and diffraction effects on tapered, shadowing on steep sidewalls

Experimental verification and optimization of design (mask layout) and exposure conditions is very time consuming and expensive as it cannot be done on planar test wafers.

Lithography simulation is an excellent technique for analyzing and optimizing complex scenarios without the need of experiments, and is a standard for high resolution IC manufacturing using projection lithography[1]. For proximity lithography GenISys introduced the LAB[2] simulation software few years ago. Recently, SUSS MicroTec and GenISys enabled "source-mask-optimization" (SMO) for mask aligner, including illumination shaping provided by the new SUSS MO Exposure Optics, and the mask layout[3, 4, 5].

However, calculating the light propagation in a 3D topography is a big challenge. Rigorous methods which have been developed for IC manufacturing fail for MEMS, packaging or display applications because the larger areas to be simulated would lead to excessive data volumes and calculation times. This paper is presenting a 3D topography simulation dedicated for proximity lithography for high-topography, thick resists and larger areas in reasonable calculation time.

2. MASK ALIGNER LITHOGRAPHY SIMULATION

2.1 PLANAR STACKS

Mask aligner lithography simulation for planar cases starts by calculating the so called "aerial image" (the intensities in air at a given distance below the mask) using a fast algorithm based on Kirchhoff scalar diffraction theory. The model takes into account a broad band light source (e.g. spectrum of mercury lamp), and the source

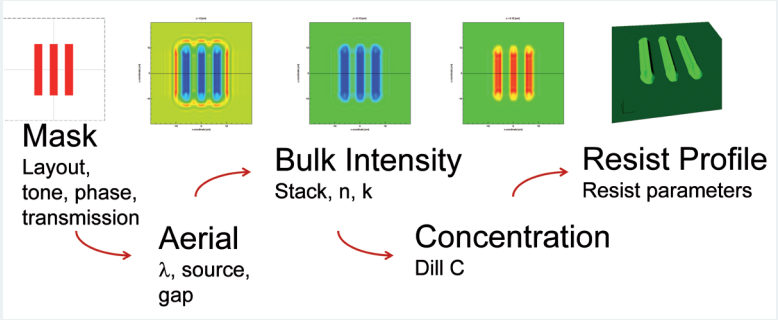


Figure 1. Essential steps in mask aligner lithography simulation; 80% of the lithographic effects are already contained in the aerial and bulk images

shape (e.g. circular with collimation angle, or an arbitrary source shape). This “aerial image” is then propagated into the resist, taking into account all back-reflections from substrate and coatings. LAB simulation software is also able to model resist “bleaching” (change of absorption coefficient during exposure). The well-established Dill Model computes photoactive-compounds concentration (PAC) from the light intensities, and the development process is modeled using empirical models such as MACK4.

2.2 3D SIMULATION PRINCIPLES

Simulation of mask aligner lithography coupled with wafer topography is a challenging task for several reasons. First, the simulation window is typically large (about laterally 100 µm x 100 µm simulation area, vertically 10 µm resist thickness and topography). Second, modeling of broad-band illumination requires repeating the simulation for all wavelengths individually. Third, several different angles of incidence must be taken into account for extended light sources. Last but not least, light propagation in a non-planar stack has to be computed. The usage of established electromagnetic modeling methods such as FDTD (Finite Difference Time Domain) or RCWA (rigorous coupled wave analysis) in case of large volumes is prohibitive because of their high computation cost and memory consumption.

To address the challenges mentioned above, we developed a fast approximate method that exhibits excellent time and memory scaling properties (Table 1). In our method, the simulation domain is divided into homogeneous convex regions. Inside each region, propagation from interface to interface is computed in a single step. Then, transmission and reflection is calculated (Figure 2). The entire procedure is repeated for each interface several times until convergence is reached.

Method	Time Scaling	Memory Scaling
RCWA	$N^6 \times Z$	N^4
FDTD	N^4	N^3
Our Method	N^3	N^2

Table 1. Comparison of different electromagnetic modeling techniques with respect to time and memory consumption. N denotes the number of unknowns along one dimension, Z is the accuracy of vertical discretization.

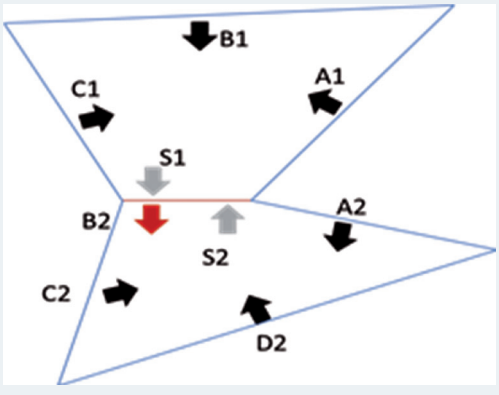


Figure 2. Iterative computation of propagation and transmission/ reflection. For a given interface (here exemplarily B2), first the fields at the neighboring interfaces are propagated to the selected interface and are summed up (S1 and S2). Then, field B2 is computed as the transmitted part of S1 + the reflected part of S2.

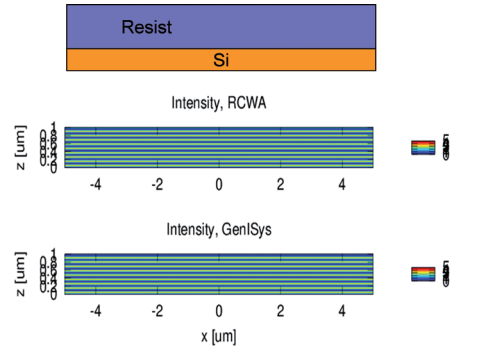


Figure 3. Comparison of TMM and 3D on a planar stack

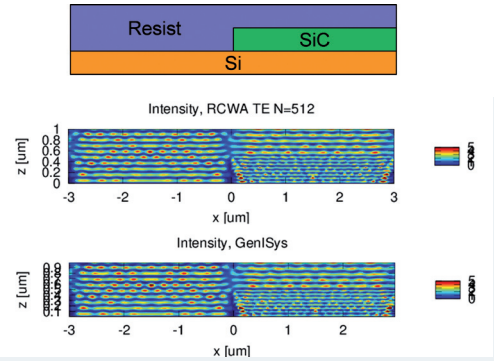


Figure 4. Comparison of RCWA reference and 3D algorithm on a vertical step

2.3 VALIDATION

The method has been validated by comparing the result of the 3D computation to well-known solutions. For planar stacks, the new method results in the same intensity distributions as the well-established TMM algorithm (Figure 2). To test topographic scenarios, the new algorithm was benchmarked on an existing RCWA implementation (Figure 3).

3. INDUSTRY EXAMPLE

The study was done on a 2 micron step in the stack. Would that lead to visible lithographic artifacts?

The method, applied to a real case scenario shows a good agreement to the visible artifacts. Fortunately, the structure turned out to be printable as is – no further optimization was required.

Figure 5. The stack exhibits several "steps", the most pronounced being a 2 micron step; the entire stack is buried under 5.5µ resist; exposure conditions are: broadband illumination, 70µ proximity gap

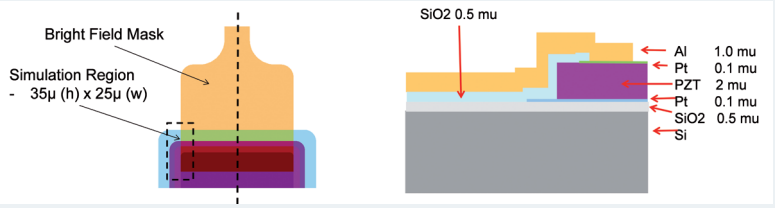


Figure 6. Simulation, XY-View at resist top (left) and resist image (right)

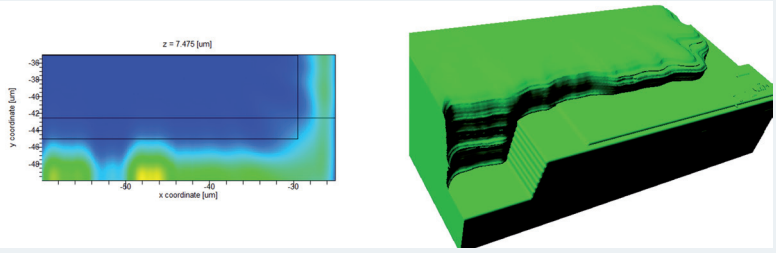
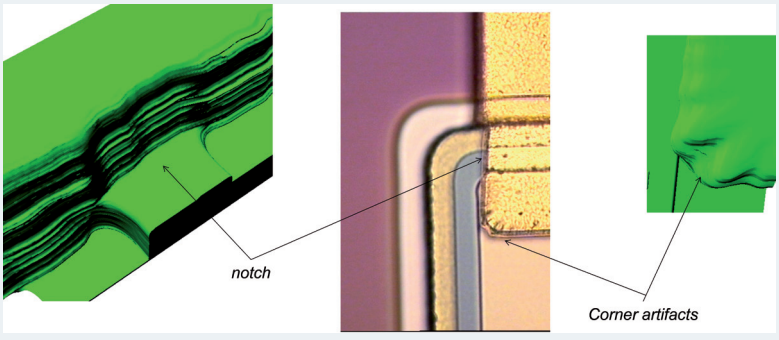


Figure 7. Comparison of resist Image to experimental result (Al layer already etched, resist is still present); the notch is clearly visible, as well as the corner artifacts at the 70µ proximity gap



4. SUMMARY

Lithography simulation enables the ability to transfer the benefits of mask aligners beyond the classical limits by resolution enhancement techniques such as layout optimization (OPC), source shaping, advanced mask technologies (grey-tone, phase shift), or combinations thereof such as source-mask-optimization. The combination with the SUSS MO Exposure Optics opens new opportunities for next generation products for 3D packaging, flat panel display and MEMS products, particularly through the integration of the 3D topography simulation that is capable of computing larger areas, thick layers, and high-topography in reasonable time using off-the-shelf PCs.

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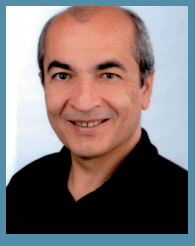
THE AUTHORS

Ulrich Hofmann holds a physics degree (Diplom) from the Technical University in Munich and has more than 20 years experience in the semiconductor industry, working in various technical and management positions on E-beam technologies as well as optical lithography technologies. Ulrich pioneered technologies such as real-time proximity effect correction, hierarchical data processing, and ultra-high bandwidth datapath for massive parallel E-Beam direct write, and drove the development and factory integration of a next generation mask lithography tool. In 2005, he founded GenISys GmbH, a software house providing solutions for the optimization of microstructure fabrication processes for R&D, semiconductor manufacturers and equipment suppliers throughout the world.



Nezih Unal received his Diploma in Electronics Engineering at the University Wuppertal, with a focus area on semiconductor technology. He has started working on the development of Reactive Ion Etching (RIE) processes for IC manufacturing at Motorola in 1988. In 1992 he joined microParts GmbH to develop and manufacture 3D MEMS devices using X-ray lithography. Nezih joined SIGMA-C GmbH as Director of Sales in 2003, and positioned the optical lithography simulation software SOLID in the market. As Vice President Marketing & Sales at GenISys GmbH, Nezih Unal is one of the company's key figures in creating unique solutions that make a difference.

Ralph Zoberbier graduated in Precision Engineering and Microsystems Technology from the University of Applied Sciences in Nuremberg. He joined SUSS MicroTec in 2001 as R&D Project Manager and became International Product Management Aligner in 2005.
Since 2010 he leads the Aligner Product Management team as Director Product Management. With the recent acquisition of Tamarack Scientific Inc. his area of expertise was extended by complementary projection lithography and laser process technology. In 2006 Ralph gained a MBA degree in Entrepreneurship at Louisville University, Kentucky

Ton Nellissen holds a Masters degree in Chemistry from the Utrecht University, The Netherlands. In 1982 he joined Philips, where he worked on semiconductor process development, and became responsible for the development and implementation of colour filters for CCD image sensors. Other activities were in the field of semiconductor packaging where he developed special photolithographic techniques based on inclined illumination and diffractive optics to realize out of plane conductor tracks. Further he was strongly involved in the development of a mask-less imaging technique for pattern-wise UV exposure on photoresist coated substrates. Ton Nellissen is currently active as project leader and senior scientist in the field of process development for MEMS devices. He has authored several papers on micro electronics and packaging and holds also several patents in this field.