

# LED WAFER LEVEL PACKAGING – MOTIVATION, CHALLENGES AND SOLUTIONS TO MEET FUTURE COST TARGETS

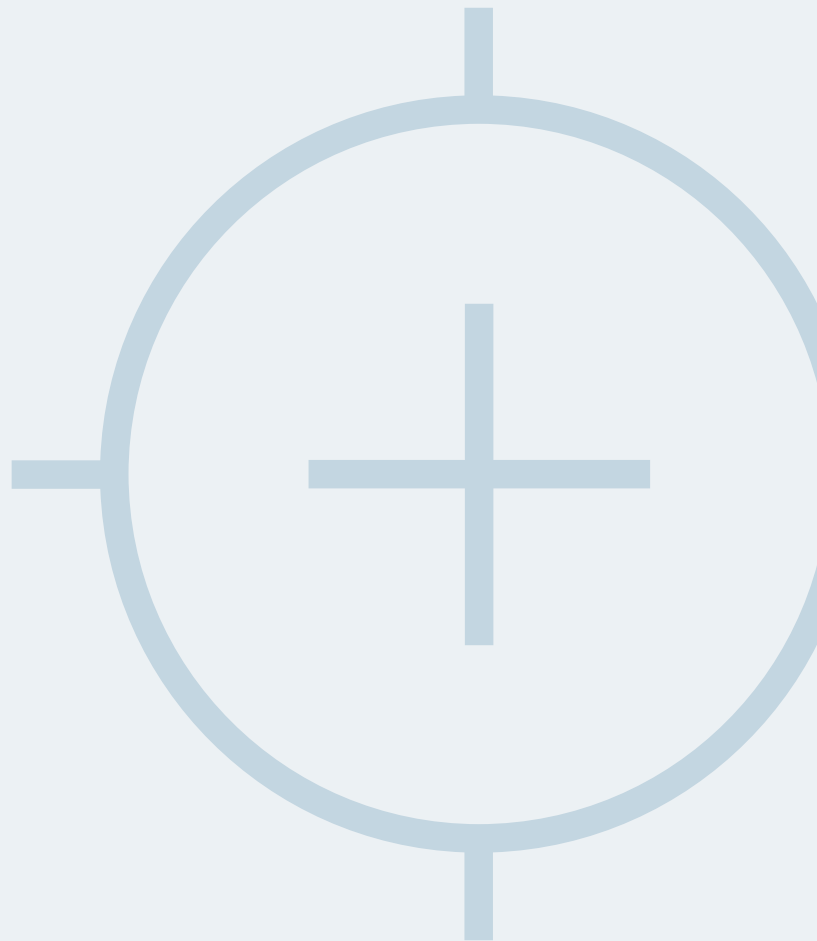
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## LED WAFER LEVEL PACKAGING – MOTIVATION, CHALLENGES AND SOLUTIONS TO MEET FUTURE COST TARGETS

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Since LED became an attractive alternative for general lighting, the market demand for higher brightness, higher efficiency and lower costs was the motivation for improving the LED technology.

Whereas an increase in brightness and efficiency is mostly a question of the LED chip design, a reduction of the costs is in the focus of the manufacturing technology. As Haitz stated in 2000, the cost per lumen falls by a factor of 10 every decade. This, later referred to as Haitz's law<sup>[1]</sup>, is considered the LED counterpart to Moore's law, which states that the number of transistors in a given integrated circuit (IC) doubles every 18 to 24 months. Both laws rely on the process optimization in the production of semiconductor devices. However, at the IC industry it is recognized that an increase in the number of transistors come along with higher costs as manufacturing processes then have to meet

higher requirements. These performance related expenses need to be compensated to keep the overall costs low. Several factors could be key to success, e.g. the introduction of standards, the integration of several functions to minimize the number of process steps or the increase of the wafer size from >2" to 300mm or even 450mm in the near future.

The most perceived approach to lower LED manufacturing costs is a wafer size increase, with the idea to process as many devices as possible at the same time. This was also a reason for introducing wafer level packaging (WLP) in order to avoid packaging processes on die level. Today, WLP is a standard manufacturing process for the IC industry, but the technology also already found its path into other applications like wafer level cameras where opto wafers and device wafers are mounted together on wafer level to reduce costs significantly. Looking into the

LED manufacturing process today, most steps are on die level after chip singularization. Therefore costs are dominated by the huge number of dies often mounting to several thousand dies on one wafer. It is obvious that WLP is clearly beneficial for LED packaging and it is also the path to success for LED adoption in mass markets like general lighting. A few LED manufacturers already work on WLP for LED. However, there are different boundary conditions to adopt WLP of LEDs. In example there is limited usability of WLP processes on the LED device wafer directly. The final processed LED chips need to be singularized and placed on another board or wafer for further packaging (chip to wafer packaging)<sup>[2]</sup>. Nevertheless, this fan-out principle gives additional opportunities. First of all, it allows a fast transition to larger wafer sizes like substrates for further substrate level processing. Moreover, it also allows the implementation and integration of additional functionalities to the LED chip module, e.g. electrical connects,

Zener-Diode, mirrors or optics drivers (Fig. 1), that further can improve the performance of die and package. Nonetheless, a key aspect for adopting WLP in LED manufacturing is to benefit from the know-how of existing packaging manufacturing technology, processes and from the experience of the equipment suppliers in this industry. SUSS MicroTec, a leading supplier of equipment for WLP for many years, offers a broad solution portfolio. Its mask aligners, coat/develop systems and wafer bonders serve not only the IC wafer level packaging industry but also WLP applications in the field of MEMS, CMOS image sensors and wafer level cameras. For example, a fully automated lithography cluster (Fig. 2) enables wafer processing with highest reliability and lowest operator intervention for the full lithography process. However, automation is just one factor. Furthermore the equipment needs to be tailored to match the requirements of WLP applications. Existing concepts for state-of-the-art LED packages (Fig. 3) combine

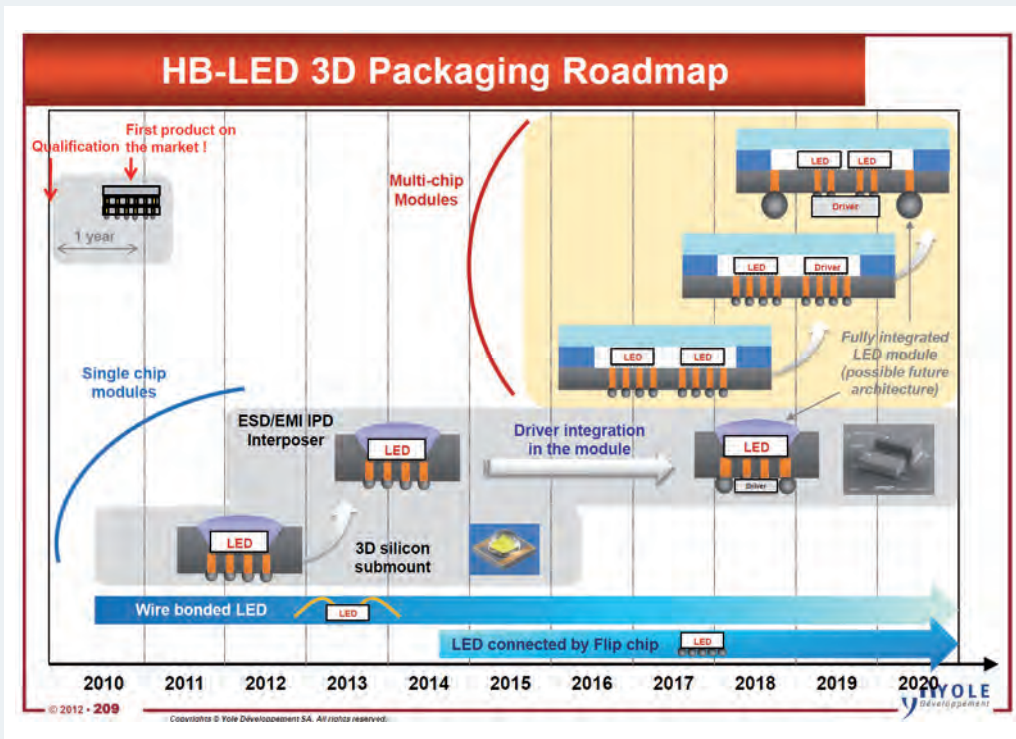


Figure 1. HB-LED 3D packaging roadmap<sup>[2]</sup>

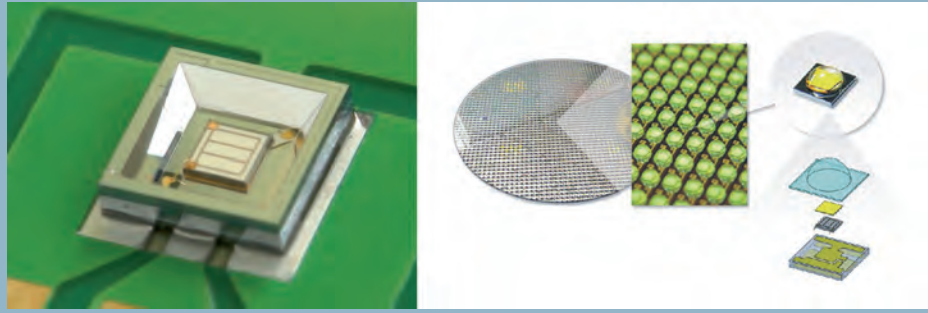


Figure 3. Design concepts for state-of-the-art LED packages based on wafer level packaging technology from Hy-mite (left) and VisEra (right).

several features. The embedded design with thin silicon membranes at the bottom optimizes the thermal contact and therefore minimizes the thermal resistance. Through Silicon Vias (TSV) provide the electrical contact to the SMD mount and inclined, mirrored sidewalls increase the package reflectivity and improve light efficiency. However, the high topography of such concepts often reaches several hundred of microns and requires innovative lithography techniques and semiconductor manufacturing experiences. Not only the formation of the TSV at the bottom of the cavities are challenging, also patterning of

the interconnections from top to the bottom need special equipment and process solutions. Dedicated mask aligner lithography is considered the best to overcome the need for extreme large depth of focus for the exposure process.

For example, SUSS Mask Aligners used in this application are equipped with the SUSS MO Exposure Optics which allows an optimal adaptation of the mask aligner illumination system to the process requirements for best pattern fidelity and highest resolution over severe topography. The innovative illumination system uses two subsequent microlens-based Köhler integrators. The second Köhler integrator is located in the Fourier plane of the first. The new illumination system uncouples the illumination light from the light source and provides excellent uniformity of the light irradiance and the angular spectrum. Spatial filtering allows to freely shape the angular spectrum to minimize diffraction effects at large exposure gaps that can be found when exposing polymers in trenches, groves and vias. In addition telecentric illumination and the ability to precisely control the illumination enables the introduction of resolution enhancement technologies like customized illumination, optical proximity correction and source-mask optimization in mask aligner lithography<sup>[3]</sup>. In addition, perfect patterning on topographies up to several hundred microns requires conformal resist coating over the whole topography (Fig. 4). Here SUSS MicroTec's proprietary AltaSpray coating technology comes into play; a unique resist deposition method that is capable of producing



Figure 2. SUSS MicroTec LithoFab200. The fully integrated cluster for coating, baking, exposing and developing of substrates from 2" to 200mm is specifically designed for volume production.



Figure 4. 50 μm and 150 μm L/S in conformal coated AZ 4999 across 200 μm deep etched trenches. Exposed on a SUSS MicroTec Mask Aligner with dedicated illumination optics.

highly uniform resist films on different 3D microstructures. The AltaSpray technology is capable of coating 90° corners, KOH etched cavities, Through Silicon Vias or lenses with topographies ranging from a few micron to 600 μm or more. The ability to produce conformal resist coatings on severe topography makes them the ideal choice for Wafer Level Packaging applications like 3D image sensor packaging, MEMS and LED.

Nonetheless, these patterning processes are only the first step. They are used for patterning processes of the silicon package. After the placement of the LED dies to the packaging substrate or wafer, the overall packaging process continues on wafer level with phosphor deposition and lens molding. Finally LED manufacturing could benefit from existing technologies as used for Wafer-Level Camera (WLC) manufacturing. For WLC either all components are manufactured on 8" wafer, the opto-wafers are mounted onto the CMOS wafer, or alternatively the lenses are molded directly on the device wafer on wafer level<sup>[4]</sup>. The tool of choice for this application is the SUSS MicroTec Imprint Lithography

Equipment (SMILE). SMILE allows the imprint replication of structures in the micron to millimeter scale on up to 200 mm diameter areas. SMILE uses soft stamps to perform either an imprint process into a puddle dispensed polymer or a transfer process of material that was previously microdispensed into individual micro molds. In both cases the material is typically cross-linked by UV exposure after pattern shaping.

In the last years, the manufacturing cost reduction of LED devices was mainly accomplished by increased equipment throughput, lower Capex, yield improvements and a higher degree of automation using dedicated tools for LED manufacturing. Further significant cost reduction is expected by the adoption of WLP approaches that are already field proven in other industry applications like IC and MEMS WLP. SUSS MicroTec offers a wide product portfolio of high quality equipment which provides tailor made solutions and processes to meet the specific requirements of tomorrow's LED WLP designs.

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Michael Hornung is Technical Marketing Manager at SUSS MicroTec Lithography based in Garching, Germany. During his career at SUSS MicroTec he passed further functions. He was project manager in R&D, responsible for the (nano) imprint technology and other new technologies for mask aligners. He also worked as application engineer for a while and led the application group at SUSS MicroTec for two years. Before he joined SUSS MicroTec he was project manager at CERN in Geneva, Switzerland, working at the inner detector for the ATLAS project. Michael Hornung holds a Ph.D. degree in Natural Science from the University of Freiburg, Germany and an MBA from the University of Applied Science of Ludwigsburg, Germany.