TEMPORARY BONDING AND DEBONDING - AN OVERVIEW OF TODAY'S MATERIALS AND METHODS

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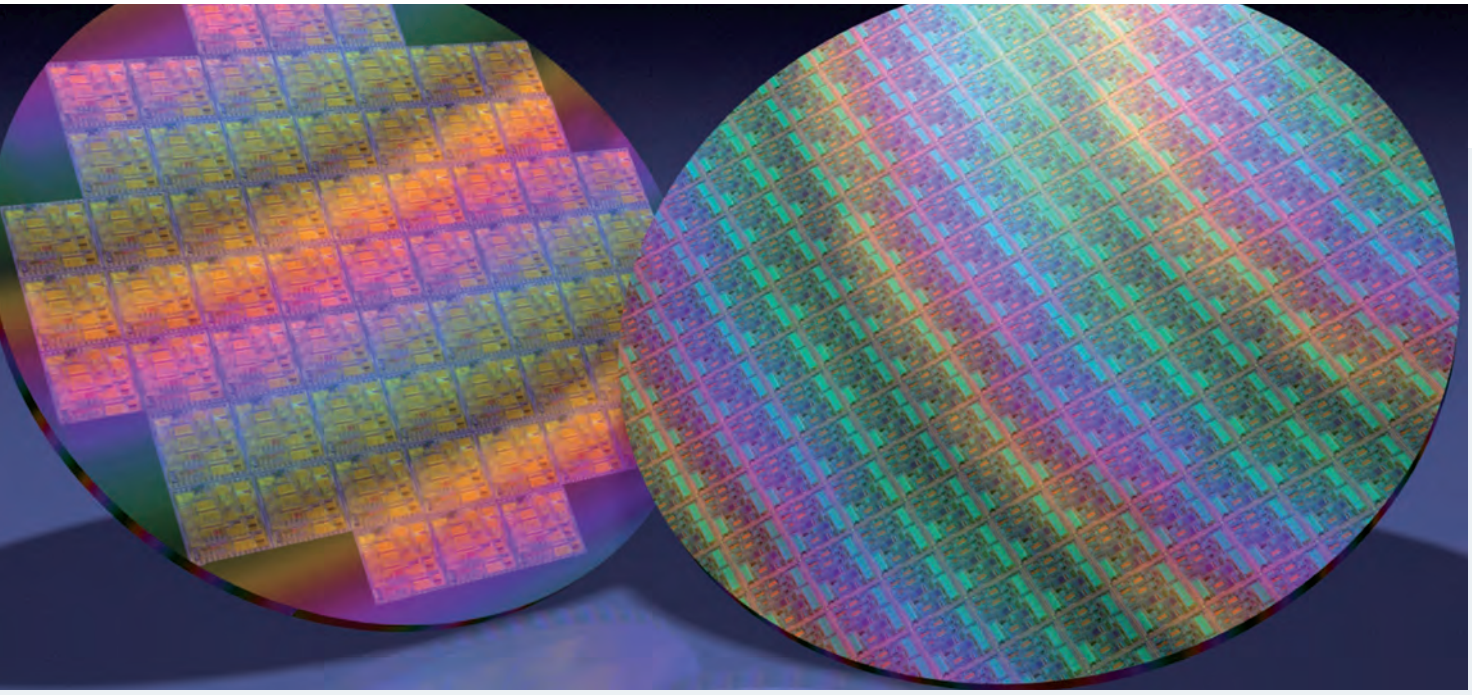

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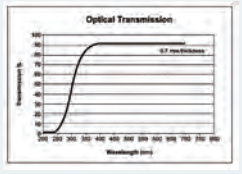
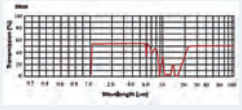




Carrier wafers are an integral part of the temporary bonding process and their selection dictates what type of bonding and debonding methods can be employed. Photosetting adhesives require a carrier wafer that is transparent at the wavelength of light needed for curing – most common being UV radiation. Furthermore, if laser ablation is used for debonding, like the original 3M Wafer Support System, the carrier wafer must allow laser light to pass through to weaken the adhesive bond sufficiently to enable carrier wafer removal.

Mechanical Properties	Corning Glass	Silicon
Density (g/cm^3)	2.38	2.33
Young's Modulus (GPa)	73.6	129.5 [100]
Knoop Hardness (kg/mm^2)	453	1150
CTE (0-300 °C, x10-7/ °C)	31.7	31.5

Figure 1. Comparison of the physical properties of Silicon vs. Glass. [1]

Size of the carrier wafer also needs to be carefully considered. The typical choices are a carrier wafer that is equal to or slightly greater in diameter to the device wafer; however, if the device wafer undergoes edge trimming to reduce the likelihood of cracking and chipping during backgrinding, the effect will be the same as attaching an oversized carrier. Since the device wafer is very thin and fragile at the edges after back grinding there is a handling advantage with an oversized carrier as it serves as a bumper.

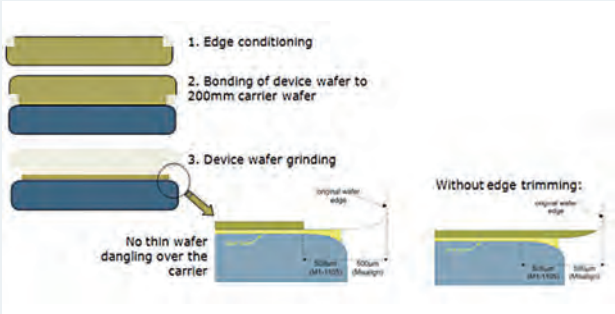
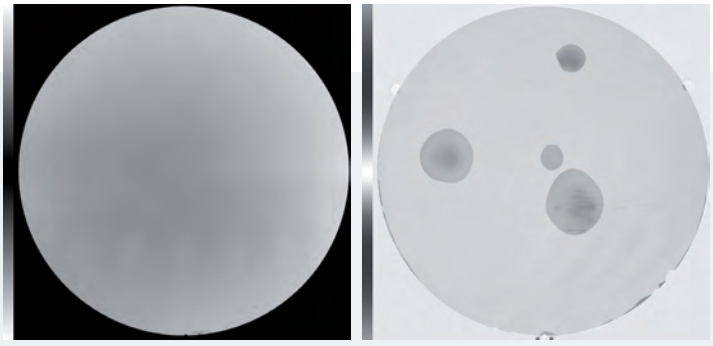


Figure 2. Edge conditioning (trimming) reduces wafer diameter after back grinding.[2]



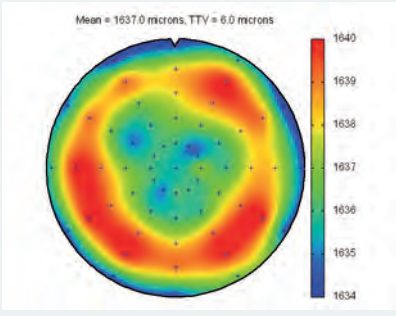
Example 1. Scanning Acoustic Microscope (SAM) scan of bonded wafers with and without voids.

The choice of carrier wafer also influences what inspection techniques can be used in subsequent process steps such as bonding. After the wafers have been bonded the bond quality needs to be confirmed. There are several options available including scanning acoustic microscopy (Example 1) or full field optical inspection such as the Spark system by Nanometrix. Since very small voids can potentially lead to delamination under high vacuum or during high temperature processing, the detection limit needed depends on the bond strength of the adhesive to the various substrate interfaces. There is a delicate balance between the need for strong enough adhesion to prevent bubbles from growing and weak enough adhesion to permit debonding at the end of processing.

After determining that you have a void free well bonded wafer to carrier pair, the last important item to check is the Total Thickness Variation (TTV) of your bonded pair. TTV control in the low single digit micron range is needed primarily for the final Thru Silicon Via reveal process. If there is a great deal of variation in thickness the high spots will be ground down too much and more importantly the low spots may not be ground down enough to expose the tops of the vias. Although some thickness variation can be overcome by sophisticated grinding equipment, it is best to bond the wafers with as little TTV as possible. To achieve the best bonding performance in terms of TTV control low TTV coating is considered by many to be important; however, newer bonding techniques don't necessarily require good post adhesive coat TTV to achieve good post bond TTV. Furthermore, TTV can be affected by post bond processing so caution must be taken depending upon the adhesive properties and the processes it is subjected to.[3]

Now that we understand what we are trying to achieve - a void free low TTV bonded pair - how do we go about getting it and what other factors need to be considered? First and foremost is adhesive selection. There are many types of adhesives available today and more in various stages of making their way onto the market. In terms of their primary function, bonding, there are three mainstream classifications: thermocompression, thermoset and photoset. As the name implies, thermocompression adhesives bond using heat and pressure; however, what differentiates them from other adhesives is their ability to "flow" or be reset by applying more heat or pressure. Thermoset adhesives, on the other hand, can use the same bonder as thermocompression adhesives, but once the adhesive is set it cannot be reworked - as the crosslinking/reactive groups have been activated and the process cannot be undone. Photoset adhesives are similar in that once the polymerization has occurred it cannot be reversed.

It is often very helpful to put together a matrix to sort out which adhesive(s) qualify on paper – such as cost vs. thermal stability[4]. Other notable qualities to be considered are; chemical resistance, vacuum stability, bonding speed, debond throughput, and final clean requirements. Thermal stability can be established with thermal gravimetric analysis (TGA) and thermal desorption spectroscopy (TDS). To what degree the adhesives need to be thermally stable is a function of the adhesion strength and process



Example 2. Typical TTV mapping result display format.

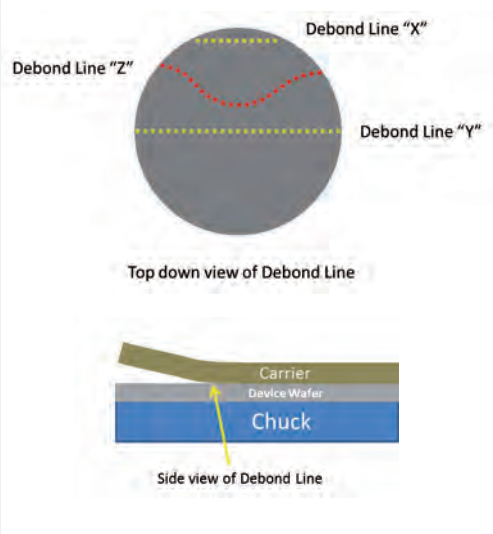
conditions. Some adhesives are very chemically inert, which is great for resisting chemical attack during photolitho or etch processes, but it also means that residue from these adhesives is very difficult to chemically rinse or dissolve away as is sometimes needed during the final cleaning process to ensure the device wafer's surface is clean enough for soldering or compression bonding - the next big processing challenge in fabricating both homogeneous and heterogeneous 3DIC's. However, some very chemically resistant adhesives make films that can be easily removed by peeling techniques and this could eliminate the need for costly and hazardous chemical stripping baths. As you can see careful thought and compromise is needed during the adhesive selection process.

Once the adhesive has been selected the bonding process and recipe need to be sorted out. Bonding is typically achieved with light, heat and pressure, singly or in combination. Anything that minimizes movement and stress on the wafers during bonding will help produce the best results. Let's examine why. First, in order to minimize void formation during bonding it is best to bond inside a vacuum chamber. Of course, the chamber does not provide a perfect vacuum and a small amount of gas could be trapped at the bond interface; however, current bond chambers are able to pump down enough to reduce the voids to below detection levels of the metrology equipment. A side benefit to bonding in a vacuum is it also helps draw out any volatile solvents remaining in the adhesive films that could outgas and cause delamination in downstream processing. The bond chamber also has to keep the wafers centered and rotationally aligned (notch aligned) during the bonding process until the adhesive has set and can restrict movement. The difference between success and failure is a matter of a few microns or tenths of a degree of rotation.

The device and carrier wafers are now being held firmly in place inside the vacuum chamber ready for bonding. The best strategy for putting the two wafers together depends on the state of the adhesive – liquid, gel or solid. Certain adhesives require a significant amount of pressure to achieve good bond strength; whereas, others might squeeze out contaminating the chuck/bond chamber and possibly become bonded to the chuck – not very desirable in a high volume manufacturing environment since cleanup will stop everything. For this reason the bonding force needs to variable - from very low force for liquids to very high force for solids (pseudo solids). Another critical factor is CTE mismatch. Bonding usually takes place at a predetermined steady state temperature. However, for throughput reasons, the bonded pair is not extracted from the bond chamber at room temperature and the differences in CTE of the adhesive, device wafer and carrier wafer will all add stress to the bond while they are cooling. Furthermore, if the cooling process is not done in a controlled manner thermal gradients can also contribute to stress. These types of stresses can manifest themselves in bow, warp and increased TTV – all very undesirable. Temporary wafer bonding for the purposes of 3DIC manufacturing is very challenging and requires a significant amount of materials and equipment engineering to be successful.

As with bonding, the debonding method is largely dictated by the adhesive. Thermal slide debonding has been around for a while and utilizes thermo plastics that soften when heated. Unfortunately, heating is required for processing too so this method's utility is severely limited by thermal budget. Chemical dissolution is an almost stress free process, but it takes a considerable amount of time and requires the use of expensive perforated carriers and lots of solvent. Laser ablation to remove the carrier wafer has been successfully used in production, but prohibits the use of Silicon carrier wafers which are inexpensive and have perfectly matched CTE to

Silicon device wafers. The most recent innovation in separating the thinned bonded wafers from the carrier is room temperature mechanical lift off debonding. The reason this debonding technique is superior is most easily explained by looking at Example 3. By forming a straight debond line across the wafer you minimize the force needed for separation. The debond line length is directly proportional to the amount of force needed for debonding. By peeling the carrier from the device wafer utilizing a straight debond line you get the most efficient debond wave front and thus the least amount of force applied - regardless of the type of adhesive used for bonding. Furthermore, by securing the device wafer to a chuck using a film frame, and only applying force to the carrier wafer during the debond process, the delicate device wafer is subjected to the absolute least amount of stress during carrier separation and is left ready for transport to the final process.



Example 3. The debonding wave front lines "X" and "Y" (yellow dashed lines) are shortest possible. The debond wave line "Z" (red dashed line) represents a non-optimal uncontrolled debond line.

Once the carrier wafer has been removed the final requirement is to clean the device wafer surface that was exposed to the adhesive. Any residue remaining after debonding can interfere with downstream assembly processing such as soldering and thermal compression bonding. Since the wafer is very fragile at this point it needs to be supported and the best method is to use tape on film frame. Since cleaning solvents can also attack the supporting tapes it is important to protect the tape if solvents are used for final cleaning. Fortunately tape manufacturers are developing new tapes specifically for this application and special efforts to protect the tape may become obsolete.

Pressure to bring 3DIC's to market is building and temporary bonding is one of the key elements to enabling low cost high yielding process integration schemes. With the new class of room temperature mechanically lift off adhesives and the latest generation of lift off debonding equipment the path to high volume manufacturing of 3DIC's is well in sight. It won't be long now until these fabulously efficient high performance 3DIC packages are found in many of your favorite consumer electronic devices.

THE AUTHOR

Chris Rosenthal's 15 years of experience in the semiconductor industry range from test and burn-in sockets to extreme front-end photolithography.
His interest in 3DIC, temporary bonding/debonding in particular, started over 5 years ago and since then he has been actively pursuing a universal solution to the challenges associated with thin wafer processing and handling.

REFERENCES

[1] Dr. Gary R. Trott and Dr. Aric Shorey "Wafer Mechanical Properties: A Comparison To Silicon", 6th International Microsystems, Packaging, Assembly and Circuits Technology, 2011

[2] http://www.imec.be/ScientificReport/SR2009/HTML/1213307.html

[3] Tamura, K., Proceedings from 60th Electronic Components and Technology Conference, June 2010; Page(s): 1239 – 1244

[4] International SEMATECH 2009 Conference on 3D Packaging, Hitachi DuPont Microsystems, LLC, Page