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SUSS report

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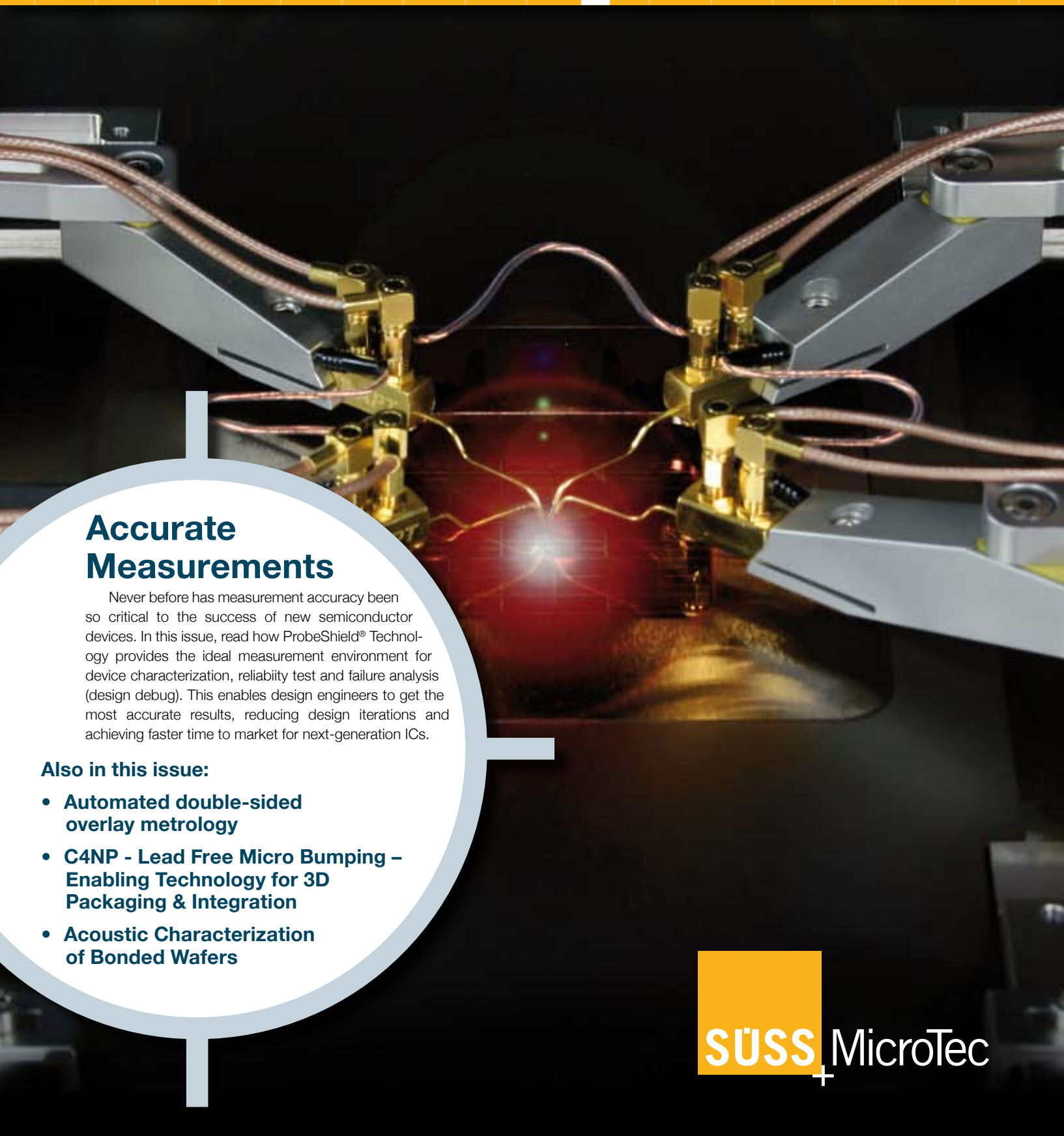

Accurate Measurements

Never before has measurement accuracy been so critical to the success of new semiconductor devices. In this issue, read how ProbeShield® Technology provides the ideal measurement environment for device characterization, reliabiity test and failure analysis (design debug). This enables design engineers to get the most accurate results, reducing design iterations and achieving faster time to market for next-generation ICs.

Also in this issue:

- **Automated double-sided overlay metrology**
- **C4NP - Lead Free Micro Bumping – Enabling Technology for 3D Packaging & Integration**
- **Acoustic Characterization of Bonded Wafers**

SÜSS MicroTec

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Full View

Advancing Moore's Law

With the holidays past and the wrapping paper on its way to the landfill we are now trying to figure out how to use the latest gadget we 'had to have' (my collection of electronic toys that I haven't figured out how to use is growing continuously).

The next wave of smaller, faster and better 'must have' toys will shortly be in our local stores. Whenever we think that we have reached a hard to beat level, a new functionality gets integrated. The mobile devices can now function as music player, camcorder, digital camera, video phone and yes, we can still use them to make phone calls.

One of the key enabling technologies for these outstanding capabilities is the proliferation of 3D technologies for stacking semiconductor devices. SUSS MicroTec equipment plays an enabling role in these revolutionary 3D processing technologies. With the focus of semiconductor volume and innovation shifting quickly to consumer applications we need to anticipate these market requirements to have equipment and processing technologies available for this fast paced market.

With a solid infrastructure for designing and manufacturing semiconductor equipment that meets world class standards we will particularly focus on process and equipment innovation. We see our responsibility in continuing to provide technology approaches that help to advance Moore's law.

There is little doubt that 3D technologies will be required to continue Moore's law over the next years.

Building on our well established lithography and wafer bonding equipment we will support the most stringent process demands for 3D packaging and 3D integration. With a renewed focus on product and process innovation we will set the pace for the 3D equipment industry.

The potential use of 3D stacking seems to have no boundaries. With image sensors for mobile phones driving the early adoption of 3D packaging we can already see this continue into memory stacking as well as a novel approach to manufacture CMOS image sensors using 3D technologies. Backside illuminated image and hybridized sensor arrays are leading us into very high density 3D integration.

We can never know exactly where the next wave of opportunity will be. What we can do is be ready to meet our customer requirements for equipment capability and deliver it with our well known quality of product and service to maximize the success of our customers. Your success is our success.

SUSS. Our Solutions Set Standards.

Wilfried Bair
Vice President Strategic Business Development

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Automated double-sided overlay metrology

Keith A. Cooper and **Thomas Huelsmann,** SUSS MicroTec

The growth of MEMS devices and other technologies using double-sided patterning has led to a maturing of MEMS manufacturing processes. Along with such techniques as deep silicon etch and release of mechanical structures, MEMS devices have likewise taken novel lithography processes to a new level of maturity and broad use. Patterning of very thick photoresist layers, etching of hundreds of microns of silicon, and double-sided lithography – techniques with only limited application a few years ago – have now been brought into the mainstream for MEMS process flows.

As these techniques become more commonplace, the equipment set to perform these process steps must also grow and evolve. Demand for new MEMS device features as well as greater functionality within existing devices has fueled a demand for more efficient use of wafer real estate on the front and backside of the wafer. Device layouts may require frontside to backside overlay of 1µm; this trend toward smaller feature sizes and tighter front-back registration has driven a need for tighter registration of frontside to backside features, as well as a need for overlay metrology tools. And as backside patterning moves toward greater production volumes, so also must the backside metrology tools provide automated measurement for production scenarios. The concept of double-sided patterning is not new – it has been present in the process flow of MEMS and communication devices for many years. Si pressure sensors, GaAs telecom chips, InP lasers, and many other such devices have utilized the backside of the wafer, either for device functionality or due to cost pressures to capture and utilize otherwise wasted substrate real estate.

The earlier uses of backside lithography employed viewing systems with infrared (IR) illumination; the proper choice of IR illumination source coupled with an IR-sensitive camera yielded sufficient clarity in the image to perform alignments of frontside to backside features on many materials included GaAs, InP and in some cases Si. But not all substrates yielded a reasonable image to align, particularly metallized circuits, Si substrates with high B-doping levels, or other inherently IR-opaque materials such as Al203. Due to this material opacity problem and the need to perform tighter front-back alignments for smaller features, savvy equipment suppliers designed imaging systems which employ image-capturing software so that back and front of substrate can be viewed simultaneously even with highly opaque materials. Despite the ease of use and therefore popularity of this

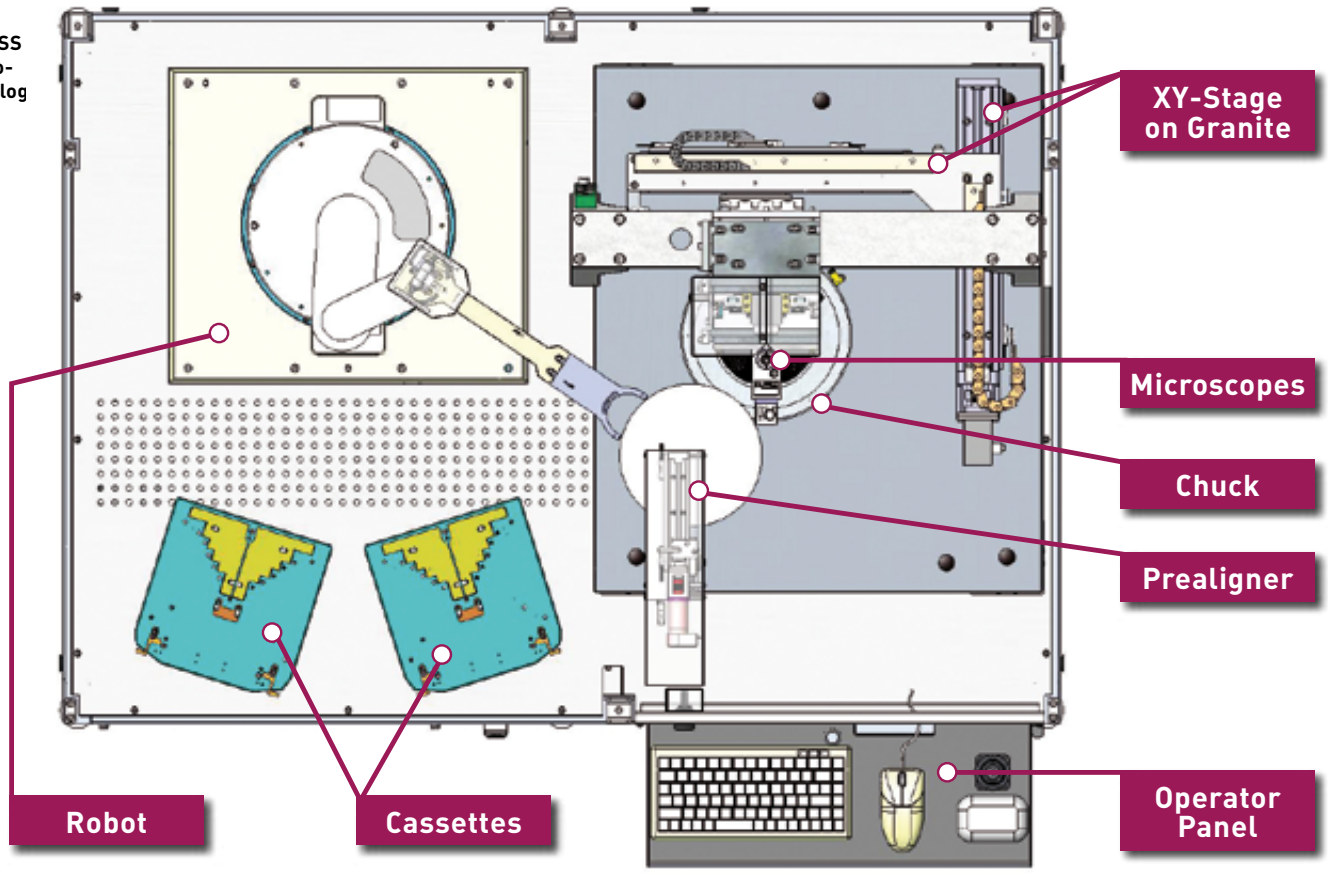


Figure 1: Layout of SUSS DSM200 Automated Metrolog Tool

Figure 2:
View of tool with robotic handling, cassettes and non-contact prealigner

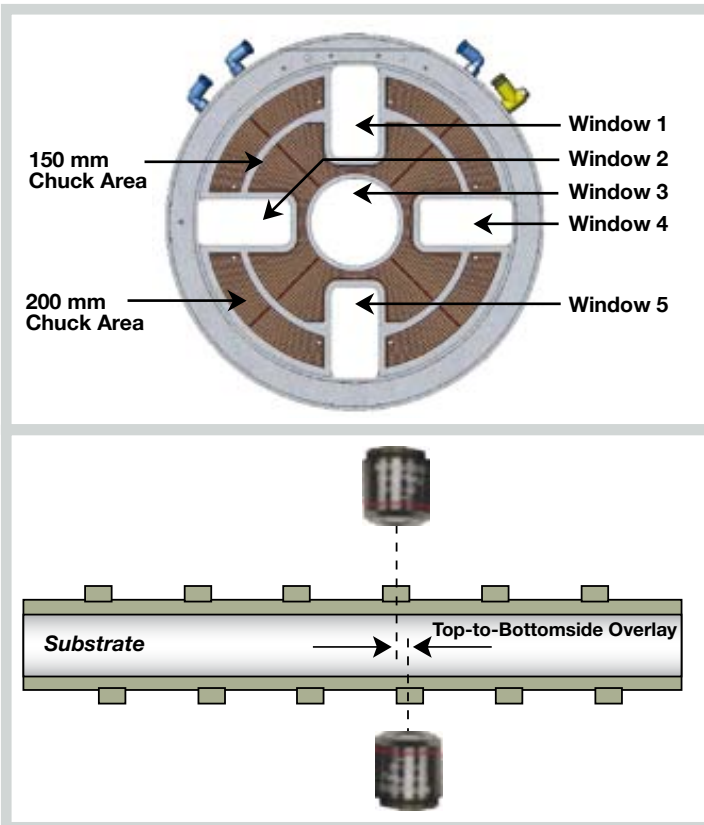


Figure 3:
Typical Layout of 150mm wafer Chuck

double-sided alignment technique, IR is still valuable for buried circuit layers and other device layouts and is used for those process schemes.

Many of these MEMS or optoelectronic devices have undergone the customary shrinkage of geometries in order to make the circuits smaller, faster or more cost-competitive. With this reduction in feature size comes the requisite tightening of alignment tolerance for front-front or front-back overlay. This progression is only natural as the devices become more mature or as the cost of such circuits is reduced in an effort to create broader market appeal. In their 2006 Global MEMS newsletter, Yole Developpement has projected a 13% CAGR across many MEMS devices, with many of these requiring backside patterning and the corresponding front-to-backside metrology steps.

But as the market for such devices grows and the production volumes ramp significantly, so does the need to automate the process and metrology steps to keep the cost of ownership (COO) in line with market demand. There is a clear and present need to provide automated metrology systems which will provide process control for these processes requiring backside alignment. The requirements of such a tool would include:

- hands-off metrology on various sized wafers up to 8".
- Robotic handling to process various sized, often fragile, substrates with high throughput
- Access to multiple arbitrary measurement locations for process and metrology flexibility
- Repeatability, reproducibility, and accuracy
- Diagnostics / Factory Automation: auto-calibration, auto-diagnostics, SECS/GEM interface

Figure 1 shows a block diagram in plan view of a tool designed to meet these requirements. With a granite base for machine stability and a flat reference surface, the tool incorporates an XY translation stage mounted atop the granite so that all motions are carried out with minimal friction. This granite has been polished to a total surface finish of 2µm over its entire surface to minimize or eliminate the need for re-focusing between measurement sites.

A field-proven robotic handling system with a non-contact prealigner (Figure 2) also provides a fast and easy method to change wafer sizes or materials without any mechanical change-over of prealigner or robot end-effector. Since the tool operates completely in a hands-off mode, it can measure and report frontside to backside metrology results at a throughput of 50 wafers/hour, and the results are completely independent of the operator. Edge handling is also available for those applications where exclusion areas on the wafer dictate a certain rim of handling area. This feature is especially attractive for MEMS or optolelectronic applications where the optical and mechanical functional-

Figure 4:
Layout of vertically superimposing microscope for fiducial measurement

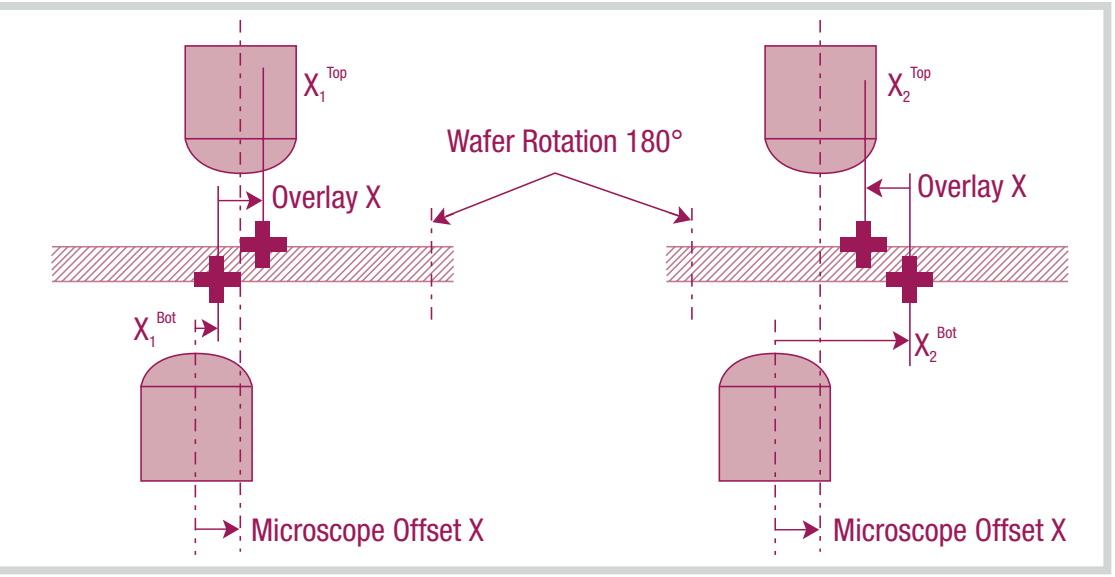


Figure 5:
The DSM Principle of Operation

ity of the features is particularly susceptible to damage from handling. To accommodate an advanced production scenario incorporating factory automation, SEC/GEM interface, RF ID reader for the cassettes and wafer ID reader are all available.

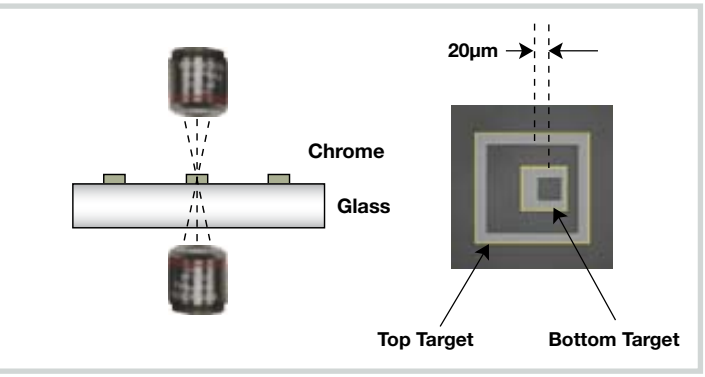


Figure 6:
Measuring the top-to-bottom "overlay" of a transparent substrate to quantify the tool accuracy

To provide freedom and flexibility in choosing the overlay verification sites, the chuck has large viewing areas with unobstructed access to the top and bottom sides of the wafer. (See Figure 3) This ensures not only that features critical to the device's performance will be visible, but also that there is no optical shift and ensuing overlay offset in the measurement process created by any uncharacterized optical aberrations in the chuck material. More than 4000mm2 on a 6" SEMI wafer is available for viewing.

The measurement of the top-bottom overlay is carried out by a vertical superimposed microscope, depicted in Figure 4. The measurement technique is to simultaneously view the top and bottom fiducial images with CCD cameras, then determine the relative position or these two targets using a pattern recognition algorithm based on the Cognex Patmax software. Typical fiducials for the overlay metrology tool are the same as those used for preceding lithographic alignment; targets may be between 30 and 300µm, and are most typically about 100µm in X and Y. The Cognex system utilizes a very durable and field-proven software platform so that the system is impervious to variations in contrast, rotation of the images, and even reversal of the image tone.

After determining top-bottom overlay at this first site, the alignment stage is automatically moved to position the alignment fiducials for each of the desired locations into the field of view of the cameras and the process repeats.

One main challenge in precisely measuring the alignment accuracy of structures on the top and bottom side of the wafer lies in several mechanical imperfections that occur during operation, like the offset between the optical axis of the microscope. In order to maintain control of these deviations each time a wafer is measured, the DSM200 rotates the substrate automatically by 180° at the end of the first measurement cycle, as depicted in Figure 5. In this way errors such as misalignment in the optical axis of the microscopes can be eliminated so the final result is accurate and trustworthy for all measurement sites. The final overlay between the top and bottom target is calculated by the formula below.

$$Overlay\ X = \frac{1}{2}\cdot[(x_1^{Top} - x_2^{Top}) - (x_1^{Bot} - x_2^{Bot})]$$

$$Overlay\ Y = \frac{1}{2}\cdot[(y_1^{Top} - y_2^{Top}) - (y_1^{Bot} - y_2^{Bot})]$$

For any metrology tool to be effective, it must deliver consistent results as measured by repeatability and accuracy. To measure repeatability, a Si wafer was printed on a double-sided lithography tool from SUSS MicroTec, followed by developing of the resist features to create optically visible lithographic features. After development of the resist, the patterned wafer was loaded into cassettes and measured in the DSM200 tool as described above.

Detection repeatability can be quantified by loading a sample into the measurement tool, recording the indicated overlay repeatedly, then performing statistical analysis of the output data. Detection repeatability can be explored further by unloading and loading the same sample multiple iterations, measuring the overlay each time and analyzing the data for evidence of drift or fluctuation.

Potential sources for detection repeatability error would include mechanical drift in the stages for wafer chucking or objective/camera mounts, uncertainties in the position detection algorithm, vibration in the tool, and thermal drift. Any one of these sources can contribute significant error which would disqualify the tool for its intended use, and must be carefully considered from a system-level point of view from the ground up when designing the tool.

Measurement accuracy for the tool was quantified by means of measuring a transparent substrate with very thin patterns of Cr on one side, similar to a lithographic photomask. A quartz substrate, 1mm thick, with optical transparency and consistency parallel to photomasks was patterned with a laser writer, then the patterned features were transferred into the underlying Cr layer by means of dry etching. The overlay of these Cr images can be measured by a benchmark topside-topside me-

trology tool such as the Vistec LMS. Then this wafer was measured on the SUSS DSM200 by using the top side microscope to look at one top side feature while the bottom side microscope looks also at the same feature (for an anticipated 0µm overlay) or an adjacent top side feature (for an anticipated 20µm overlay), as shown in Figure 6.

For any metrology to meet the measurement requirements, it needs to deliver a very tight grouping of overlay readings, indicating a very high detection repeatability. Results from the tests described above for the DSM200 are depicted in Figure 7, with 2000 total measurement cycles at multiple sites. The data indicate 0.035µm for the X direction and 0.067µm for the Y direction, both at 3 sigma, indicating that the tool does supply the requisite detection repeatability for a front-back overlay requirement of 1µm or better.

Even if a metrology tool can repeatedly detect the apparent overlay error between 2 features, this information is nearly useless unless there is likewise a correlation between the metrology tool's results and some external measurement standard. Results from the accuracy tests using the transparent substrate with Cr features are plotted in Figure 8 and show a mean + 3 sigma value less than or equal to 0.15µm, well within the range of performance required for current or coming generations of devices requiring front-to-backside overlay.

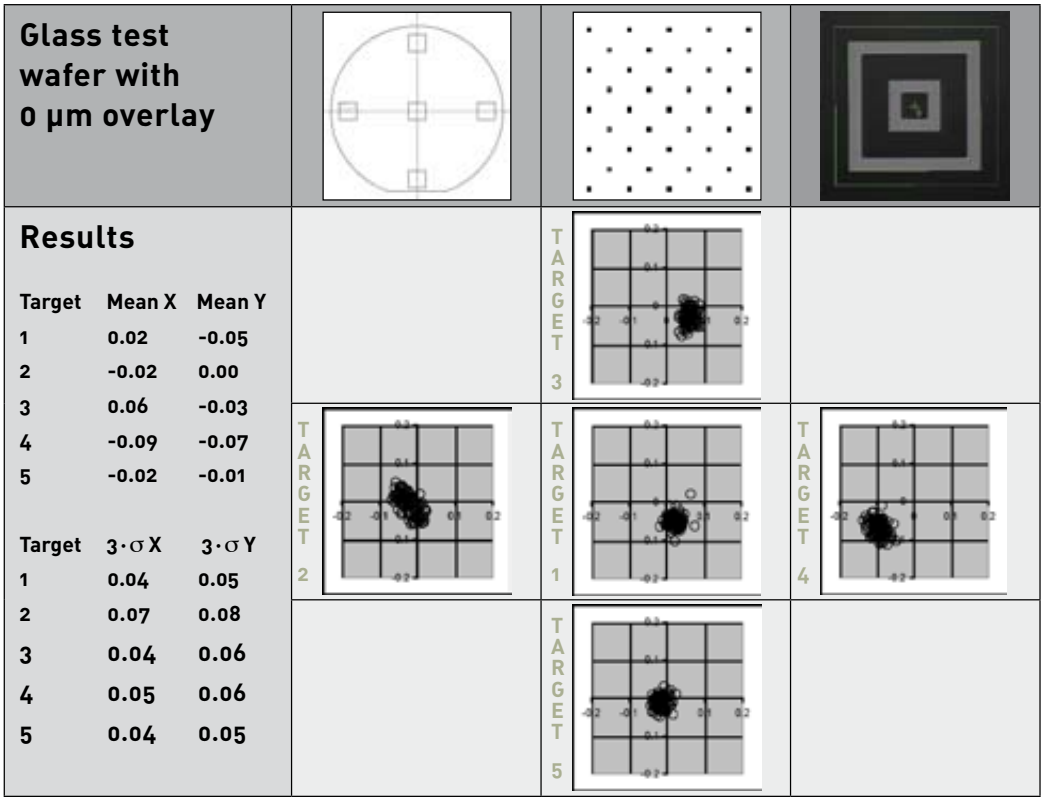
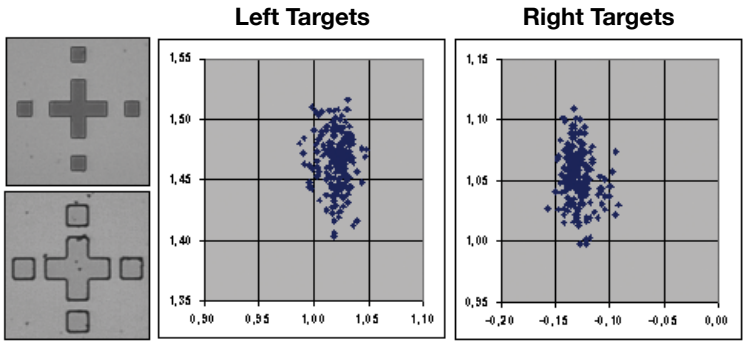


Figure 8:
Verification of DSM200 overlay data against external standard

CONCLUSION

A growing demand for high quality frontside to backside lithography processes has likewise generated a need for an accurate, automated tool to quantify the overlay for such processes. Operating in a cassette-cassette mode for high throughput, such a tool has been designed and qualified to provide overlay metrology for technologies such as MEMS, 3D Integration, and other devices with front to back registration requirements down to 1µm or tighter.



	Offset	Offset	
Mean Value X	1,021	-0,129	µm
Mean Value Y	1,465	1,054	µm
3 * Std. Dev. X	0,032	0,033	µm
3 * Std. Dev. X	0,067	0,064	µm

Figure 7:
Detection Repeatability for 2000 measurement cycles

KEITH COOPER

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THOMAS HUELSMANN

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Accurate Measurements

Joshua Preston,
Marketing Group Manager, SUSS MicroTec

Semiconductor device manufacturers face a challenging marketplace; consumers demand higher performance, better reliability and lower prices for their electronic devices. To meet this challenge, new technologies are being developed using advanced and/or hybrid designs, new materials and innovative manufacturing processes. To realize a return on the investment in these technologies, device manufacturers must keep yield high and time to market short.

One area in which significant gains in efficiency can be realized is in the device characterization process. In this process, it is necessary that accurate measurements are obtained quickly because the manufacturer benefits from more efficient model extraction, faster model turnaround and fewer design iterations, reduced time to market and ultimately a higher return on investment.

The device characterization process is critical for developing a well-designed component, but it is becoming increasingly more complex. The driver behind this is, as mentioned, the higher performance, better reliability and lower cost demanded by the end user, which results in devices that require challenging measurement setups to extract accurate parameters that are needed to verify the device model. It is not uncommon today that a measurement takes several hours (or even days) to set up. Additionally, the accuracy of the measurement cannot be stressed enough. Test engineers need to have full confidence in their results: they must be repeatable, understandable and most importantly real and true. If the results are flawed, then the models and devices will be flawed as well, which necessitates another iteration of the entire process. This is further complicated by communication delays that result from the fact that device characterization is commonly done in a different location because it is in a different department or has been outsourced to a test house, both of which may be in another country.

To meet these challenges, test system manufacturers must provide test engineers with the tools necessary for accurate, efficient device characterization. This must be a holistic approach and starts with the wafer probe system, as the platform for the wafer-level measurements, and includes probes, cables and of course the measurement equipment. The ideal test system maximizes measurement accuracy, positioning accuracy and what I will call “human accuracy”, that is, the ergonomics and usability of the system. This article will focus on the improvements that can be made in these three areas and give concrete examples of how the device characterization process can be improved, thus increasing the return on investment in new devices.

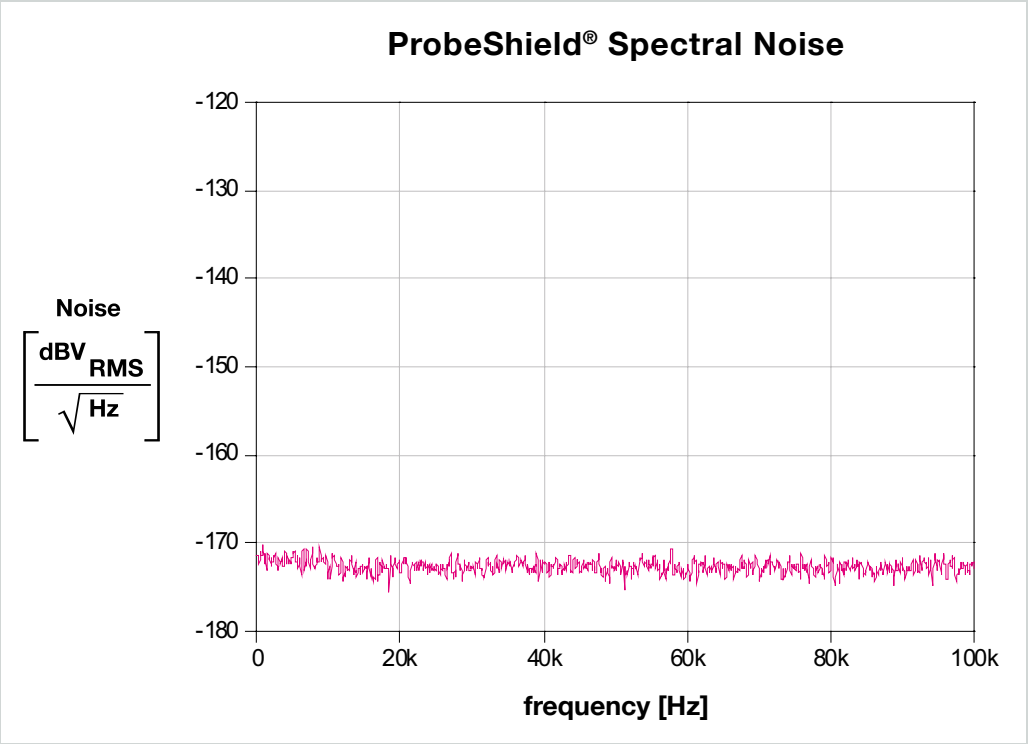
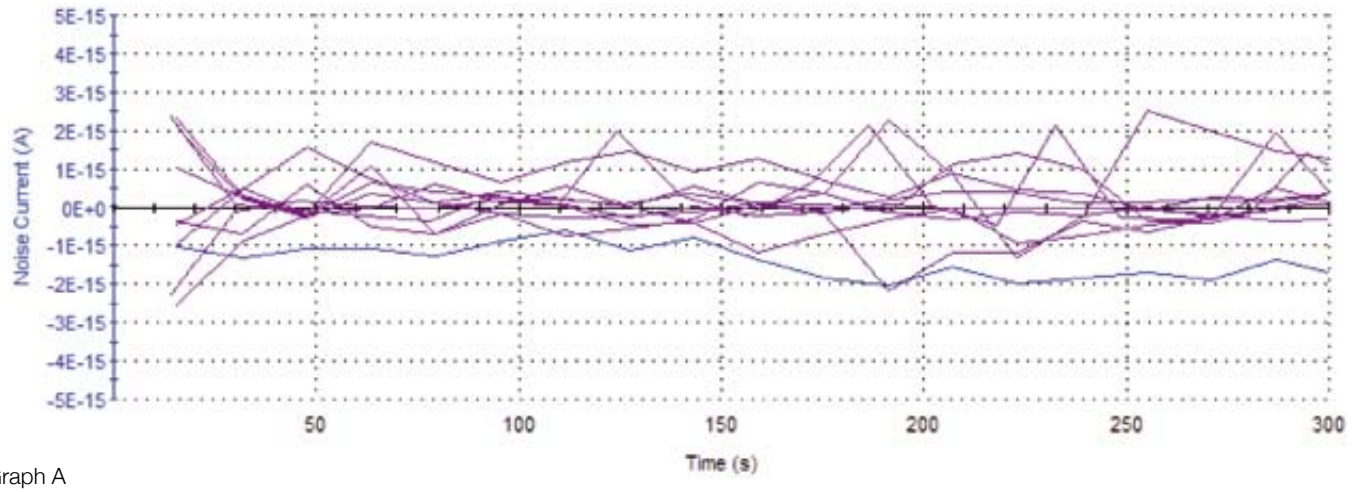


Figure 1:
Since small signals from the DUT need to be measured with high accuracy, the probe system must provide an environment free from EMI/RFI and light. Shown here is the spectral noise floor measured inside the ProbeShield system from SUSS MicroTec. By keeping the noise to an absolute minimum, it is possible to achieve highly accurate parameter measurements.

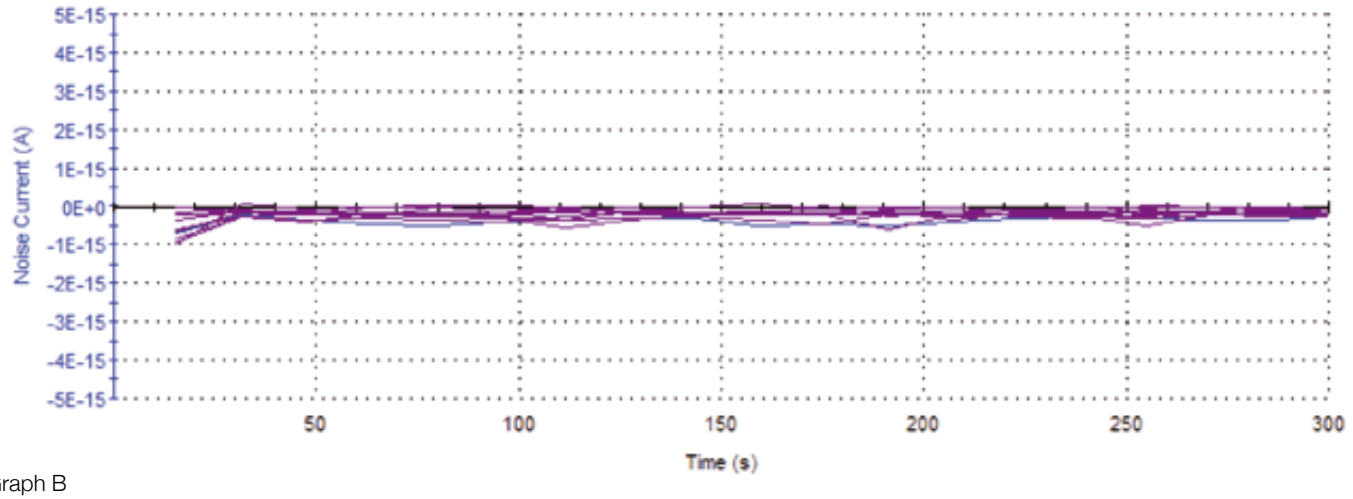
Measurement Accuracy

At the basis of any device characterization and reliability test process is the accurate measurement of parameters from the device under test (DUT). These parameters include measurements of current-voltage (I-V), capacitance-volt-age (C-V), low-frequency (1/f) flicker noise, HF noise and scattering (S-) parameters, and are highly sensitive to interference from external sources of noise. Therefore, the most basic requirement for accurate parameter measurements is a test system featuring a shield based on sound electromagnetic design principles, such as ProbeShield® Technology from SUSS MicroTec, to prevent unwanted EMI and RFI as well as light from influencing measurements. This is especially critical when sensitive measurements must be taken, and if implemented properly, the noise floor is kept low and results are more accurate (see Figure 1).

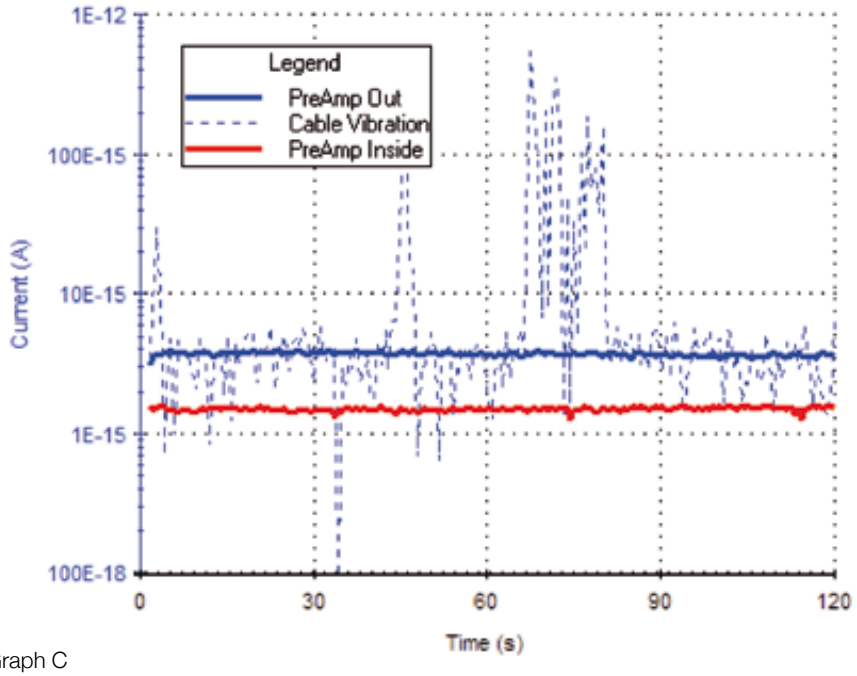
A well-designed EMI/RFI shield also allows measurement equipment to be integrated into the shielded environment of the system. For very sensitive measurements, elements like signal pre-amplifiers are used to capture the signal and amplify it before transmitting it to the main measurement unit such as a parameter analyzer. When these elements are placed inside the shield, the EMI/RFI and motion-sensitive elements like triaxial cables are kept in a protected environment and any exterior signals are kept from interfering with the equipment. A simple experiment as shown in Figure 2 confirms the benefit of measurement equipment integration. Furthermore, additional shielded rooms are no longer necessary if the equipment is integrated into the shielding of the test system. This reduces capital outlay and the overall cost required for test processes.



Graph A



Graph B



Graph C

Figure 2:
In this experiment, Keithley preamplifiers were used to measure very-low-signals from the DUT. In Graph A, the preamplifier was placed outside the shielded measurement system, resulting in poor measurement repeatability for each of the ten measurements taken. In Graph B, the same measurement was done another ten times with the preamplifier inside the shielded measurement system. Graph C demonstrates how any slight disturbance of the sensitive cables connecting the pre-amplifier to the probes can affect the measurement results. When placed inside the shielding, the sensitive cables cannot be disturbed and only the high-power cables running from pre-amplifier to measurement instrument are exposed.

Integrating elements of the measurement setup inside the shielded environment has another major advantage. Cable lengths, obvious limitations in measurement accuracy, can be minimized. Shorter cables ensure a better measurement dynamic range and thus more accurate measurements. When all of these issues are taken into account, an optimal environment is created for extracting the most accurate measurements from the DUT.

Measurement integration also means that suppliers of the various elements of the device characterization system work together to ensure that the entire system provides value to the user. That is, the system should not just be a mixture of measurement equipment, probe station, probes and cables. Each piece must be correctly integrated and tuned to operate seamlessly with the other elements in the system. As such, a system with various elements that are simply thrown together runs the risk of operating inefficiently and driving up the cost of test to a point where it no longer provides value to the user.

Positioning Accuracy

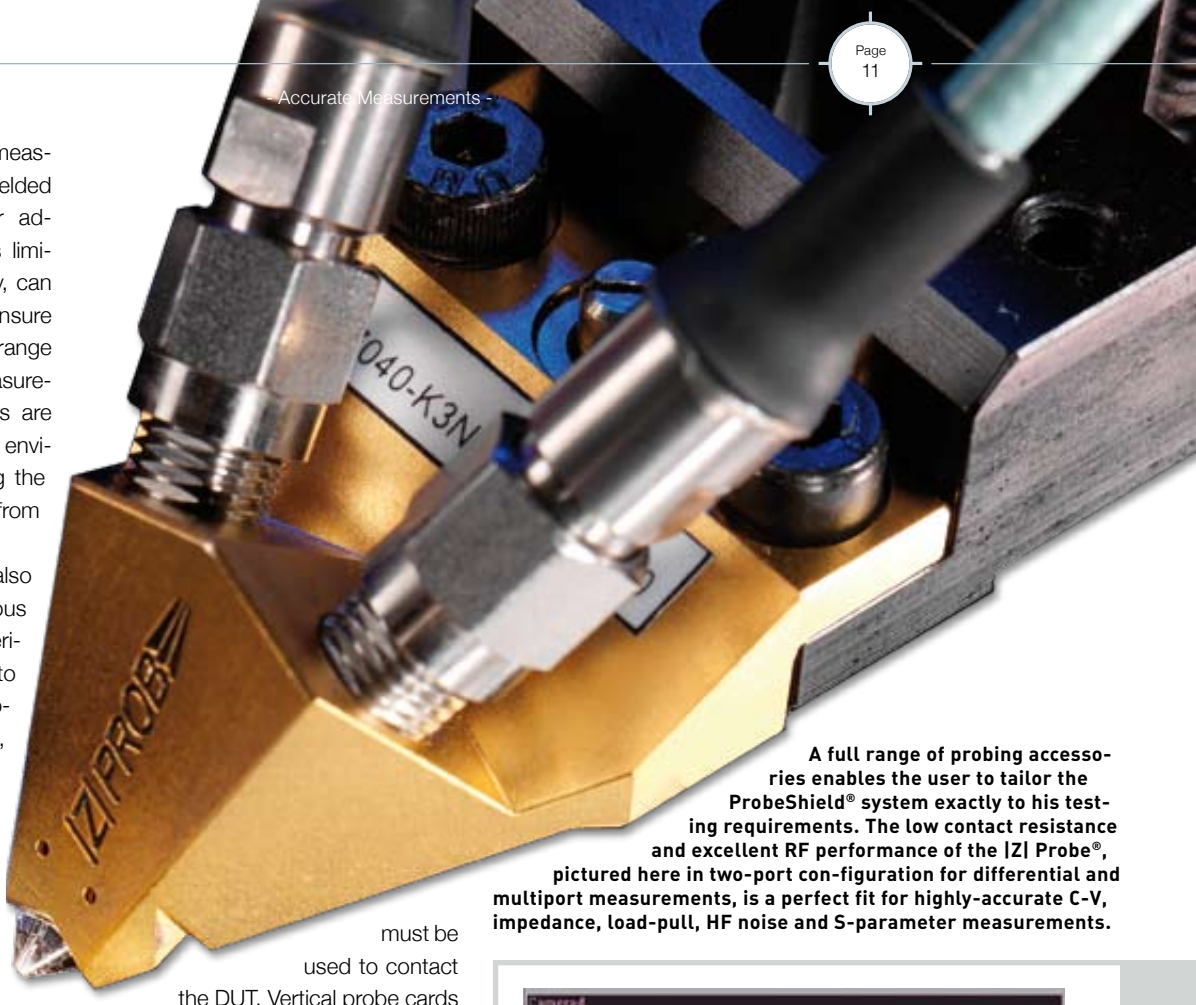
The need for a faster feedback loop in the manufacturing process and faster classification of process improvements has increased the importance of wafer-level reliability. As a result, contact pads for reliability test are moving into the wafer kerfs alongside the pads used for device charac-terization. To accommodate all these pads, their size as well as the space between them, the pitch, is shrinking. Contacting small pads, sometimes as small as 40 x 40µm, is already an issue for some device manufacturers and will become more pronounced in the near future. If stable, repeatable contact is not achieved, measurement results are compromised and time is wasted running test procedures over and over again.

As pads get smaller and more numerous and advanced packaging technologies like wafer bumping become ubiquitous, vertical probe cards must be used to contact the DUT. Vertical probe cards cannot be aligned like a traditional cantilever probe card because there is no viewing port for probe-to-pad alignment. To solve this challenge, probe station manufacturers have developed technologies that assist the operator in aligning probe cards to the pads. SUSS MicroTec's MicroAlign™ Technology, for example, automates the probe-to-pad alignment process by using a selfcorrelating camera system and a unique software package. The process of aligning the probe card to the pads takes less than five minutes, after which test routines can be run.

Since many vertical probe cards have thousands of contact tips and can exert an extreme amount of force, the chuck stage must be able to handle such extreme forces. A well-designed stage minimizes deflection and therefore increases contact stability and repeatability while reducing damage done to wafers and probe cards.

Human Accuracy

The high rate of turnover of operators and technicians in the semiconductor industry is a significant cost to manufacturers, especially as measure-



A full range of probing accessories enables the user to tailor the ProbeShield® system exactly to his testing requirements. The low contact resistance and excellent RF performance of the |Z| Probe®, pictured here in two-port con-figuration for differential and multiport measurements, is a perfect fit for highly-accurate C-V, impedance, load-pull, HF noise and S-parameter measurements.

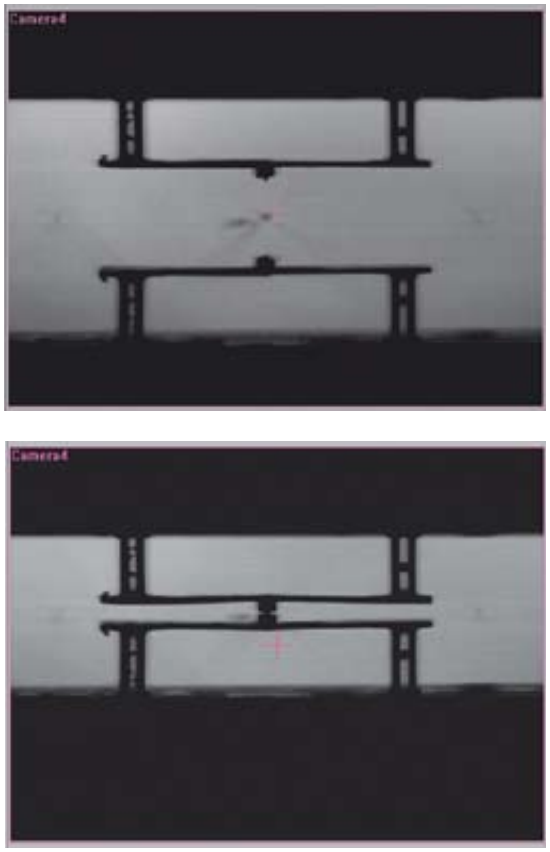


Figure 3:
The ContactView system is used to assist operators in setting contact between the probe card and the wafer. Shown here is a FormFactor vertical probe card at separation and in contact. The mirrored image at the bottom of the picture is the probe card's reflection on the surface of the wafer

ment setups, tasks and equipment become more complicated. A test system with a highly ergonomic, safe and intelligent design provides the optimum the learning curve for new operators and technicians. An easy-to-use, intelligent system also helps safeguard investments made in measurement equipment, probe cards and wafers.

An example of an innovative new safeguard in wafer probe systems is SUSS' patented ContactView™ system. This is an integrated, side-looking camera that provides an additional dimension for viewing the wafer and probe tips as they approach each other; an example is shown in Figure 3. This assists the operator in safely setting contact and prevents damage to probe cards and wafers.

Increasing the automation in the test system also improves human accuracy. Automated systems take the guesswork out of operation as well as assisting the operator in carrying out tasks. In addition, the system can be kept running overnight and on weekends without the need for human intervention. An example of such a system is SUSS' unique ReAlign™ Technology, which automatically compensates for thermal drift after temperature change. Most test routines are run at various temperatures, presenting a significant challenge to the operator because she must adjust the alignment of the probe tips to the pads after each change in temperature to accommodate for thermal drift. ReAlign Technology automates this process based on the alignment algorithms from the MicroAlign system. The process requires no operator intervention and can be called from the test executive, which means lengthy tests at several different temperatures can be run overnight or on the weekends.

Soft Assistance

Of course, the accompanying software is also a means by which the human accuracy of a system can be enhanced. There are several software tools available today that help users configure wafer-level calibration for RF and microwave test systems as well as tools to find the correct test frequency when using S-parameter measurements to characterize gate oxides. Simple-to-use software, when designed properly, guides operators through the setup and provides a system of checks to ensure that the calibration and test routines run safely. The software can also alert the operator or text executive when a recalibration or re-alignment is necessary. This is a considerable productiv-ity improvement since the time needed to setup and run the routines is significantly reduced when compared to manual, unassisted setup. Furthermore, there are software tools available that support test engineers a-round the world when working to develop new technologies. A typical example is when the team in Laboratory A measures the DUT and obtains a result that is different than the team in Laboratory B. SussCert™ software, for example, generates confidence intervals to allow these teams to quickly judge the performance of the measurement system and easily compare results.

The high rate of turnover of operators and technicians in the semiconductor industry is a significant cost to manufacturers, especially as measurement setups, tasks and equipment become more complicated

Conclusion

It can clearly be shown that there are significant gains to be realized from enhancing the device characterization process. Maximizing measurement accuracy by using a well-designed probe system with an advanced EMI/RFI shield results in the benefits of faster model turnaround and fewer design iterations, both of which are preconditions for reducing time to market and higher return on investment. The system also needs to be able to keep up with the trends of shrinking pad-sizes and new technologies such as high-pin-count vertical probe cards by providing precise positioning accuracy. And of course, the entire system must be designed with the human interface in mind. A strong focus on enhanced human accuracy increases the return on training investments and leads to gains in productivity. In addition, the use of intelligent hardware and software systems is the enabler for unattended test routines for automated generation of modeling and reliability data. Altogether, a well-designed and integrated device characterization system helps test engineers add value to the semiconductor design and manufacturing process by overcoming current and new challenges with the highest accuracy.

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Joshua, originally from the USA, holds an M.B.A. degree from the Handelshochschule Leipzig (Leipzig Graduate School of Management) and a B.S. in Economics from the University of Idaho.

C4NP

Lead Free Micro Bumping – Enabling Technology for 3D Packaging & Integration

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ABSTRACT

Technology roadmaps for electronic packaging and 3D integration show the continuing trend of increasing input/output connection density between the semiconductor chip and the package or between two different IC's. For FlipChip packaging applications, 150µm pitch full grid solder bump arrays have already entered production. Bump pitch requirements for 3D applications such as the integration of memory and logic are even tighter. These fine pitch applications exceed the capabilities of traditional wafer bumping processes such as solder screening or ball placement. Controlled Collapse Chip Connection – New Process (C4NP) technology has the ability to produce these very fine pitch connections in a cost effective manner.

This paper reviews the latest C4NP data for a 50µm pitch application. Glass molds were fabricated, filled with solder, inspected, and the solder transferred to a fine pitch wafer. Four molds have been fabricated with cavity top diameters ranging from ~33 to 40µm. The molds were filled with binary SnAg solder using the mold fill tool, automatically inspected with the mold inspect tool, and wafers were bumped with the solder transfer tool. Characterization of the filled molds and bumped wafers is presented.

In addition, the paper also reviews production cost analysis for various UBM stackups and solder bump processes, based on a specifically developed cost model. The Electroless Ni Immersion Au (ENIG) UBM structures in combination with C4NP solder bumping provide a significant cost reduction over alternative structures.

C4NP is a unique solder bumping technology developed by IBM which addresses the limitations of existing bumping technologies by enabling low-cost, fine pitch bumping using a variety of lead-free solder alloys. It is a solder transfer technology where molten solder is injected into pre-fabricated and reusable glass molds.

The glass mold contains etched cavities which mirror the bump pattern on the wafer. The filled mold is inspected prior to solder transfer to the wafer to ensure high final yields. Filled mold and wafer are brought into close proximity/soft contact at reflow temperature and solder bumps are transferred onto the entire 300mm (or smaller) wafer in a single process step without the complexities associated with liquid flux. C4NP technology is capable of fine pitch bumping while offering the same alloy selection flexibility as solder paste printing. The simplicity of the process makes it a low cost, high yield and fast cycle time solution for both, fine-pitch as well as chip scale package bumping applications.

Fine pitch C4NP molds were fabricated by ULCOAT, Japan. Mold fill, inspect and solder transfer was done using the C4NP process at the IBM Hudson Valley Research Park, Hopewell Junction, New York, United States.

C4NP MICROBUMP MOLDS

C4NP molds are formed using borofloat glass plates, which have a coefficient of thermal expansion (CTE) close to silicon wafers. Photolithography is used to pattern and etch the cavities into the 13" x 14" glass plate. The cavity diameter and depth precisely determine the volume of the solder bump, the cavity arrangement on the mold correspond to the bump pitch and bump location on the wafer. Figure 1 shows a SEM photograph of a generic glass mold with etched cavities.

For this work, the micro-bumping target pitch was 50µm. The molds have been manufactured by ULCOAT in Japan. ULCOAT is a qualified supplier of C4NP molds. Their standard and proprietary manufacturing process was used to make 4 different molds.

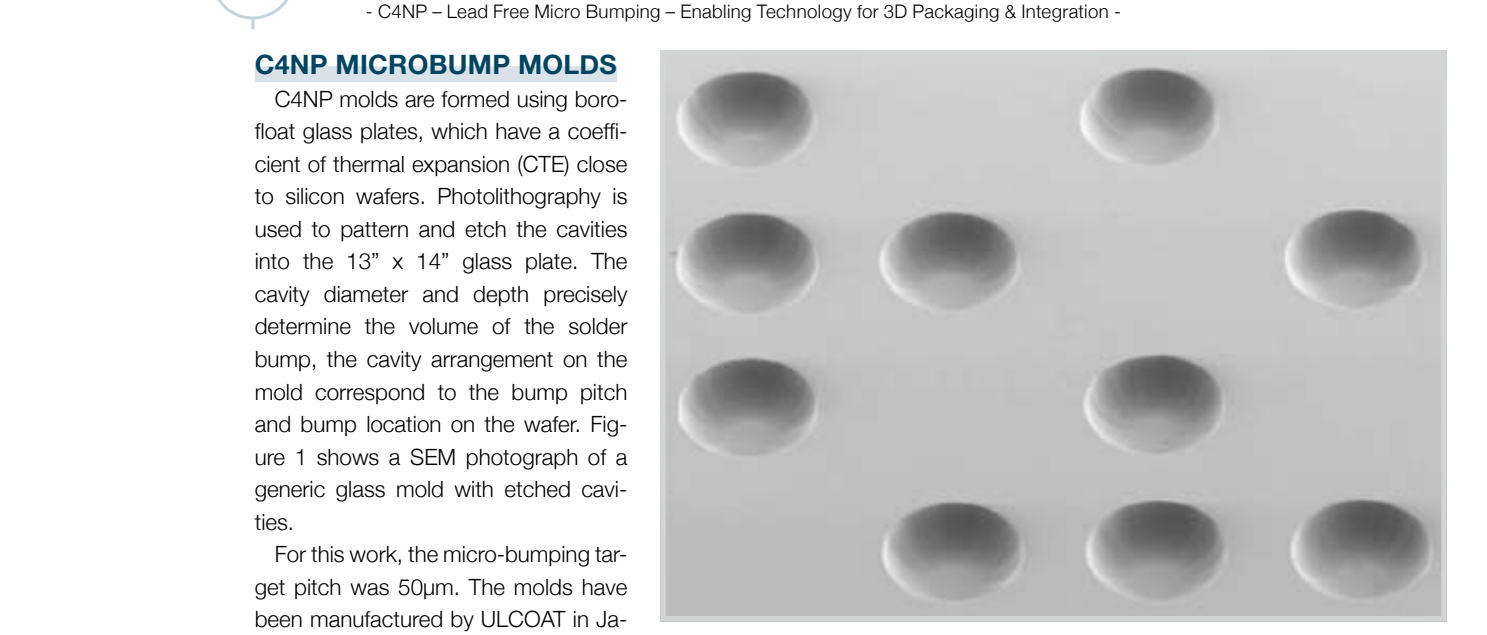

Figure 1:
Generic C4NP Glass Mold with etched cavities

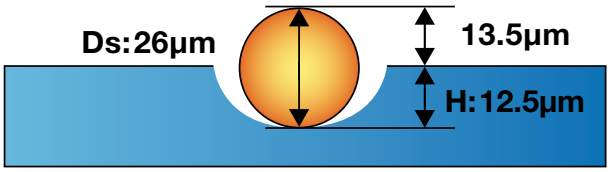

Figure 2:
Solder standoff after reflow in cavity

Unlike molds for traditional flip-chip bumping applications with typical bump pitches of 150µm or above, micro-bump molds have much tighter flatness requirements. The various mold flatness issues are illustrated in Figure 3. It is critical that the solder standoff during transfer is higher than the overall mold flatness as illustrated in Figure 2.

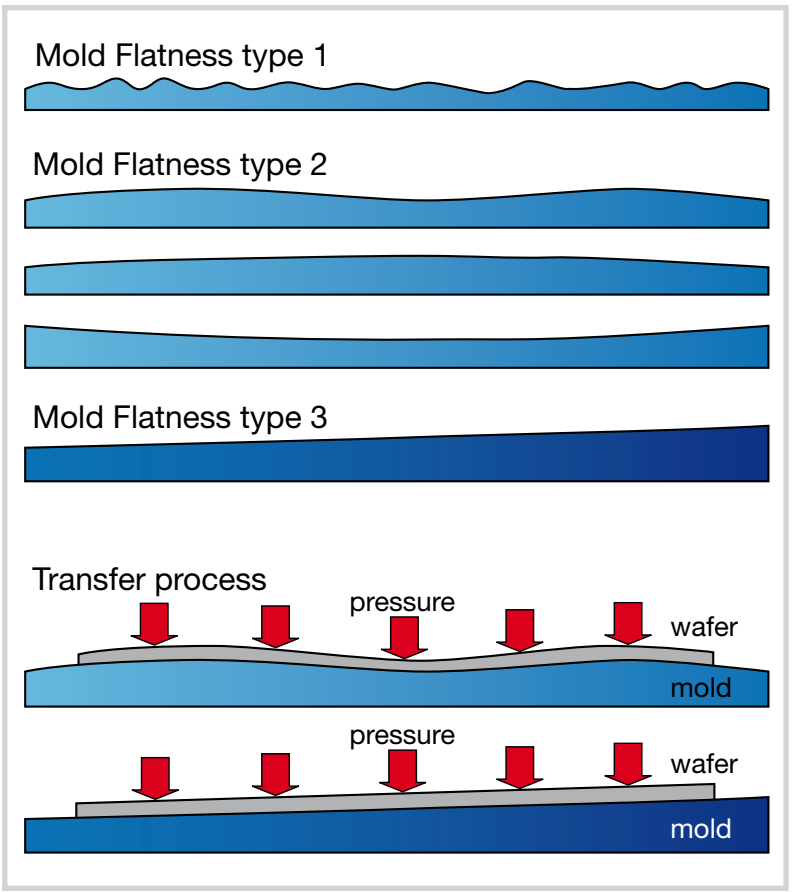

Figure 3:
C4NP Mold flatness concerns

Three different types of mold flatness issues have been identified:
Type 1 - Waviness (short wavelength);
Type 2 - Waviness (long wavelength);
Type 3 - Slope / Wedge. The most common flatness issue found on C4NP molds are Type 2 - Waviness (long wavelength). The unique design of the C4NP solder transfer chuck in combination with the properties of the glass molds allows good compensation of Type 2 and Type 3 flatness issues. However, Type 1 flatness issues are difficult to compensate for.

The glass plates for these molds have been specifically selected to meet the stringent flatness requirements. The molds were measured and inspected prior to the mold-fill process step.

The measurements as listed in Figure 4 show that the first three molds (ID 7731Z006 - 7731Z008) are similar in cavity depths. The cavities in Mold ID 7731Z009 are significantly shallower. Depth measurments on molds are particularly difficult and are not 100% accurate. The volume calculation as shown is based on a constant depth assumption. The data was collected by sampling a 10% area of the mold in an S-shape pattern across its surface. The cavity diameter uniformity of the micro-bump molds used in this experiment is shown in the following figures. The size of the circle illustrates the deviation from the mean diameter. A blue circle indicates a cavity diame-

Lot ID	Mean Depth (µm)	Mean Top Diameter (µm)	Mean Vol (x10 4 µm 3)	Volume uniformity	Partial Visual inspection
7731Z006	13.6	39.9	1.19	8.00 %	no defects found
7731Z007	14	40.1	1.23	4.60 %	no defects found
7731Z008	13.9	40	1.21	4.80 %	no defects found
7731Z009	8.8	32.6	0.54	3.70 %	no defects found

Figure 4:
ULCOAT micro bump molds as measured

ter above mean, a red circle means that the actual measured cavity diameter is below mean:

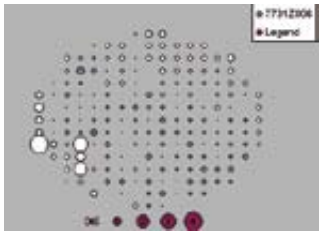

Figure 5

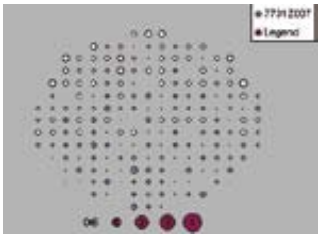

Figure 6

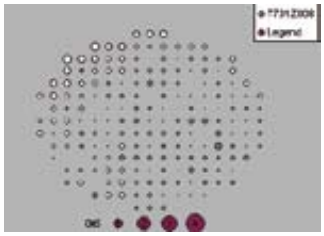

Figure 7

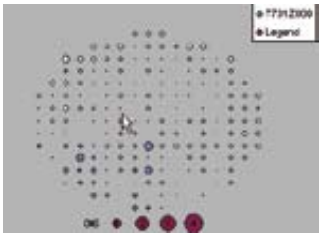

Figure 8

MOLD FILL PROCESS

After the molds have been manufactured and inspected, they were scanned beneath a solder injection head which fills the cavities with liquid solder precisely to the top surface of the mold. Therefore, the solder volume transferred to the wafer is directly related to the volume of the glass cavity. The molds were filled using the SUSS C4NP MFT (Mold Fill Tool) installed at IBM's manufacturing facility in East Fishkill, NY.

A C4NP vacuum fill head was used to fill the molds under a controlled N2/O2 environment. The solder for this experiment was a lead-free SnAg alloy. The fill speed was 1mm/sec.

In a standard C4NP process flow, filled molds are inspected immediately after fill using the SUSS C4NP MIT (Mold Inspect Tool). Since the MIT is configured for standard flip-chip size bumps (<100µm bump diameter range), the microscope resolution was not sufficient for micro-bumps (see Figure 10). Filled mold inspection was done manually using a standard microscope. Due to the large number of bumps per mold, yield information could not be extracted from these limited number of inspection points.

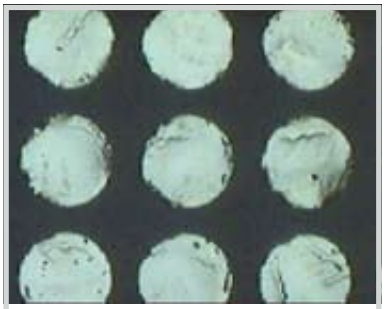

Figure 9:
Filled micro-bump cavities

Figure 10:
Image from standard C4NP MIT – resolution not sufficient for micro-bumps.

MOLD TRANSFER PROCESS

The last step in a standard C4NP process flow is the transfer of solder from the filled mold onto the wafer. At this stage, the wafer must have a fully processed UBM (Under Bump Metallurgy) prepared in order to receive the solder bumps. The UBM for this particular project was provided by IBM using both sputtered and electroplated Ni UBM processes (1µm Ni). The goal of this work was to evaluate micro-bump capability. No reliability data was collected.

Figure 11:
Micro-bumped chip-site (500µm scale)

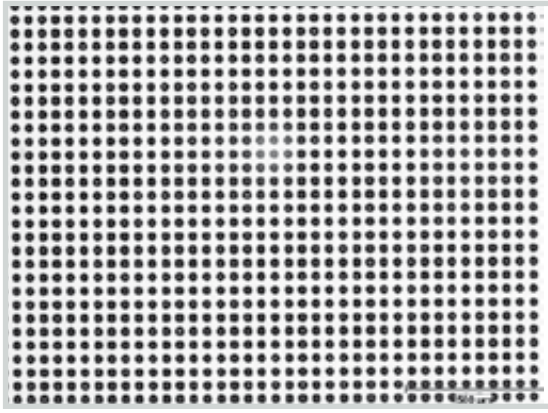

Figure 11

Figure 12:
Micro-bumped chip-site (100µm scale)

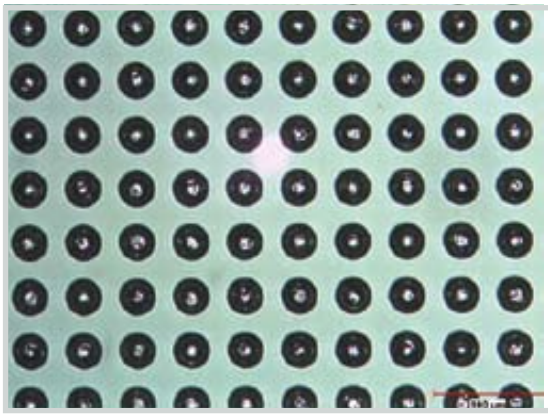

Figure 12

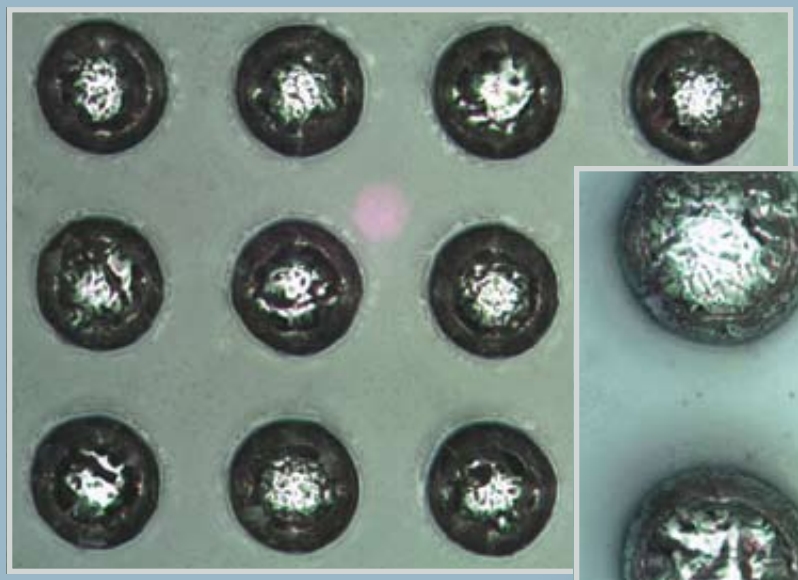

Figure 13:
Micro-bumps at 500x magnification

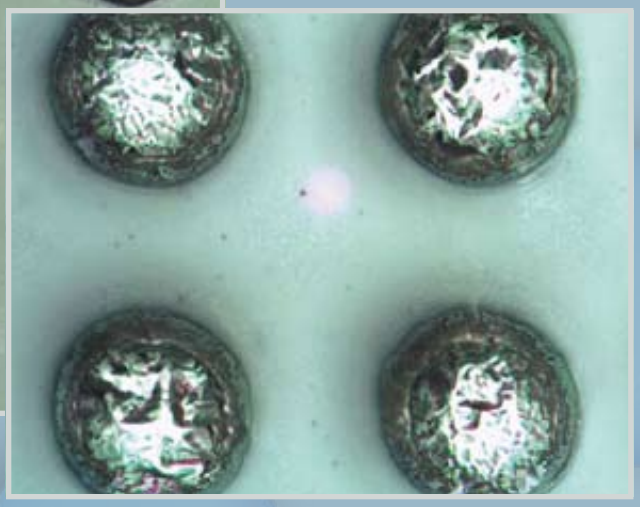

Figure 14:
Micro-bumps at 1000x magnification

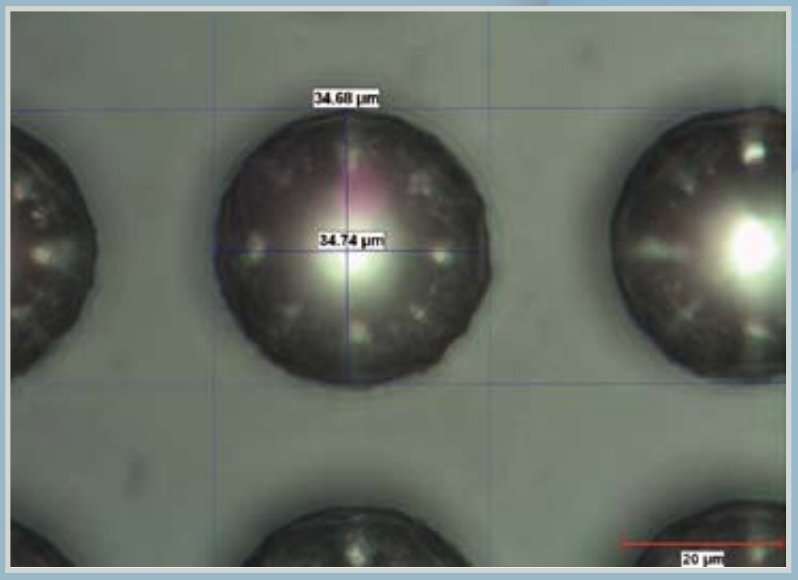

Figure 15:
Bump diameter of C4NP micro-bump

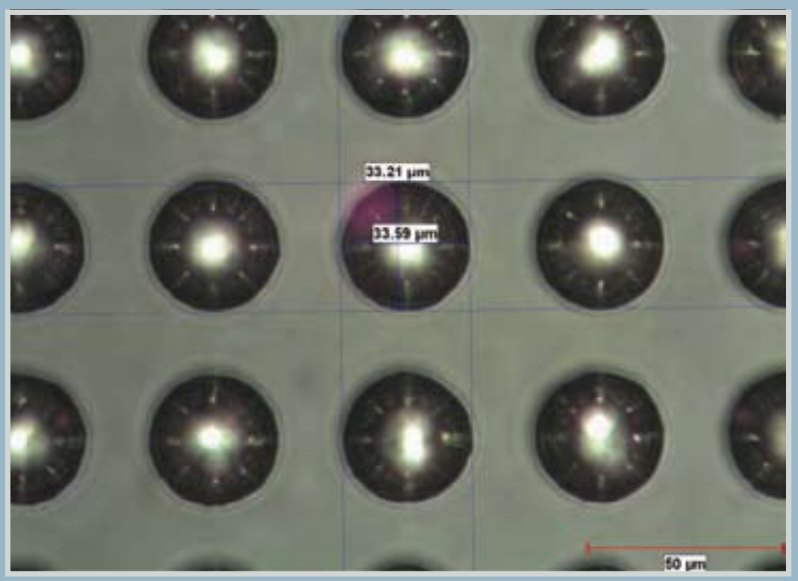

Figure 16:
Bump diameter of C4NP micro-bump

The transfer was performed in a SUSS C4NP STT (Solder Transfer Tool) installed at IBM's manufacturing facility in East Fishkill, NY. The standard SnAg solder transfer process was utilized including a formic-acid vapor scrub prior to transfer to eliminate oxide build-ups on solder and UBM.

MICROBUMPS ON 300MM WAFERS

Inspection of micro-bumps proved particularly difficult due to limitations of standard flip-chip bump inspection equipment. However, the initial feasibility demonstration already yielded many good micro-bumped chips (>85% chip yield) with each chip containing 11,890 fine-pitch bumps, as shown in the following pictures.

Initial metrology of the generated micro-bumps showed excellent size and height uniformity. This is expected as solder ball size is a function of mold cavity volume. As shown elsewhere in this paper, mold cavity volume uniformity is typically in the 5% range or less.

The bumps shown in Figure 15 and Figure 16 show excellent dimensional control. Bump height measurements showed an average bump height of 21µm with very tight height variation.

Figure 17 and Figure 18 show SEM photographs of the 50µm pitch micro-bumps illustrating the excellent bump height and size control of the C4NP process.

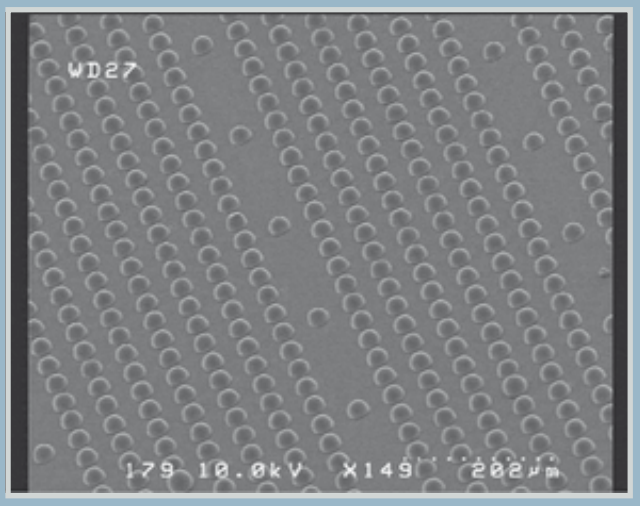

Figure 17:
SEM of micro-bumps

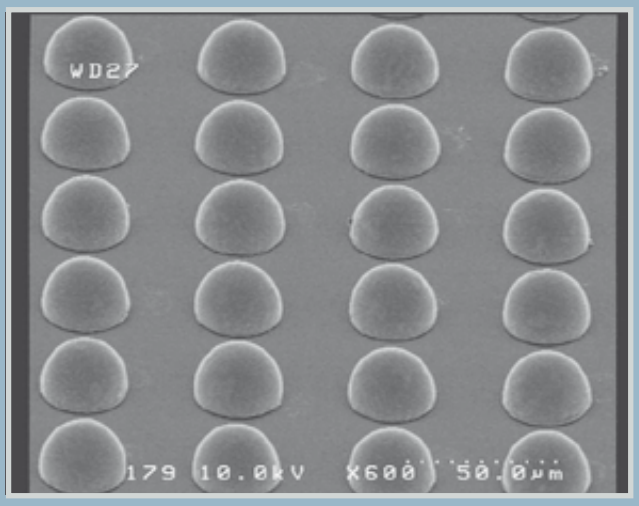

Figure 18:
SEM of micro-bumps

PRODUCTION COST ANALYSIS:

There are two main aspects contrib-uting to the per wafer cost of a lead-free solder bumping process: the cost to create the UBM stack and the cost of building the bump by depositing solder. Prior to C4NP, the most widely used manufacturing pro cess for lead-free flip chip solder bumping was based on electroplating of both part of the UBM stack as well as the solder using a single lithographic layer for patterning. This sequence makes it difficult to draw a line between UBM and bump formation as shown in Figure 19.

The C4NP process is significantly different as it decouples UBM and bump formation entirely. The UBM stack is formed using any variety of UBM processes as described else where in this paper. The bumps are formed using the C4NP process sequence. Figure 20 illustrates the UBM flexibility in combination with C4NP solder deposition.

This fundamental difference in process sequences manifests itself not only in per-wafer cost but also in non-cost related distinctions such as cycle time and process logistics.

The per wafer cost for production wafer bumping is a function of the following cost determining factors: personnel cost, consumable and material cost, equipment maintenance and support, equipment depreciation, building overhead as it relates to equipment footprint and cleanroom requirements, wafer yield, NRE cost per part number or bump pattern, chemistry supply, waste treatment and IP cost.

It would be beyond the scope of this paper to provide quantitative numbers for these various factors. However, Figure 21 summarizes a qualitative assessment of these parameters.

As part of this work, a sophisticated cost model has been developed to investigate the impact of UBM cost on the overall per wafer bumping cost and to model the cost differences of the various UBM process methods described in this paper. Integrated Device Manufacturers (IDM) as well as bumping service providers have largely implemented some version of a UBM and Solder plating process. Assumptions were made as to the type of equipment used, its footprint and facility requirements as well as its capital cost and throughput. Data from several leading equipment suppliers and IDMs formed the basis for this model.

The results show that the UBM-BUMP cost ratio is approximately 2:1. In other words, over 60% of per wafer cost in a typical plated bumping line is driven by the cost of the UBM. This ratio obviously depends on the specifics of the process sequence as well as the type of equipment used. By running the model under varying assumptions, the UBM-BUMP cost ratio ranged from 60%:40% to 75%:25%. From a process perspective, electroplating and photo lithography and their associated cost contributions had the biggest impact on overall per wafer bumping cost.

The results of modeling a typical wafer bumping line show that reducing

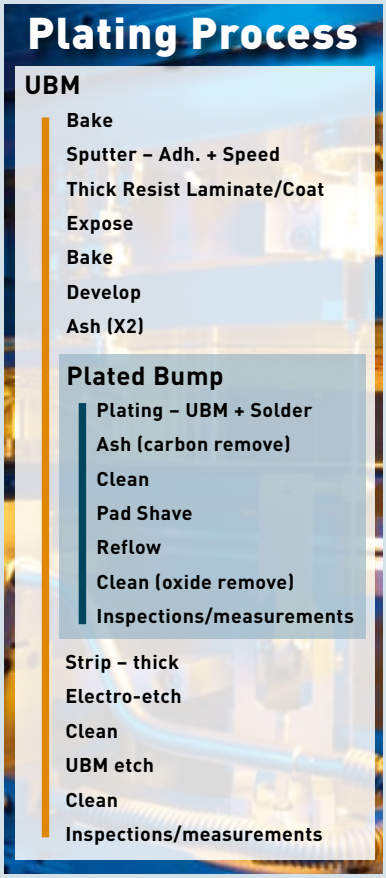

Figure 19:
Integrated UBM-BUMP process flow

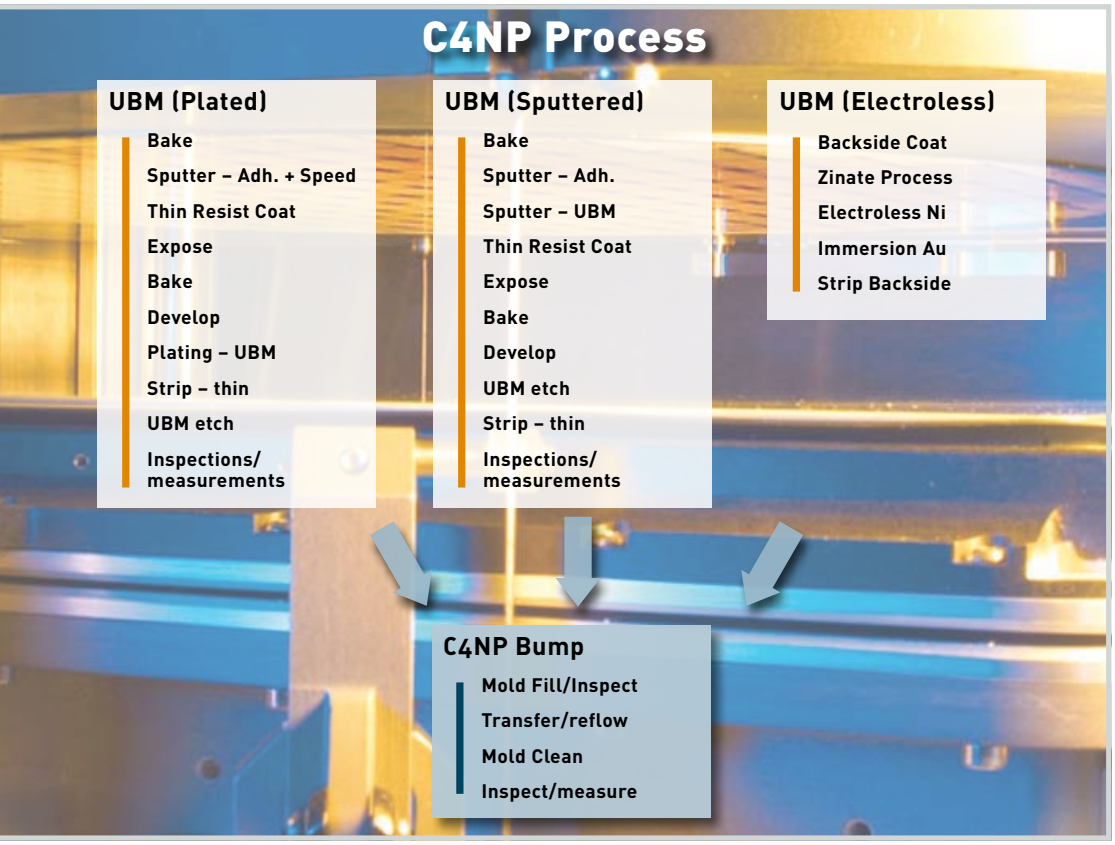

Figure 20: UBM variety in conjunction with C4NP solder deposition method

the UBM cost will have the largest impact on overall per wafer cost.

Unlike a plated bumping line, C4NP bumping technology enables the use of alternative, lower cost UBM process sequences as outlined in Figure 20. This paper focuses on the evaluation of a sputtered TiW/Ni/Cu UBM as well as an electroless Ni/immersion Au UBM which does not involve sputtering. No electroplating technology was utilized. Figure 8 illustrates the per wafer bumping cost results based on the various models. The cost numbers have been normalized in order to show the differences in the various processes without disclosing sensitive or proprietary information from tool and materials vendors. Furthermore, the absolute cost numbers also vary significantly based on regional parameters such as personnel and building cost. For the purpose of a cost comparison, a normalized view eliminates the effect of those parameters. The models were based on 300mm wafers with lead-free solder cost parameters.

A traditional plated bumping line ("Plating UBM and Bump") was modeled as the 100% reference. As outlined above, the UBM portion of the per-wafer cost is over 60%, 61% in this particular case. In comparison, the C4NP bumping line when used with a plated UBM ("Plated UBM+C4NP") resulted in a 16% reduction in overall bumping cost. Although the overall cost reduction is significant, the relative cost of the UBM is even higher – 73% of the total per-wafer cost in this particular case. This is expected due to the necessary electroplating infrastructure in addition to C4NP. Eliminating electroplating all together by replacing the UBM process with an all sputtered metal stack ("Sputtered UBM+C4NP") further reduced the per-wafer cost. UBM processing still accounts for about 69% of the total cost. However, the total cost is down to 74% compared to a traditional plated bumping line. Although lower than in the case of electroplating, UBM cost is still relatively high mainly due to the use of photo lithography. The model for electroless Ni/immersion Au UBM ("ENIG UBM+C4NP) in combination with C4NP solder deposition showed the biggest impact on cost. The total per-wafer cost is reduced to 38% compared to the per-wafer cost of an electroplating bumping line. The UBM only accounts for 42% of that reduced cost.

In conclusion, the achievable cost reduction by utilizing a non-electroplated UBM in combination with C4NP is significant. The reduced cost is mainly driven by the elimination of electroplating and the reduced or eliminated use of photo lithography. Of course, each UBM construction must be evaluated to determine if it meets the reliability requirements for a given application.

One of the most fundamental differences between C4NP and alternative bumping technologies is the use of glass molds. A minimum number of molds are required depending on the number of wafers per day with a particular bump pattern. The cost of molds directly impacts the per wafer bumping

Figure 21: Cost factors for wafer bumping line

Cost Factor	Comment
Personnel cost	Operators, Engineers, Management, Administrative overhead
Consumable and material cost	Bulk solder, glass molds
Equipment maintenance and support	Equipment engineering, scheduled downtime
Equipment depreciation	Function of capital required
Building overhead	Function of footprint and clean-room quality required
Wafer yield	Function of process complexity, number of process steps
NRE cost per part number/bump pattern	Function of mask cost, mold cost, number of uses per mold, number of molds required
Chemistry supply	Function of solder composition and method of deposition
Waste treatment	Function of chemistry used
IP cost/IP wafer toll	Function of IP ownership

cost. The number of reuses of a given mold is critical. Data in previous publications shows that C4NP molds can be used several hundred times before they have to be replaced. The various cost models above consider the impact of C4NP molds on the overall per-wafer cost.

CONCLUSIONS

Solder micro-bumping using lead-free solders is an enabling technology for next generation packaging and integration schemes such as 3D Silicon Carrier Technology. Manufacturing feasibility has been demonstrated using C4NP process to produce high-yielding, high quality micro bumps on wafers up to 300mm.

Bumping cost largely depends on the UBM (Under Bump Metallurgy) technology used. C4NP is a bumping process which can accommodate any UBM. It therefore enables low-cost bumping in comparison to electro-plating of solder.

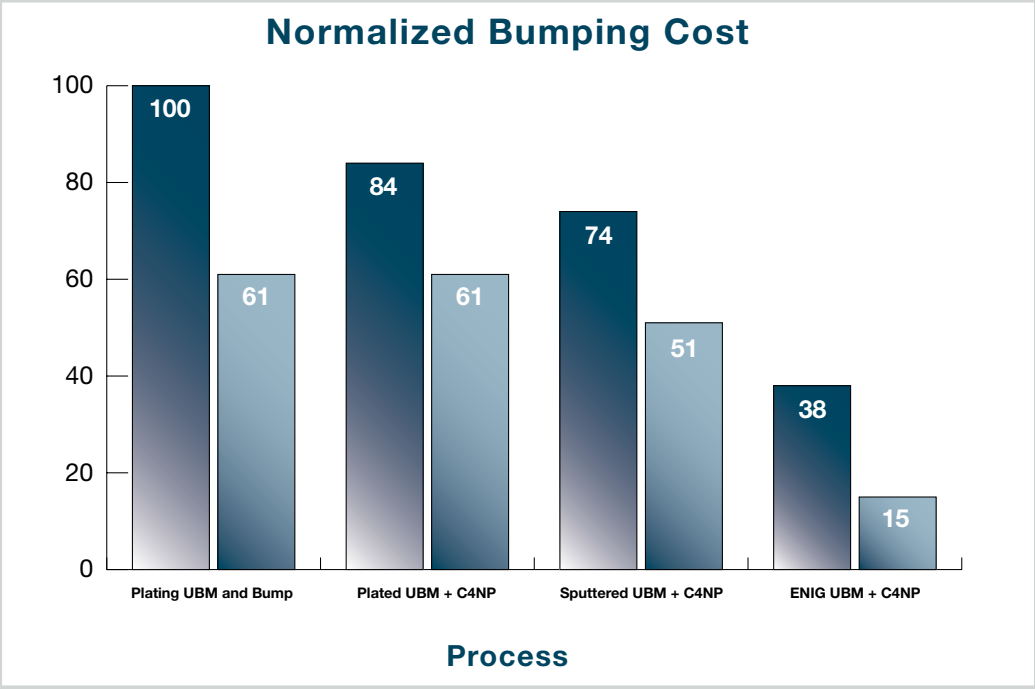

Figure 22: Total per-wafer cost and respective UBM portion of the cost

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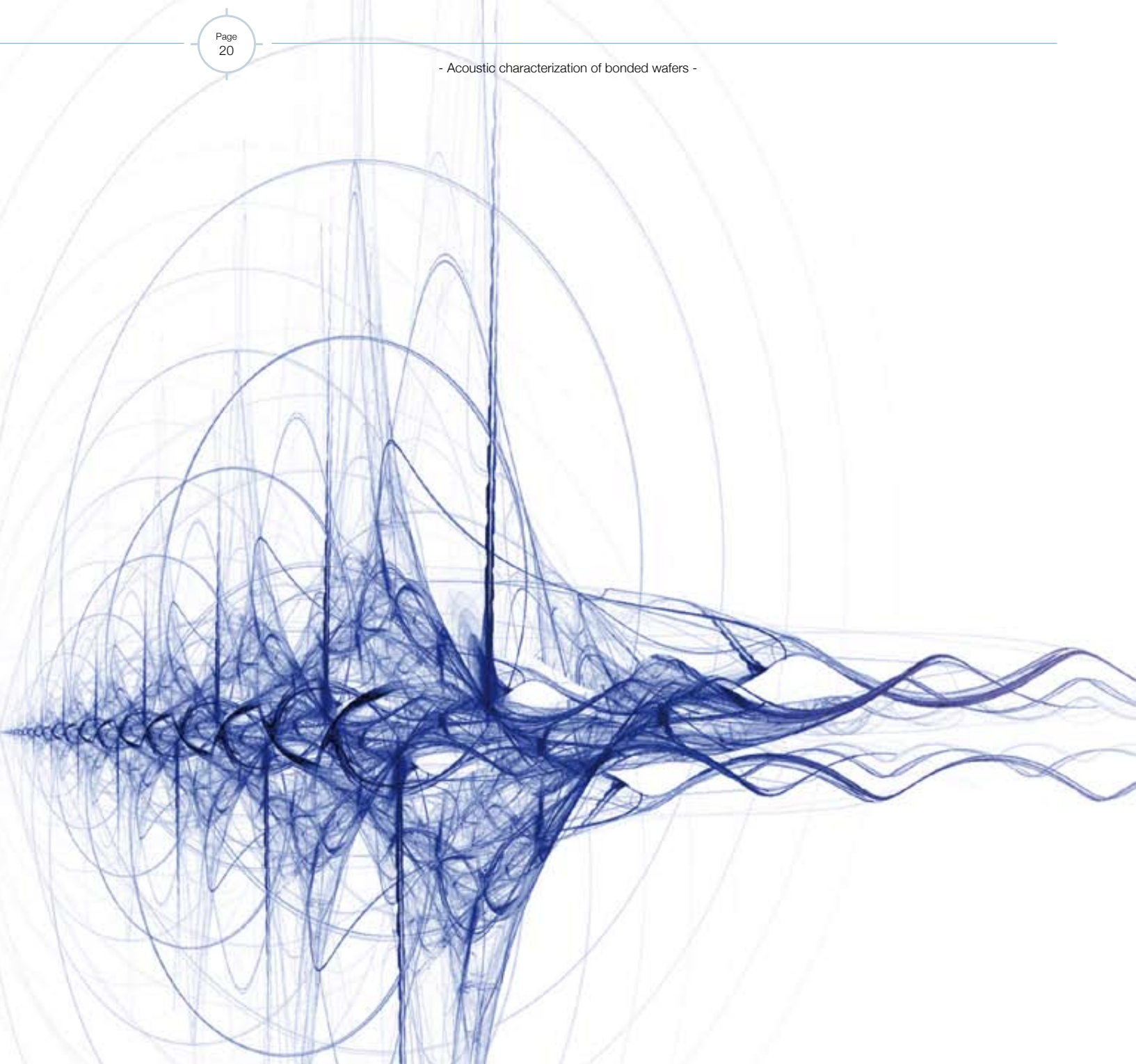

Accoustic Characterization of Bonded Wafers

Dr. Shari Farrens, Chief Scientist and **Sumant Sood, Sr. Applications Engineer,** SUSS MicroTec

ABSTRACT

As more and more MEMS products move towards commercialization, a variety of wafer level packaging techniques have emerged to decrease production costs. Wafer to wafer bonding methods provide hermetic packages for hundreds of devices in a single processing step. Once bonded, most defects are no longer visible to the naked eye but are responsible for die failures. Detection of internal defects in bonded wafer pairs is vital to achieving anticipated yield and for long-term device reliability of packaged MEMS devices. Acoustic micro imaging provides a nondestructive technique for detecting and analyzing these defects and is an essential component of process development and root cause analysis.

INTRODUCTION

Wafer bonding is a mainstream process for the MEMS industry and is an enabling technology for new markets including 3D integration and wafer level packaging. The main types of wafer bonding are glass frit, anodic, metal diffusion, metal eutectic, silicon direct bonding and adhesive bonding.

The variety of techniques reflects the diversity in the products and applications that are addressed by advanced MEMS devices. To protect the delicate moving parts in the MEMS devices, lids or caps must be placed over the devices and seal out moisture, gases and outside access. Most companies find this and the final packaging step are the single most expensive and time consuming tasks in their overall product development program. In addition, almost all MEMS manufacturers must use a unique specialized package for their devices to meet the hermeticity goals, electrical conductivity requirements or cap wafer transparency goals needed for each application. Depending upon the combination of needs one or more of the bonding methods can be used. Yield and device reliability issues are the first priority in any cost of ownership model and thus measurement of the bond quality as early in the process flow as possible is highly desirable to control production costs.

Bond interface defects include voids (air or vacuum pockets) and delaminations (unbonded areas), as well as foreign particles and cracks. Detection of these defects at a buried interface represents a quality control challenge to metrology engineers. While some of the products are transparent to IR (infrared radiation), the sensitivity of this method is limited to large defect size. X-ray imaging is sensitive to extremely small imperfections but is not suitable for polycrystalline interfaces and complex multilayer structures. The technique that addresses the broadest range of materials in the appropriate spatial size range is the acoustic micro imaging method. This paper will discuss the methods used to identify bond defects and bond integrity using acoustic microscopy for a variety of bond interface types.

ACOUSTIC MICRO IMAGING

Acoustic Micro Imaging (AMI) is a non-destructive technique that uses high frequency ultrasonic energy (typically 10 MHz to 300MHz) to look inside

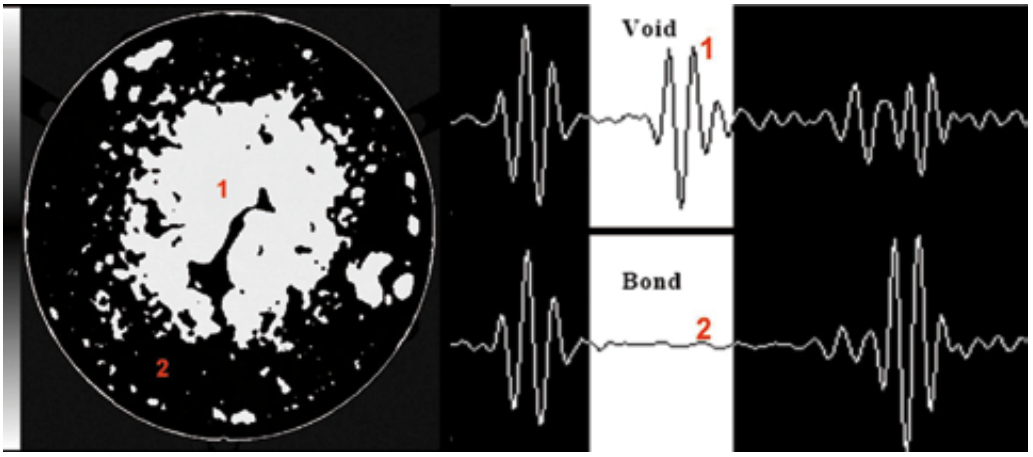

Figure 1:
The acoustic image shows the bond interface between two wafers. Using a symmetric black/white color map, the unbonded areas appear white in contrast to the bonded areas shown in black. The signal frequency scans have the gate (signal acceptance window) for the interface highlighted in white. The bonded area (2) shows no reflection within the gate where as the void area (1) shows a high amplitude reflection.

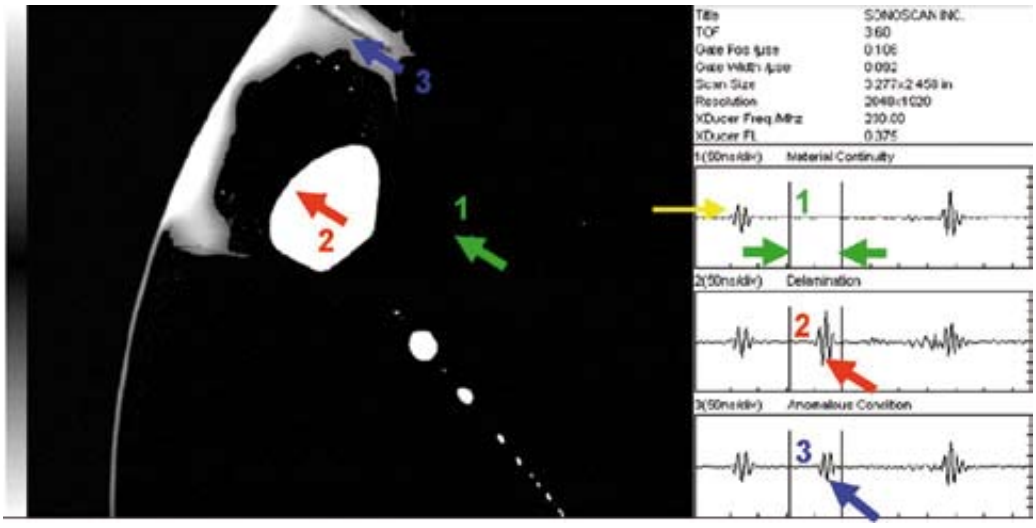

Figure 2:
Section of a bonded wafer interface. (1) marked with green arrow shows the bonded area which is all black. (2) marked with red arrow shows the void caused by trapped air which is all white. (3) marked with a blue arrow depicts an anomalous condition, probably due water ingression through the crack in the wafer. Capillary action often causes water to leach into the interface between die or at unbonded edges.

objects, detect defects and characterize material properties and changes. A focused ultrasonic transducer alternately sends pulses into and receives pulses from reflected signals and discontinuities within the sample. To produce acoustic images, these ultrasound pulses must be effectively delivered or coupled to the sample. Since, air does not conduct ultrasonic frequencies efficiently, the transducer as well and the sample are immersed in a liquid such as alcohol or more commonly de-ionized water. By the same reasoning it is the lack of transmission at air pockets and other defects which result in signal reflection and are the basis of the imaging method.

Ultrasound does propagate well through most solid materials used in microelectronics such as silicon wafers and all compound semiconductor materials regardless of doping levels. In general, the higher the frequency of the transducer, the higher is the resolution of acoustic images. Lower frequencies on the other hand, are more transmissive but give lower image resolution. This technique is largely sensitive to air-gaps, voids and cracks between bonded wafers which exhibit large reflections. Maximum image contrast is obtained when such interfaces are encountered. Additional image contrast is caused by changes in the velocity of the sound waves (incident and reflected) as the various layers are traversed along the wave path. These changes will give rise to "shades" of color or grayscale and allow the user to also observe embedded metal layers as an example.

To evaluate defects at the bonded wafer interface, reflection mode acoustic imaging is generally used. Whenever ultrasound is focused at a boundary between two materials, it is defined as an Interface Scan. In this technique, the ultrasound travels through the substrate until it encounters a different material. At this point, some or all of the ultrasound is reflected back to the transducer. Air gaps or vacuum will return almost 100% of the original signal while the bonded area returns little if any signal due to the impedance match at the interface of the identical materials. The amplitude and phase polarity information of the reflected echoes are used to image the interface. The equation that describes the interaction between materials at an interface is as follows:

$$R = I\frac{Z_2 - Z_1}{Z_2 + Z_1}$$

where R is the amplitude of the reflected pulse, I is the amplitude of the incident pulse, Z1 is the intrinsic acoustic impedance of the material through which the pulse is traveling and Z2 is that of the next material which is encountered by the pulse. All the acoustic images used in this paper were produced using a Sonoscan D9000 series C-Mode Scanning Acoustic Microscope (C-SAM) using interface scan mode.

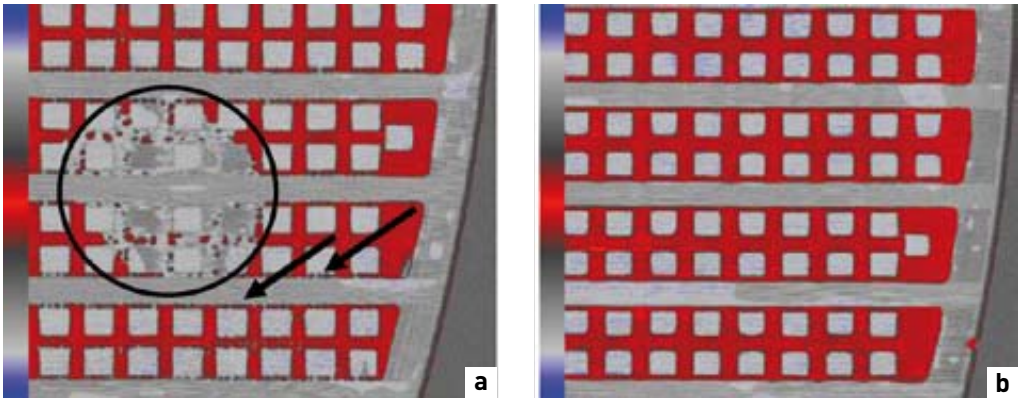

Figure 4:
(a) Image of glass-frit bonded wafers section showing (a) Broken seal rings and non-uniform frit probably due to bad screen-printing (b) good glass frit seals on a section of another bonded pair

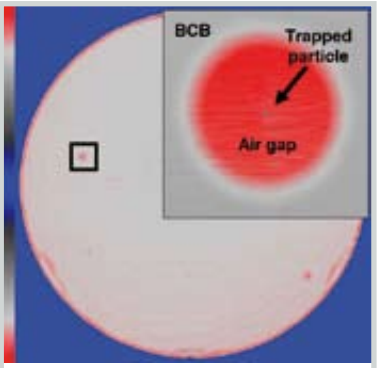

Figure 3:
Image of 8" Si pair bonded using BCB polymer. The defect is highlighted. The inset shows a high magnification image verifying that it is a particle induced defect. The red area around the particle represents an air pocket surrounding the particle source.

BONDED WAFERS EVALUATION

The bond interface for silicon to silicon bonded wafers during direct/fusion bonding was evaluated via interface scan methods. In this case, the voids reflect 100% of the ultrasound while Si-Si interface is almost transparent to these pulses. This provides optimum contrast in the images for the detection of air-gap type defects from trapped particles or improper bond wave propagation. In acoustic terms, a void represents a layer of material whose acoustic impedance differs very sharply from the values of the overlying and underlying material. This sharp difference means that a pulsed beam of ultrasound is reflected at near 100%

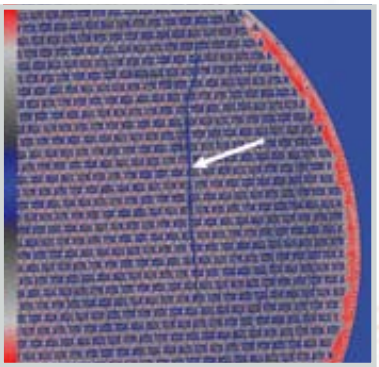

Figure 5:
Acoustic image of Au-Si eutectic bonded wafer pair section. A crack is present in this sample (arrow) which is otherwise not recognizable by naked eye. The pattern of the devices and dark blue seal rings can also be seen in the image.

intensity. Figure 1 shows the difference in contrast between voids and bonded areas using interface scan. Using the color map used in Figure 1 to analyze the scan results, voids typically appear as bright white. In some cases, anomalous features could be detected as gray especially on the edge of the wafer interface or around cracks.

One possibility is that these regions contain a contaminant that has filled at least a portion of the air space, resulting in the slightly different color than a traditional air-gap type void. Delaminations at the edge of the wafer will often ingress water during the scan as shown in Figure 2.

The acoustic characterization of adhesive/polymer bonded wafers poses a challenge because of the low acoustic impedance of polymers used in wafer bonding such as BCB (Benzocyclobutene) and polyimides. Bonded areas between similar materials or materials with similar impedances show very little signal reflection Generally, the contrast between bonded and delaminated areas is low and the transducer needs to be very close to the wafer surface in order to get the best focus at the interface. Figure 3 shows an interface scan of a Si wafer pair bonded using BCB. By looking at the color map used for this image, it is evident that at low resolution, the voids cannot be distinguished very clearly from the rest of the bonded interface.

In glass frit wafer bonding, the main area of interest is the glass frit seal rings at bonded wafers interface. These seal rings are used to encapsulate and protect the MEMS devices. The A-scan signal is gated at the bond interface to get an echo from the frit areas. The areas with the MEMS devices show high amplitude reflection of negative polarity (gray areas) while the frit areas show a low reflection (red areas). The image below shows different sections of a glass frit bonded pair. Figure 4(a) shows the circled area where the glass-frit mesh is broken leading to loss of hermetic seal rings around the devices. In addition, the frit width is non-uniform as shown by black-arrows, probably due to problems during screen printing. Figure 4(b) shows similar area on another wafer with good frit mesh in red.

Crack detection in bonded wafers is also possible using acoustic micro imaging. In this application the cracks in the silicon are “shadowed” against the bond interface (as seen in a eutectic bonded wafer pair in Fig. 5). The size of the shadow produced by the crack will be proportional to the depth of the crack. This normally renders the crack more detectable in the acoustic images and provides information in the images related to depth variations.

SUMMARY

Acoustic Micro Imaging has been shown to be an effective technique for evaluating bonded wafers for the presence of internal defects. AMI has the advantage of being nondestructive in nature and gives important information about the samples that is not easily obtained by any other techniques including X-ray and IR imaging. The obvious drawback is the requirement for the component to be immersed under water. Newer designs such as the waterfall transducer alleviate the problem by flowing the water over and under the component and transducer only during the scan period. The continuing improvements in resolution in acoustic micro imaging will not only benefit the metrology for SOI and MEMS applications but will help characterize newer bond types that evolve with advanced MEMS and 3-D integration.

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is the inventor of plasma activated substrate bonding and holds several patents for this enabling technology. Dr. Farrens has authored and co-authored over 100 publications on SOI, wafer bonding and nano-technology. With over 15 years of hands-on, worldwide experience in academia and industry she is considered an expert on MEMS and wafer to wafer bonding technologies.

SUMANT SOOD
is the Senior Applications Engineer for Wafer Bonders at SUSS Microtec Inc.. His recent experience includes development of plasma enhanced wafer bonding processes for SOI and strained silicon on Insulator (sSOI) applications. Sumant has authored and co-authored more than 15 papers in wafer bonding, SOI, strained silicon and related areas. He received his B.Tech in Electrical Engineering from Punjab Technical University, India and MS in Microelectronics from University of Central Florida.

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1. Janet E. Semmens & Lawrence W. Kessler, „Acoustic Micro Imaging in the Fourier Domain for Evaluation of Advanced Packaging, Pan Pacific Conference“, Jan 2002.

2. Janet E. Semmens & Bryan P. Schackmuth, „Evaluation of Silicon on Insulator (SOI) Bonded Wafers Using Automated Acoustic Micro Imaging“, Pan Pacific Conference, Jan 2001.

3. Larry Dues & Tom Adams, „Checking for Wafer-to-Wafer Bonding Integrity“, Electronics Engineer, Dec 1999

Clif's Notes

Get Rid of Those Darn Spots!

Clifford J. Hamel, Applications Engineer, SUSS MicroTec, chamel@suss.com

The latest SUSS MA200Compact aligner utilizes the Cognex 8100 pattern recognition software for automatic alignment of the mask to substrate patterns. The system is capable of aligning patterns of nearly any shape or design with alignment accuracies of less than 1.0µm. Automatic alignment and the accuracy of that alignment rely on the ability of the pattern recognition software to reliably detect the pattern or model on the substrate. This pattern or image on the substrate, Figure 1, will sometimes be significantly different from the desired pattern shown in Figure 2 due to the presence of unwanted spots or prior processing steps shown in red. These additional patterns may also change in shape, color, or size over time which will add even more difficulty to the alignment process.

A very useful option on the MA200Compact automatic alignment software is the capability to specify areas of the proposed target that should not be considered when doing the pattern recognition. This option is termed 'masking' and has been found to be very useful for automatic alignment of difficult substrates.

Masking is the method whereby unwanted images and artifacts are discarded from the desired target model during the search process. Through a simple procedure available in the Cognex software those areas of the image which are not desired in the target model are removed by using this simple process. The areas highlighted in Figure 3, for example, could be discarded from the model leaving only the dark cross image to be used in the automatic alignment process.

Judging the quality of a proposed target model is accomplished in the software by using a figure of merit called the 'acceptance threshold'. The automatic alignment system searches the field of view for patterns which might fit the target model and assigns an acceptance value to each pattern. The pattern area which exceeds this acceptance threshold value will be used in the alignment process. A typical value for the threshold is about 70 to 80 for a good target model.

In the example shown below a target model has been trained as the green area shown in Figure 4. This model would require that in all subsequent searches for targets that all substrates have nearly the same placement and quality of those lines seen in the target model. A test search of a similar area on another substrate would yield a threshold value of say less than 50 or 60 due to the presence of additional lines and edges in the field of view not in exactly the same place as the model. By masking out all those extra lines, spots, etc that are not wanted in the model, for example the yellow areas shown in Figure 5, a more robust model can be created. Using this 'masked model' on subsequent searches will produce threshold scores greater than 90 which is well above the typical acceptance value.

In summary, the use of the masking option will significantly improve quality of target acquisition in the automatic alignment process. As a result there will be no alignment failures and improved through put.

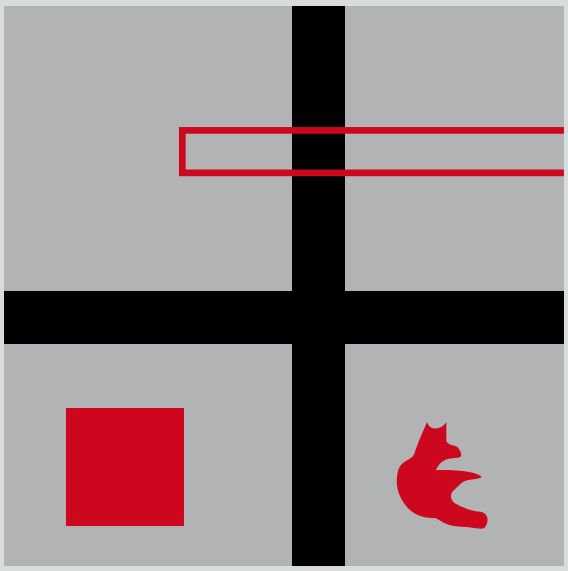


Figure 1: Alignment Target w/ Unwanted Images (Red)

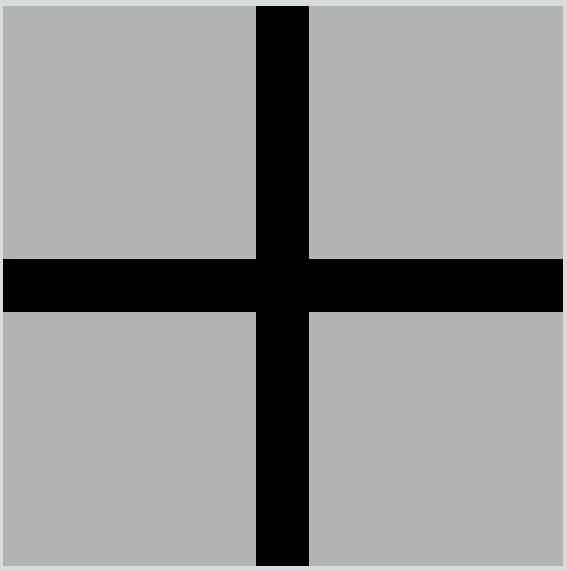


Figure 2: Desired Target Model

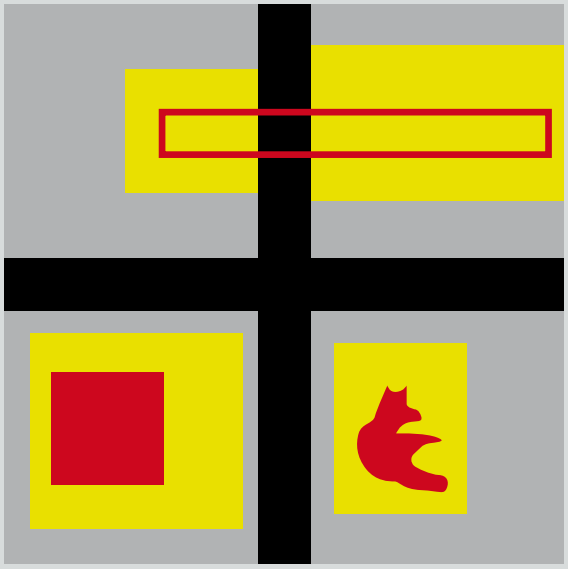


Figure 3: Target Model with Masked Areas

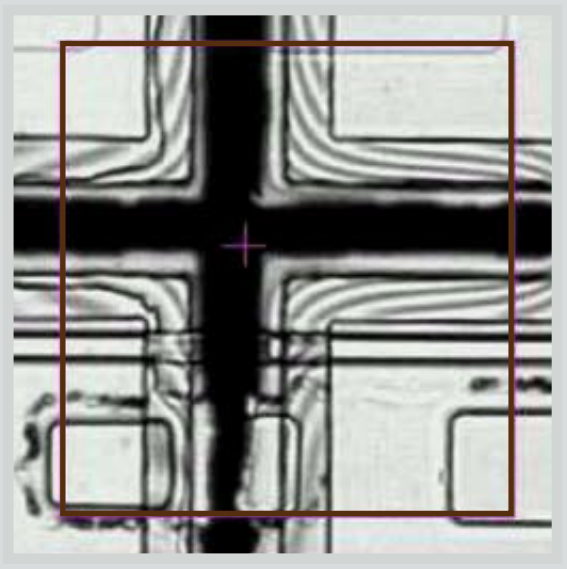


Figure 4: A Typical Target Model w/ Unwanted Images

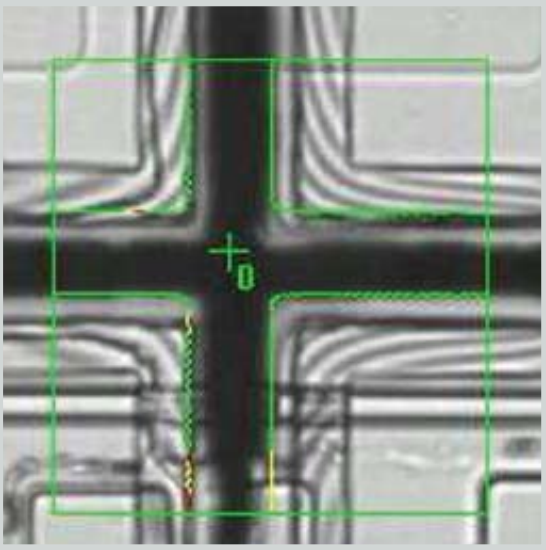


Figure 5: Actual Device Image With Masking In Use

Cliff Hamel

is the principle applications engineer at SUSS MicroTec, Inc. for lithography processes involving full field mask aligners and automated cluster coating equipment. Over the last ten years at SUSS he has co-authored several papers in the field of thick resist processes and process optimization. He has over 26 years of BEOL process and mask fabrication experience at IBM where he was the principle engineer and inventor for lift off process development. He received his BS in chemical engineering at Trinity College of Vermont.

SUSS in the News

Here's a summary of our recent press releases. To read the entire press release, please visit www.suss.com/about_suss/latest_news

January 16, 2008
Freescale Selects 200mm SUSS Tool Set for MEMS Facility

SUSS shipped and successfully installed several microelectromechanical systems (MEMS) production tools at Freescale Semiconductor. The equipment included a new DSM200 Series Front-to-Back Alignment Verification System, the latest generation SUSS MA200Compact Mask Aligner as well as a SUSS ABC200 series Wafer Bond Cluster system for use in MEMS sensor applications. "Front-to-Backside alignment verification is an important metric for Freescale for cost-effective mass production of MEMS devices," said Satoru Matsumoto, vice president, Fab Operations, Freescale Semiconductor. "The ability of the DSM system to provide outstanding process control at an early stage of the process can help produce a higher overall yield. We chose SUSS MicroTec because it offers effective lithographic and wafer bonding solutions for MEMS applications as part of a competitive package." The Wafer Bond Cluster with unsurpassed post bond alignment accuracy is especially designed to meet the stringent requirements for advanced MEMS sensor production. Freescale first purchased and installed the equipment in its 150mm Sendai Fab. Based on Sendai's successful experience, Freescale purchased additional tools for its 200mm MEMS production line at its Oak Hill Fab in Austin, Texas.

January 16, 2008
SUSS MicroTec Lithography Quality Management Now Certified According to ISO9001:2000

SUSS MicroTec Lithography GmbH, a leading manufacturer and supplier of production and process lithography systems now holds the globally recognized ISO 9001 certification for having established a high level process- and system-oriented quality management (QM) based on ISO9001 quality standards. The certificate is evidence of SUSS MicroTec Lithography's commitment to provide consistent highquality development, production and service processes at both German manufacturing sites in Garching (near Munich) and Vaihingen/Enz (near Stuttgart).

ABC200 Automated Wafer Bonding Cluster System, State-of-the-Art Production Wafer Bonding

Wilfried Bair
Vice President Strategic Business Development, SUSS MicroTec AG

December 5, 2007
SUSS MicroTec AG appoints new VP Strategic Business Development

SUSS MicroTec, a leading supplier of precision manufacturing and test equipment for the semiconductor and related markets has appointed Wilfried Bair to the position of Vice President Strategic Business Development. Initially he will be focusing on further developing SUSS' 3D Packaging and 3D Integration product portfolio. An expert in 3D technology applications, Mr. Bair joins us after gaining many years management and business development experience in the semiconductor industry throughout Europe, the US and Asia.

November 21, 2007 · SUSS MicroTec Receives Multiple Wafer Level Packing Equipment orders from ASE

SUSS MicroTec received significant multiple orders for its lithography production equipment from the ASE Group, the world's largest provider of independent semiconductor manufacturing services in assembly and test. The first order packages were booked in October and November and included several production mask aligners and coat/bake/develop clusters for 200 and 300mm, that will be installed at ASE's wafer level packaging and redistribution process facility in Kaohsiung, Taiwan.

September 25, 2007
Leaders in 3D Packaging Equipment Announce Seminar Series on Integrated Process Solutions
NEXX Systems, Surface Technology Systems (STS), and SUSS MicroTec announced they will collaborate with Fraunhofer IZM to demonstrate integrated process solutions for 3D wafer level packaging. As a first action, a series of seminars has been scheduled from October 26 to November 7, 2007. The seminars will be held in Singapore, Japan, China, Korea, and Taiwan and are targeted at packaging industry professionals involved in 3D packaging applications.

September 11, 2007 · Rohm and Haas Purchases Coating Cluster from SUSS MicroTec for Resist and Spin-on Dielectric Qualification
SUSS announced it received the first order for its new Gamma XPress coat/develop cluster from Rohm and Haas Electronics Materials, a world leader in the development and manufacture of electronic materials for the semiconductor markets. The system from SUSS MicroTec will be used by Rohm and Haas Electronic Materials to develop, characterize and optimize photodielectrics and both thick and thin photore-sists. The SUSS Gamma XPress was chosen over alternative equipment due to its superior thick resist processing capability and its bridge tool design that permits concurrent handling of wafers with different sizes without mechanical changeover.

September 4, 2007 · SUSS MicroTec and STS take MEMS Roadshow to Europe
SUSS MicroTec and Surface Technology Systems, two of the leading providers for MEMS manufacturing solutions worldwide, announced that the successful "MEMS Roadshow", which toured 5 cities in the US earlier this year, will now travel to Europe.

August 14, 2007 · SUSS MicroTec Annouces New 200mm Coater Chosen by HD MicroSystems to Support Polymide Material Technologies
SUSS announced that HD MicroSystems, L.L.C., a joint venture between Hitachi Chemical Co., Ltd. and DuPont Electronic Technologies, has installed the advanced 200mm Gamma Production Coat/Develop Cluster to support the company's polyimide and PBO material technologies.

July 10, 2007 · SUSS MicroTec Accounces New Gamma XPress
SUSS launches the Gamma XPress, an advanced coating cluster targeting wafer bumping as well as LED manufacturing applications. The Gamma XPress coating cluster is offered in different configurations designed for specific applications. These include gold bump coating, under bump metal or redistribution coating, high volume LED coating as well as standard and dry film developing. The market-oriented concept of the Gamma XPress combines an efficient and flexible production setup with short lead times, thus helping to keep the customers' time to market to a minimum.

July 19, 2007
SUSS MicroTec launches iVista™ High-Resolution Digital Microscope
Innovative new microscopy tool to enhance productivity and simplify routine tasks
SUSS MicroTec AG, the premier supplier of wafer-level test systems for semiconductor devices, launched the iVista™ High-Resolution Digital Microscope. Its introduction follows the rapid changes to device design implemented by manufacturers in response to economic and technological drivers. These changes challenge all test engineers, who are now faced with small pads, high numbers of contact pads and extremely complex circuitry.

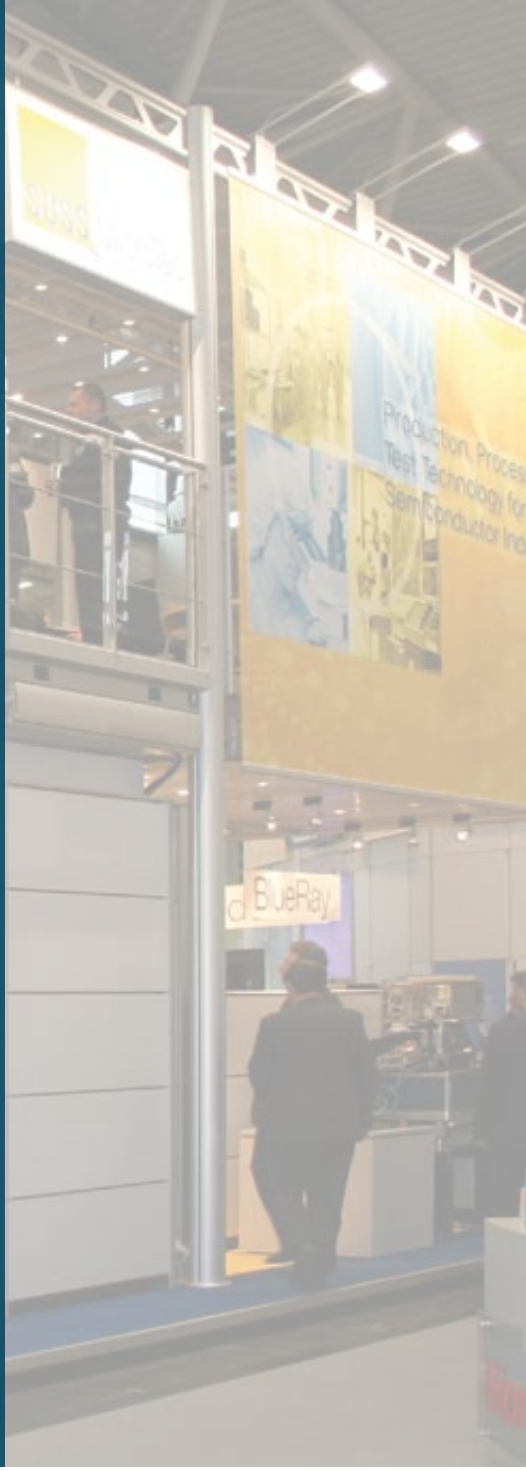
July 18, 2007 · SUSS Announces 300mm SOI Bonding System
SUSS announced the launch of it's new 300mm SOI wafer bonding system. Called the ELAN CBC300SOI, it represents the most recent addition to SUSS' wafer bonder product portfolio. Additionally, SUSS announced it has already shipped its new 300mm SOI wafer bonding system to a leading manufacturer of silicon-on-insulator (SOI) wafers.

July 17, 2007 · SUSS MicroTec Unveils New ProbeShield® Technology
Advanced wafer-level device characterization and reliability test system shortens time to market and increases return on investment
SUSS MicroTec AG, the world's premier supplier of wafer-level device characterization and reliability test systems for the semiconductor industry, today unveiled its new ProbeShield® Technology. Implementing unique design features, ProbeShield Technology significantly improves the way in which semiconductor devices are characterized and their reliability tested. The semiconductor device manufacturer thus benefits from quicker, more accurate measurement results, which means more efficient model extraction, faster model turnaround and fewer design iterations, reduced time to market and ultimately a higher return on investment.

Below are some of the places you can find SUSS in the upcoming months:

Date	Tradeshow/Seminar	Location	Focus
Jan. 28-31, 2008	Elektronic EP 2008	Stockholm, Sweden	Test
Jan. 30-Feb. 1, 2008	Semicon Korea	Seoul, Korea	Semi
Feb. 13-15, 2008	nanotech2008	Tokyo, Japan	Nano, MEMS
March 4-5, 2008	Innovation in Microsystems	Munich, Germany	MEMS
March 13, 2008	MEMUNITY Workshop	Ilmenau, Germany	MEMS
March 18-19, 2008	IMAPS Device Packaging	Scottsdale, Arizona	Packaging
March 18-20, 2008	Semicon China	Shanghai, China	All
March 24-27, 2008	ICMTS	Edinburgh, Scotland	DWC
April 1-4, 2008	AMPER	Praha, Czech Republic	Semi
April 9-10, 2008	Smart Systems Integration	Barcelona, Spain	MEMS, Nano
April 15-18, 2008	Expo Electronica	Moscow, Russia	Semi
April 21-24, 2008	ICMMT2008	Nanjing, China	Test
April 23-24, 2008	Semiconductor Conference Dresden	Dresden, Germany	WLP
April 23-25, 2008	Sensors Expo	Tokyo, Japan	MEMS
April 29-30, 2008	3D-Integration	Washington	3D
April 27-May 1, 2008	IRPS	Phoenix, Arizona	DWC
April 29-May 1, 2008	Nepcon	Birmingham, Great Britain	Test
May 5-7, 2008	Semicon Singapore	Singapore	All
May 6-8, 2008	CLEO 2008	San Jose, CA	Opto, LED
May 6-8, 2008	Sensor & Test 2008	Nurnberg, Germany	MEMS
May 6-8, 2008	Opto 2008	Nurnberg, Germany	MEMS
May 27-29, 2008	PCIM Europe	Nurnberg, Germany	DWC
May 27-30, 2008	ECTC	Lake Buena Vista, Florida	ADP, MEMS
June 2-4, 2008	Semicon Expo CIS 2008	Moscow, Russia	All
June 4-5, 2008	EEEfCOM 2008	Ulm, Germany	All
June 11-13, 2008	OPTO Taiwan 2008	Taipei, Taiwan	All
June 15-20, 2008	IMS/MTTS-Symposium	Atlanta, GA	Test
June 20, 2008	ARFTG	Atlanta, GA	Test

For updates to our schedule, please visit www.suss.com



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or write to **info@suss.com** with your comments and suggestions.

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SUSS. Our Solutions Set Standards

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