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SUSS report

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A Robust Broadband Calibration Method for Wafer-Level Characterization of Multiport Devices

WiMAX, UWB, WirelessHD, 4G: Next-generation technologies are driving development of advanced high-frequency differential and multiport semiconductor devices. In this issue, read about the new RRMT+ calibration method, which enables these RF devices to be accurately characterized on wafer, improving yield and optimizing the development cycle.

Also in this issue:

- **Vacuum and Hermetic Packaging for MEMS Using Lead-Free Solder**
- **UV nanoimprint materials: surface energies, residual layers, and imprint quality**
- **CN4P Have you played a game lately?**

SÜSS MicroTec

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Full View

Getting personal with SUSS

The question is often raised why take the time, and incur considerable costs to go to a trade show – especially when information is readily available on company websites, via webcasts and in "virtual trade shows"? The SUSS Report asked SUSS' Division Managers why they think a visit to a SUSS booth at a trade show is worthwhile and why a SEMICON West® in particular will be of value.

Rolf Wolf

Rolf Wolf & Ralf Süss – Division Managers Lithography Products

Rolf: "Of course the internet is a valuable information source – and our recently relaunched website offers viewers a lot more information about our products and markets as well as the chance to download more detail if desired. However, the personal contact at a show cannot be underestimated. That is why SUSS makes a point of not only having sales account managers on hand to welcome people to our booth but also application and product engineers who are there to answer even the most indepth questions about a tool or technology."

Ralf Süss

Ralf: "…and having those experts with you when you see a new tool for the first time is invaluable.

The SUSS DSM200 Front-to-Backside Alignment Verification Tool for example will have its premiere on our wafer processing booth in the North Hall (#5639) at this years SEMICON West. It's a tool which takes the guesswork out of doubleside exposure metrology. If you require doubleside alignment and exposure of devices such as MEMS, power semiconductors and optoelectronics, then it is imperative that you take the time to look at this fantastic new system. It's high level of automation enables an operator to verify whole batches of wafers with minimal operator involvement – singling out failed wafers for rework before the irreversible etching process thus saving both time and money."

The SUSS DSM200 for accurate automated front-to-back-side alignment verification

Claus Dietrich – Division Manager Test Systems

"In 2005, when SEMI moved the back end part of the exhibition from San Jose to San Francisco to run in parallel with the front end show, the packaging, assembly and test booths were not well visited and we doubted the future of the show for us. However last year proved us wrong and we are excited that this year we can unveil 2 new products on our West Hall booth (#7311) which is dedicated entirely to our Test Systems.

In San Francisco we will be launching our new generation of **ProbeShield® Technology for highly accurate device characterization and reliability measurements.** Revolutionary new design features will enhance the shielding effectiveness, ergonomics and mechanics to provide the safest and most accurate probing solution available. Alongside the new ProbeShield Technology is the innovative new **iVista™ High-Resolution Digital Imaging System**. This powerful new microscope is dedicated for semiconductor probing applications from device characterization to failure analysis. The system is based on a unique, ultrahigh-resolution digital imaging concept to provide the user with crystal-clear live images and a multiple view function, which allows several regions in the field of view to be magnified for closer examination without losing the 'big picture'."

Gael Schmidt – Division Manager Device Bonders

"Being based as we are in the beautiful French countryside, SEMICON West is an excellent opportunity for our American customers and prospective clients to meet with us and see our latest developments for themselves without having to cross the Atlantic. We are especially looking forward to demonstrating our new **KADETT K1 – a new High Accuracy Placement and Bonding System** especially configured for R&D laboratories, Universities and preproduction environments.

The system performs accurate Pick and Place functions as well as a wide range of bonding processes including In-Situ Reflow, Thermo-Compression, Thermo-Sonic and Adhesive Bonding. The KADETT, originally developed by the Paul Scherrer Institute, has already been proven in the field for bonding Ionizing Radiation Detectors and it is also well suited for Advanced Packaging, micro-optics or MEMS assembly."

Michael Kipp – Division Manager Wafer Bonders

"A show is no longer necessarily just a tool to sell products and meet new potential buyers. It is also a great opportunity to touch base with a company you are already very familiar with. Ongoing matters can be discussed and while internet research can help initially it still doesn't beat sitting down with the experts and really getting a grip on the situation. As the head of the rapidly growing wafer bonding division I can say that this year wafer bonding experts will be on hand to discuss the latest addition to the ELAN wafer bonding family, the CB8. **The ELAN CB8 semi-automated wafer bonder** represents the next level of tool performance for high-precision, high-yield wafer bonding. Its superb force and temperature uniformity as well as the super clean, high-vacuum environment will improve yield even in the most critical applications. Of course my colleagues from the **C4NP wafer bumping project** – the joint technology development with IBM will be on the booth to update visitors with the latest results and to answer any questions. Speaking additionally as the head of all our North American operations I can personally say what a great pleasure it is to be on the booth and meet so many old and new friends."

ELAN CB8 semi-automated wafer bonder

SUSS' new iVista digital microscope on top of the ProbeShield

Vacuum and Hermetic Packaging for MEMS Using Lead-Free Solder

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ABSTRACT

Wafer bonding has been widely used for forming vacuum and hermetic packages for MEMS devices. Several techniques, including anodic silicon-glass, silicon-silicon fusion, metal compression, glass frit, eutectic, and solder bonding have been attempted and some have been demonstrated successfully. Solders have some advantages that make them an interesting area of research for wafer bonding. They offer lower permeability, lower temperature bonding, and the potential for die area savings through smaller bond rings. Some of the challenges of solder bonding are discussed. Then an overview of traditional solder wafer bonding as well as an advanced solder bonding technique called diffusion soldering is presented.

INTRODUCTION

Many MEMS devices are experiencing substantial growth as they find their way into products that span consumer devices to national security. Packaging of these devices is still one of the most difficult and costly parts of the fabrication process, especially for packages that need a vacuum environment and/or a hermetic seal. Vacuum packaging is critical for resonant devices to achieve high quality factor (Q) and also for thermal imaging devices to increase the thermal isolation of the sensor platform. Hermetic seals are needed for devices that do not require vacuum for proper operation, but still need to keep out unwanted contaminants, such as moisture. Water vapor accelerates the failure of many devices, so a clean, dry environment is necessary for long term reliable operation. Seals used to create vacuum packages can provide this environment because they must have excellent hermetic sealing capabilities in order to main-tain vacuum in the micro domain.

Glass frit wafer bonding is widely used by industry for creating MEMS vacuum packages for many reasons. It is a proven process with demonstrated long term reliability and low vacuum levels.

Its thermal coefficient of expansion can be tailored to match the device and package substrates to reduce residual stresses from thermal expansion mismatches. And it can planarize over topology, such as electrical feed-throughs, because the bonding temperature is above the glass transition temperature of the frit. There are several limitations with glass frit that spur research into other vacuum packaging approaches. The lower temperature glass frits contain lead, which is banned from importation into many countries.

Also, glass frit is usually applied through a screen printing process, which limits the smallest definable bond ring to ~200 microns. Combining this with the difficulty of aligning the screen to the wafer, a large area of the die needs to be dedicated to the bond ring to achieve a good glass frit bond. Finally, glass as a material class does not offer the best hermetic sealing capability vs. width because of its high permeability [1]. Solders have several attractive qualities that make them interesting candidates for replacing glass frit in vacuum packaging applications. First, all solders are metals, which have the lowest permeability of common packaging materials. Second, there are numerous solder alloys that span a range of melting temperatures from near room temperature to many hundreds of de-

Figure 1: Illustration of the cross section of the wafers just before tin solder bonding and after dicing.

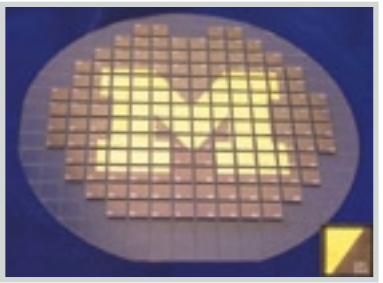


Figure 2: Picture of the bonded and diced lead-free flux-free solder bonded wafer.

Material System	Process Time and Temp.	Remelt Temp.
Copper - Indium	4 min at 180 °C	> 307 °C
Copper - Tin	4 min at 280 °C	> 415 °C
Silver - Tin	60 min at 250 °C	> 600 °C
Silver - Indium	120 min at 175 °C	> 880 °C
Gold - Tin	15 min at 260 °C	> 278 °C
Gold - Indium	0.5 min at 200 °C	> 495 °C
Nickel - Tin	6 min at 300 °C	> 400 °C

Table 2: Several Diffusion Soldering material sets with the formation and service temperatures. [2]

Composition, wt %							Eutectic °C
Ag	Bi	In	Pb	Sn	Au	Si	
…	49.0	21.0	18.0	12.0	.	–	57
…	57.0	…	…	43.0	…	–	139
3.0	…	97.0	…	…	.	–	144
…	…	99.4	…	…	0.5	–	156
…	…	…	38.0	62.0	…	–	183
3.5	…	…	…	96.5	…	–	221
…	…	…	…	20	80	–	278
–	–	–	–	-	97.1	2.9	363

Table 1: Several Low Temperature Solders with their Melting Point and Composition. [2]

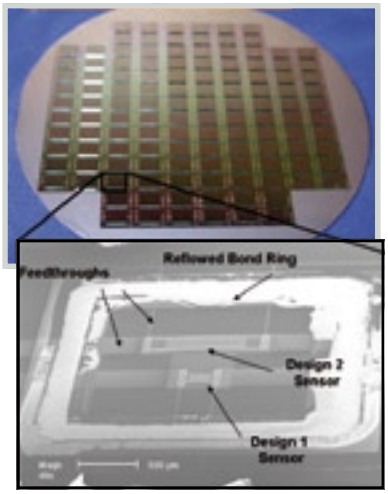


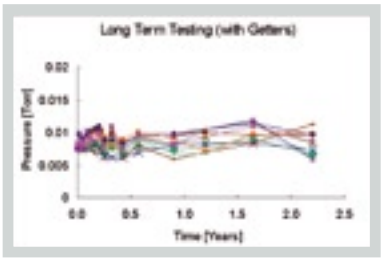
Figure 3:
A 4" wafer full of packages created with Au-Si wafer bonding.
The bottom picture shows an intentionally de-capped package with the bond ring and Pirani gauges.

grees Celsius (See Table 1). The range of melting temperatures allows the packaging engineer to pick an alloy with a melting temperature that suits the thermal requirements of the package. Lastly, solders melt and become liquid during the bonding process; this allows them to flow over and seal wafer topologies such as electrical feedthroughs. There are several challenges involved in using solder as a bonding mechanism for vacuum packaging. A typical soldering process uses fluxes to remove metal oxides and other contaminants to promote good wetting between the solder and the substrate. However, flux is not compatible with MEMS processing. The liquid flux can cause stiction issues with released MEMS devices and they leave behind residues that would ruin a vacuum package by outgassing. A flux-free solder process is necessary to vacuum package MEMS for these reasons, but it takes careful design of the bond joint and the solder process to achieve good wetting without flux. Also, the solder alloys must be lead-free to comply with emerging worldwide legislation banning lead in electronics components. The final challenge for solder wafer bonding lies in the fact that most wafer bonders have long thermal time constants, especially if the bonding chamber is pumped down to high vacuum. This increases the time the solder remains molten from tens of seconds in a typical solder process to several minutes in a standard wafer bonder process. This can be a problem because molten solder consumes most metals very rapidly through intermetallic formation [2].

All these challenges necessitate careful design of the bond joint and careful selection of the materials involved. This article reviews some of the results of solder wafer bonding projects from around the world and highlights the research efforts from The University of Michigan.

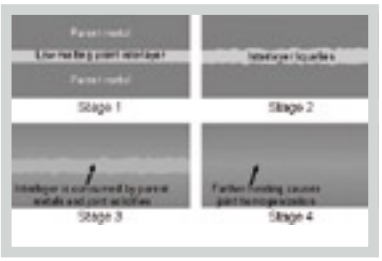
TRADITIONAL SOLDER BONDING

One of the first applications of solder wafer bonding for MEMS used lead-tin and gold-tin solders to create absolute capacitive pressure sensors by bonding a wafer with a thinned diaphragm to another carrier wafer [3].



The bond formed a good seal, but there was little information about the pressure level inside the cavity or the hermeticity of the seal. The first use of solder bonding specifically for vacuum packaging was reported by Sparks [4]. Pb-Sn solder was used to create a vacuum cavity for microresonators. The seal was goodand the pressure was measured by monitoring the Q of the resonators. However, the pressure inside was not very low because there were no integrated getters. Getters are necessary to remove the outgassing that comes off the wafers and solder during the bonding process; without getters it is very difficult to achieve pressures below 1 Torr. Another solder bonding approach was used to package Infrared Radiation (IR) sensors [5]. It achieved very good vacuum levels, but there is no detailed information on the package design or bonding process. At Michigan, we have used a thick electroplated nickel underbump metallization (UBM) covered with a thin gold layer to achieve a lead-free flux-free tin-based solder bonded vacuum package [6]. The thick nickel UBM can survive contact with the molten solder for the long bonding times inherent in standard wafer bonders without getting consumed by intermetallic formation. After electroplating the nickel, a quick etch in dilute HCl removes the nickel's native oxide and then a thin layer of gold is evaporated onto the nickel. The gold layer serves as a wettable surface and prevents further native oxide growth on the underlying electroplated nickel layer. Figure 1 shows the wafers right before bonding.

The wafers are heated to 300 °C for 10 minutes in a vacuum environment to melt the solder and form the bond. It is important that the bonding environment be non-oxidizing, such as vacuum or inert gas, because there is no flux to remove any oxide that would form on the solder in an oxidizing environment. During the bonding process, the tin solder wets the gold and consumes it, revealing a clean nickel layer underneath without any native oxide. With this process, we created vacuum packages with internal pressures in the single Torr range without any getters (See Figure 2). There are other fluxless soldering processes, such as plasma



Left Figure 4:
Plot of the pressures inside the Au-Si eutectic bonded packages vs. time.

Right Figure 5:
The four stages of a diffusion soldering process. [2]

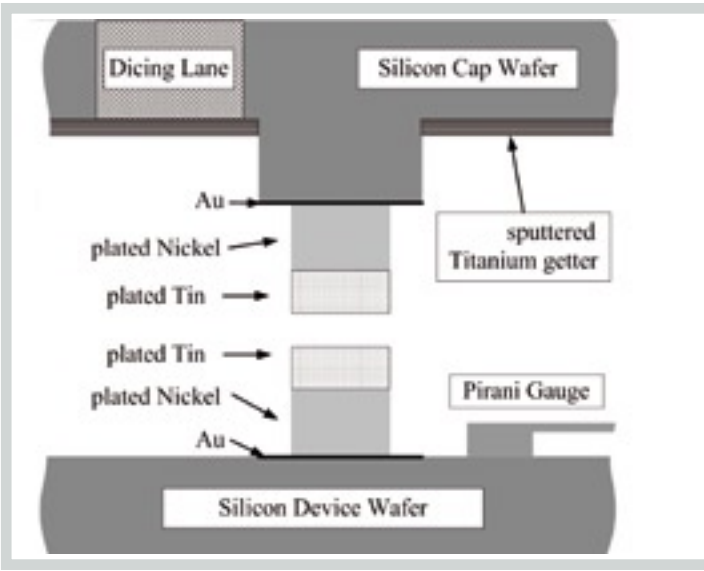


Figure 6:
Illustration of the cross section of the nickel-tin diffusion soldered packages right before bonding.

assisted dry soldering (PADS) and the indent reflow seal (IRS) technique bonding that have also achieved good results [7-8].

GOLD-SILICON EUTECTIC BONDING

Another solder, gold-silicon eutectic, has long been used for wafer bonding because of its simplicity and ready availability of gold and silicon in micromachining processes [9]. The bond forms at 363 °C for 19 at% silicon and 81 at% gold composition and can be used to create hermetic and vacuum seals. Work has been done to characterize the bonding and adhesion quality of the eutectic to different materials, including Si/Ti/Au to Au/Ti/Si; Si/Ti/Au to Si; Si/Ti/Au to polySi/Si; Si/Ti/Au to Oxide/Si; and Si/Ti/Au to nitride/Si. It was found that the bond quality and uniformity between Au-Au, Au-Si, and Au-PolySi was the best [10]. Further work has been done to apply this bond to vacuum and hermetic packaging.

Mitchell bonded a cap wafer with electroplated gold and Nanogetters™ from ISSYS Corporation to another wafer with a thin layer of polysilicon to package micromachined Pirani gauges [11]. The 4" wafers were outgassed at 345 °C for 1 hour in a 10 µtorr vacuum environment, then pressed together with a pressure of 1 MPa and heated above the eutectic temperature for 40 minu-tes using a SUSS MicroTec SB6e wafer bonder. Figure 3 shows the completed wafer, with an inset of a SEM image of a de-capped package showing the Pirani sensors. The pressures inside the cavities were all below 10 mTorr and have remained stable for over 2 years (See Figure 4). Silicon gold eutectic bonding is a mature solder wafer bonding process that produces high-yield, robust, and reliable vacuum packages.

DIFFUSION SOLDERING

Diffusion soldering is a relatively new, advanced type of solder bonding that combines the advantages of traditional solder bonding and solid-state diffusion bonding into a hybrid bonding technique that has interesting potential for MEMS vacuum packaging. It has the planarization capabilities of a traditional solder bond, but it can survive much higher temperatures than its formation temperature like a diffusion bond [2]. The bond is formed by interactions between a low melting point interlayer (usually tin or indium) sandwiched between two parent metals. The bond proceeds through four stages (Figure 5). First, all the metals are brought into contact. Second, the whole assembly is heated as quickly as possible to melt the interlayer. Once molten, the interlayer is rapidly consumed by the formation of intermetallic compounds with the parent metals. Third, the joint undergoes isothermal solidification as the last of the molten interlayer is transformed into higher melting point intermetallic compounds. Once the interlayer is consumed, the melting point of the joint has increased from the melting point of the interlayer to the lowest melting point of the resultant intermetallic compounds. There are many different combinations of parent metals with tin or indium (Table 2) [2]. Two related aspects of the design are very important to create high-quality voidless bonds. First, the interlayer must be thick enough so that it is not entirely consumed by intermetallic formation before it has a chance to melt; the heating rate plays an important role in determining this thickness [12].

Second, the heating rate during the second stage must be fast enough to reach the melting temperature before it is consumed. If the heating rate is too low, the low melting point interlayer could be completely consumed through solid-state intermetallic compound formation before the melting temperature can be reached. The minimum heating rate depends on the intermetallic compound formation rates, which vary widely for different material combinations, and the interlayer thickness, which can be accounted for with the design of the bond joint.

We have investigated the nickel-tin family of diffusion soldering as a

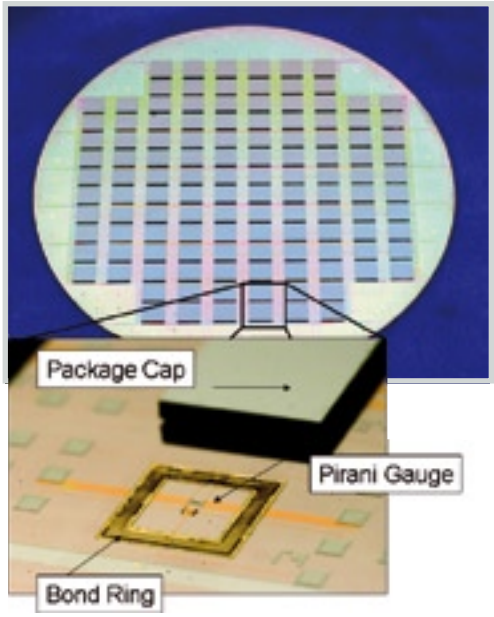


Figure 7:
Picture of a 4" wafer with nickel-tin diffusion soldered packages. The bottom picture shows an intentionally decapped package with the bond ring and Pirani gauge inside.

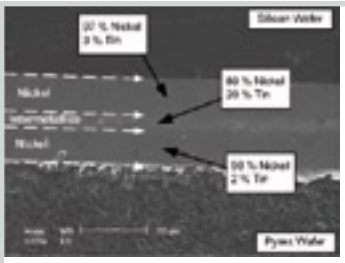


Figure 8:
Cross-sectional SEM view of a representative Ni-Sn-Ni diffusion solder bond.

Figure 9:
Plot of the pressures inside the Ni-Sn diffusion soldered packages vs. time.

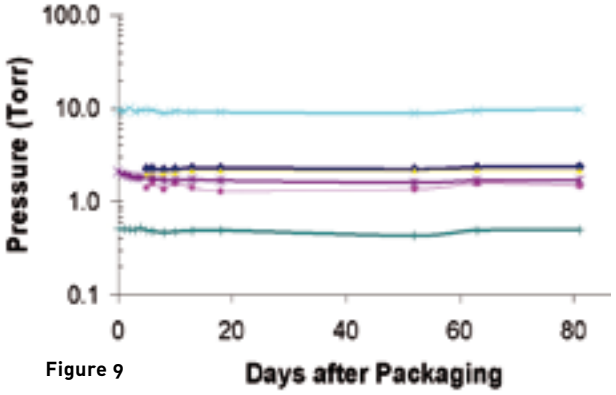


Figure 9

Figure 10:
Plot of the pressure inside one die subjected to extra thermal testing to demonstrate the thermal robustness of the diffusion soldered bonds.

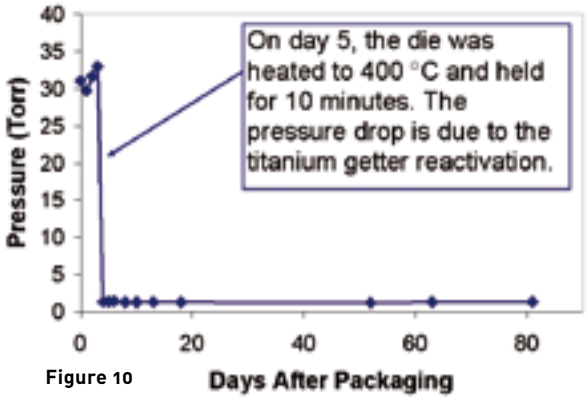


Figure 10

bonding technique for MEMS vacuum packaging [13]. The packaging process starts by sputtering a chrome/gold seed layer onto both wafers. Next, both wafers undergo two plating steps to create the 300 µm wide bond rings. Then the seed layer is etched on both wafers. Next, the cap wafer is thinned and a titanium getter film is sputtered onto it.

Figure 6 shows the cross section of the wafers prior to bonding. The wafers are heated to 300 °C at 60 °C/min using a SUSS MicroTec SB6e wafer bonder and held there for 1 hour. A compressive pressure of 100 kPa forces the wafers together (which creates a compressive pressure of 5 MPa at the bond rings). This compressive pressure serves two purposes. First, it ensures intimate contact between the bond rings across the wafer surface. Second, it helps the two electroplated tin layers wet one another by mechanically breaking the native oxide of each tin layer, which allows clean tin to come to the surface [2]. Figure 7 shows a picture of a completed wafer with a close up of a decapped package.

Figure 8 shows a SEM image of the cross section of a similar Ni-Sn diffusion soldered bond between a silicon and Pyrex wafer. The cross section shows a smooth void-free bond, with a high concentration of tin atoms in the center. The pressures inside the cavities were monitored with Pirani gauges; a representative sample is plotted in Figure 9.

The package pressures varied from 40 Torr to 200 mTorr across the wafer due to variances in outgassing and getter rates, but all of the pressures have stayed steady for several months. Finally, one of the unique features of diffusion soldering was tested. A package was measured for five days to establish a baseline pressure, then on day 5 it was heated to 400 °C for 10 minutes, afterwards the pressure was measured again (See Figure 10).

The baseline pressure was around 30 Torr but dropped to 1-2 Torr after the thermal test and has remained steady since then; indicating that Ni-Sn diffusion soldered bonds can maintain a hermetic seal at higher temperatures than their formation temperature.

CONCLUSION

Wafer bonding using solder is a very attractive technology for MEMS vacuum packaging. It can be done using a number of different material sets, with a range of melting temperatures. One of these techniques is based on diffusion soldering, which offers several advantages. The solder flows during the bonding process, enabling it to seal over electrical feedthroughs and other wafer non-planarities. The seals are made of metals and use process technologies that can be scaled, enabling narrower bond rings that will save expensive die area. All these advantages make it a likely candidate for industrial wafer bonded vacuum packaging; however some challenges remain to be solved. Material interactions and the fluxless requirement for solder bonding necessitate complicated bond joint designs that have not demonstrated the same reliability and reproducibility as glass frit. But with new solder research and process development, such as S SUSS MicroTec's C4NP process and ELAN CB8 wafer bonder, reliable wafer-level MEMS vacuum packaging with solder bonding is right around the corner.

In the near future, we are pursuing lower cavity pressures by investigating outgassing sources and investigating different material combinations, such as gold-indium.

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Warren Welch
received his B.S. in electrical engineering from Lehigh University in June 2001. During his time at Lehigh, he spent a summer at the Department of Energy's Princeton Plasma Physics Lab developing code to facilitate the visualization of scientific data. The following summer, he was part of the National Science Foundation (NSF) Research Experience for Undergraduates program at Lehigh's Sherman Fairchild Research Lab. At the lab, his work focused on reducing the number of oxide traps at the surface of a Silicon-Carbide MOS capacitor.
He enrolled at the University of Michigan in the fall of 2001 and received his master's degree in May 2003. In 2004, he was awarded the Outstanding Student Leadership Award for his efforts as part of the NSF Engineering Research Center for Wireless Integrated MicroSystems. He is currently pursuing his PhD research into applications of solder for vacuum and hermetic packaging of MEMS and plans to finish up in Fall 2007.

Jay Mitchell
received his B.S. and M.S. from Case Western Reserve University in 1999 and 2000, respectively. In 2000 and 2001, he worked for Movaz Networks in the testing and design of micromirrors for telecommunications applications. In the fall of 2002, he began the Ph.D. program at the University of Michigan in mechanical engineering and is currently working on various vacuum and low-temperature wafer-level packaging methods for MEMS and microsystems. Jay will finish his doctorate by the end of summer 2007 and is President and co-founder of ePack, a company providing MEMS packaging services and expertise.

Khalil Najafi
received the B.S., M.S., and the Ph.D. degree in 1980, 1981, and 1986 respectively, all in Electrical Engineering from the University of Michigan, Ann Arbor. From 1986-1988 he was employed as a Research Fellow, from 1988-1990 as an Assistant Research Scientist, from 1990-1993 as an Assistant Professor, from 1993-1998 as an Associate Professor, and since September 1998 as a Professor in the Solid-State Electronics Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan. His research interests include: micromachining technologies, micromachined sensors, actuators, and MEMS; analog integrated circuits; implantable biomedical microsystems; micropackaging; and low-power wireless sensing/actuating systems.
Dr. Najafi was awarded a National Science Foundation Young Investigator Award from 1992-1997, and has been active in the field of solid-state sensors and actuators for more than twenty years. He has been involved in several conferences and workshops dealing with micro sensors, actuators, and microsystems, including the International Conference on Solid-State Sensors and Actuators, the Hilton-Head Solid-State Sensors and Actuators Workshop, and the IEEE/ASME Micro Electromechanical Systems (MEMS) Conference. Dr. Najafi has served as the Editor for several journals, including the IEEE Transaction on Electron Devices, J. of Solid-State Circuits, Trans. On Biomedical Engineering, and is currently an Associate Editor for the IEEE *Journal of Micro Electromechanical Systems (JMEMS)*, the *Journal of Micromechanics and Microengineering*, Institute of Physics Publishing, and an editor for the Journal of Sensors and Materials. He is a Fellow of the IEEE and the AIBME.

UV nanoimprint materials: surface energies, residual layers, and imprint quality

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ABSTRACT

UV nanoimprint lithography is attracting more and more interest, because it has the potential of becoming a high-resolution, low-cost patterning technique. The availability of suitable UV curing materials is mandatory for successful imprinting. Within this work, a systematic investigation of commercially available photocuring materials was conducted to provide an over-view of the properties of these materials. Their wetting behavior with respect to different substrate surfaces was characterized and their surface tensions were determined from their contact angles against two specifically selected solid surfaces: This method is presented here for the first time. The adhesion properties of the UV curing materials to different substrate surfaces and to the mold were investigated and necessary curing times were estimated. Additionally, the dependence of the residual layer thickness on the viscosity and the initial dispensed volume of UV curing materials was analyzed. It was found that the resist formulation of the UV curing materials strongly influences the surface tension as well as the adhesion to different substrate surfaces. Furthermore, the experiments verified that the thickness of the residual layer for UV curing materials increases with the square root of their viscosity which is predicted by theory. To demonstrate the suitability of the UV curing materials, first imprints with the prototype imprint tool, Nano Patterning Stepper 300 from Süss MicroTec, with pattern sizes down to 50nm are shown.

Keywords: UV curing material, UV nano-imprint lithography, surface tension, contact angle, adhesion, residual layer thickness.

I. INTRODUCTION

UV nanoimprint lithography (UV NIL) is attracting more and more interest as a technique to transfer nanosized patterns without using expensive optical exposure tools [1]. The resolution of this technique is only limited by the availability of patterns that can be resolved on a mold [2] and the availability of an appropriate UV curing material.

This material has to fulfill several requirements such as low viscosity, low adhesion to the mold, good adhesion to the substrate, fast curing

		Viscosity μ (mPa · s)	UV curing time (s) at 30mW/cm² and 375nm
Dental UV sealants	Fissurit (Voco)	> 100	No curing
	Clinpro Sealant (3M ESPE)	> 100	No curing
	Helioseal (Ivoclar Vivadent)	70 – 75	100
UV glues	NOA 61 (Norland Optics)	300	20
	Z-Resist (96.5% t-butyl acrylate and 3.5% Irgacure 369)	12 – 14	> 5
UV NIL resists	Inoflex RP+ (Inomat GmbH)	100	> 5
	PAK 01 (Toyo Gosei)	50	> 5
	NIF 1 (Asahi Glass Company)	14.5	10
	NIF 2 (Asahi Glass Company)	24.5	10

Table I:
Viscosities and experimentally determined UV curing times for the evaluated UV curing materials.

	σ_{polar} (mN/m)	$\sigma_{dispersive}$ (mN/m)	σ_{total} (mN/m)
Teflon	< 0.05	27.5	27.5
Fused silica	94.7	< 0.05	94.7

Table II:
Surface tensions of Teflon and fused silica. The two solid materials were used to measure the surface tensions of the UV curing materials.

times, and high etch resistance to allow pattern transfer into the substrate. To achieve these properties, UV curing resist formulations are frequently acrylic based, but vinyl-ether-based or fluorinated-based materials have shown appropriate imprint properties as well [3-6]. As already mentioned, the adhesion properties of UV curing materials play an important role. For the evaluation of adhesion properties, the influence of the interface mold/UV curing material and substrate/UV curing material has to be investigated. To achieve a good adhesion of the UV curing material to the substrate, a very good wetting behavior and a good specific adhesion are necessary. The formation of a weak boundary layer has to be avoided.

A weak boundary layer occurs, when chain molecules of the resist are mainly bonded to the substrate surface during the adsorption and, therefore, are no longer available for bindings to other molecules in the resist. This leads to reduced cohesion forces between the substrate and the resist. A second reason for the formation of a weak boundary layer is the formation of gas voids in the case of a bad wetting behavior of the UV curing material to the substrate. This results in defects within the cured resist layer. For these reasons, an appropriate UV curing material with a good wetting behavior to a specific substrate has to be chosen. Within this work, different commercially available UV curing materials were investigated.

First, the contact angles of the UV curing materials to clean silicon (Si) substrates, Si substrates primed with hexamethyldisilizane (HMDS), and Si substrates covered with the anti reflective coating (ARC) DUV 112-6 from Brewer Science were measured. Secondly, the surface tension of the UV curing materials was determined by a method which is presented in this work for the first time. Thirdly, the adhesion properties of the UV cured materials to the three substrate surfaces and to the mold were inspected optically and compared.

Beside the investigations on the adhesion properties, the influences of dispensed volume and viscosity on the residual layer thickness (RLT) were analyzed and compared to theoretical predictions.

Finally, first UV nanoimprints with the prototype imprint tool Nano Patterning Stepper (NPS) 300 from SUSS MicroTec are presented to demonstrate the validity of the investigations.

II. EXPERIMENTAL SETUP

A. Imprint tool & experimental procedure

All imprints were performed using the imprint tool NPS 300 from SUSS MicroTec. The exposure wavelength of the UV light emitting diode array is 375nm and the power density can be ramped up to 120mW/cm².

For the experiments, a power density of 30mW/cm² was chosen to avoid an embrittlement of the UV curing materials. The UV curing materials were placed on the substrate surface manually using a pipette or automatically using a single drop dispenser just before starting the imprinting process. 200nl of the UV curing resists were placed manually in the center of the imprint site and the following investigations were performed:

- Estimation of the UV curing time for the UV curing materials.
- Evaluation of the adhesion properties for the UV curing materials to the substrate surfaces and to the mold.
- Verification of the theoretical predictions that the residual layer thickness increases with the square root of the viscosity of the UV curing material.

The single drop dispenser, where drops of the UV curing material are placed on substrate surfaces following a pattern predefined in the software of the imprint tool NPS 300, was used for (1) measuring the rsidual layer thickness for different volumes of UV curing material and demonstration of first imprints with the NPS 300.

For all imprints, a fused silica mold with a size of 12.5x12.5mm² and a surface roughness of less than 0.6nm rms was used.

The surface of the mold was modified with an antisticking layer [(tridecafluoro-1,1,2,2-etrahydrooctyl) trich-

	Contact angle (°)			
	Si	Si / HMDS	Si / ARC	Mold
NOA 61	23.7	41.8	n.i.	68.3
Helioseal	15	26.7	n.i.	66.2
Inoflex RP+	14.9	31.9	8	67.9
PAK 01	9.4	20.3	8.7	66.5
NIF 2	16.3	12.3	6.1	33.7
NIF 1	15.8	11.4	5.9	34.2
Z-Resist	6.3	25.8	10.6	65.4

Table III:
Contact angles of the evaluated UV curing materials for the three substrates and the mold. (n.i.: not investigated).

	Si	Mold	Si/HMDS	Mold	Si/ARC	Mold
Helioseal	++	--	n.i.	n.i.	n.i.	n.i.
Inoflex RP+	+	-	0	0	++	--
PAK 01	++	--	++	--	++	--
NIF 2	--	++	0	0	++	--
NIF 1	--	++	0	0	++	--
Z-Resist	++	--	-	+	--	++

Table IV:
Summary of the adhesion properties of UV curing materials after the separation of the mold from the cured resist. If the entire resist stuck on the substrate after the separation it is displayed with "++". If the resist stuck on the substrate to about 80%, 60%, 40%, and less than 40%, it is described with "+", "0", "-", and "--", respectively (n.i.: not investigated).

lorosilane] to provide a low surface tension and to allow a defect free demolding from the cured material.

During the imprinting process, the mold was pressed into the UV curing material following a predefined force profile. When the force reached its maximum level of 20N, the material was cured by an UV exposure. After curing, the mold was separated from the material again.

For the determination of the residual layer thickness, the resist thickness of every imprint was measured at 24 points with a KLA Tencor P-2 long scan profilometer. The contact angles of the UV curing materials with the substrates were measured with a KRUSS G-1 drop shape analyzer. From these meas-urements, the surface tensions of the UV curing materials were calculated.

B. UV curing materials

Nine commercially available UV curing materials were investigated ranging from dental UV sealants and UV glues to dedicated UV NIL resists. The UV curing materials distributed by Molecular Imprints like e.g. MonoMat™ were not available at the time of this work. The evaluated resists and their main properties are summarized in Table I. The UV curing times for an UV intensity of 30mW/cm^2 were determined experimentally. The UV curing times range from less than 5s for the Z-Resist, Inoflex RP+, and PAK 01 to no curing after 2 min for Fissurit and Clinpro Sealant. The UV resists, Fissurit and Clinpro Sealant, which did not show any curing after 2 min, were not considered for further investigations.

The dental UV sealants Fissurit, Clin-pro Sealant, and Helioseal were obtained from VOCO, 3M ESPE, and Ivoclar Vivadent, respectively. The UV glue NOA 61 was provided by Norland Optics and Z-resist was a homemade mixture from t-butyl acrylate (96.5%) and the photoinitiator Irgacure 369 (3.5%) from CIBA. UV NIL resists Inoflex RP+ and PAK 01 were obtained by Inomat GmbH and Toyo Gosei, respectively. NIF 1 and NIF 2 are products of Asahi Glass Company.

C. Determination of the surface tension of UV curing materials by contact angle measurements

To characterize the wetting behavior of solid surfaces, the measurement of the contact angle and the calculation of the surface tension are widely used. The surface tension (σ) is separated in a polar (σ^P) and a dispersive part (σ^D), where the polar part describes the hydrophilic character and the dispersive part the hydrophobic character of a surface.

For the calculation of the surface tension for solids, droplets of different liquids with known surface tensions are brought into contact with the solid surface under test. The interaction between the molecules in the liquid, the vapor phase, and the molecules on the substrate surface results in a droplet with an individual shape. The contact angle can be measured at the triple point liquid/solid/vapor phase. If there is a strong interaction between liquid and solid, a small contact angle occurs. A small contact angle means good wetting behavior and this is a prerequisite for a good adhesion [7]. Beside the chemical interaction, also the mechanical interation influences the contact angle requiring a surface with a defined and homogeneous roughness for reproducible measurements.

The measurement of the surface tension for liquids is quite different. A tensiometer is typically used to determine the dispersive and polar parts of the surface tension by the ring or plate method [8, 9]. In the following, a method will be presented for the first time to calculate the surface tension of liquids by measuring the contact angle of a liquid against two different solid surfaces. The advantage of this new method is that the surface tension of both, solids and liquids, can be measured with one conventional contact angle measurement tool. For this method, it is of great importance that the two solid surfaces are of high mechanical quality, e.g. that they have an optically polished surface to minimize influences of surface roughness. The calculation of the surface tension for the UV curing materials is based on the equation introduced by Owens and Wendt [10].

Here, σ_{sl} is the surface tension between the solid and the liquid material, and σ_s and σ_l are the surface tensions for the solid and the liquid material, respectively. The superscripted indices

D and P describe the dispersive and polar parts of the surface tension.

Combination of *Eq. (2)* with Young's *Eq. (3)* [11], where Θ describes the contact angle at the triple point solid/liquid/vapor phase, results in the following *Eq. (4)*.

If both the polar part of the surface tension of a first solid material and the dispersive part of the surface tension of a second solid material are neglectable, *Eq. (4)* can be reduced to the following *Eqs. (5)* and *(6)*.

Indices 1 and 2 describe the first and the second solid material, respectively. ν_1 and ν_2 are introduced to reduce the complexity of the following equations.

For calculating the dispersive part of the surface tension for the UV curing materials, *Eqs. (5)* and *(6)* have to be combined. The polar part of the surface tension of the liquid can be calculated from *Eqs. (7)* and *(4)*.

As already mentioned, one solid surface has to be a polar surface and the other a dispersive surface, respectively.

The dispersive surface used was optically polished Teflon with a dispersive surface tension of 27.5mN/m and a polar surface tens on below 0.05mN/m. The polar surface used was fused silica (Lithosil L1 from Schott Lithotec) with a polar surface tension of 94.7mN/m and a dispersive surface tension below 0.05mN/m. The corresponding values are summarized in Table II.

III. RESULTS & DISCUSSION

A. Adhesion properties of UV curing materials

To achieve a good adhesion, a good wetting behavior of UV curing materials to solid surfaces is necessary but not sufficient. A good wetting behavior is obtained when the contact angle is small. In Table III, the contact angles of the evaluated UV curing materials for Si substrate, Si substrate primed with HMDS, Si substrate covered with an ARC, and the mold are summarized. In every case, the contact angles of the UV curing materials to the substrates are smaller than to the mold indicating a better adhesion of the UV curing materials to the substrates than to the mold.

In Table IV, the adhesion properties of the UV curing materials after the separation of the mold from the cured resist are summarized. After the imprint, the whole imprinting area on the substrate was inspected with an optical microscope and categorized. The entire resist stuck on the substrate after the imprint, when the combination substrate/resist is described in Table IV with "++". If the resist stuck on the substrate to about 80%, 60%, 40%, and less than 40%, it is described with "+", "0", "-", and "--", respectively. The resists Helioseal, PAK 01, and Z-Resist showed very good adhesion properties to the clean Si substrate surface. Priming of the Si substrate with HMDS resulted in a reduced adhesion for the resists Inoflex RP+ and Z-Resist. UV curing materials Inoflex RP+, PAK 01, NIF 1, and NIF 2 showed very good adhesion properties to the Si substrate covered with an ARC.

Between the Si substrate and the resists NIF 1 and NIF 2, no adhesion was observed. This arises from the chemical formulation of these resists. They consist of a content of approximately 65% of fluorinated compounds. These fluorinated compounds decrease the specific adhesion to Si substrates. The resist Inoflex RP+ contains about 5% of fluorinated compounds. This amount is already sufficient to decrease the adhesion to Si substrates significantly.

In Table V, the surface tensions of the evaluated UV curing materials determined with the new method described in Sec. II C are shown. The resists Helioseal, Inoflex RP+, PAK 01, and Z-Resist show nearly the same values for their surface tensions.

All these resists have an acrylic-based resist formulation. The resists NIF 1 and NIF 2 show a reduced surface tension resulting from the fluorinated compound resist formulation.

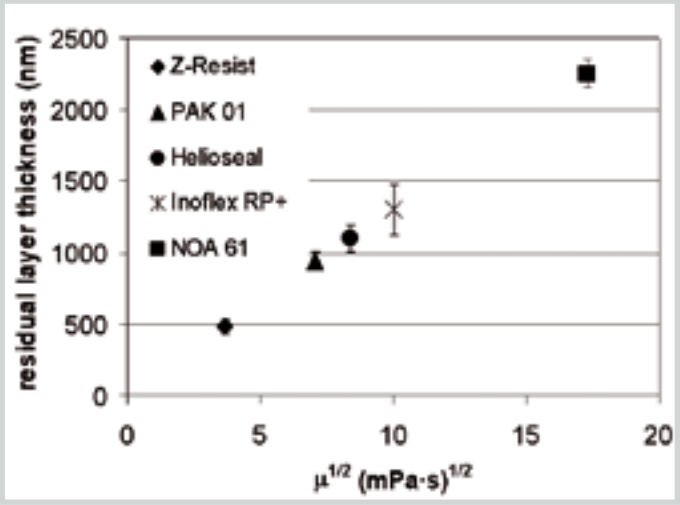

Figure 1:
Residual layer thickness for the UV curing materials.

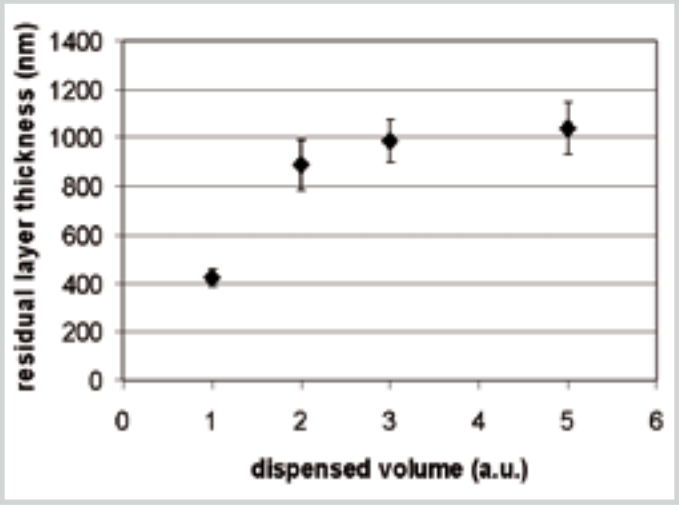

Figure 2:
Residual layer thickness for different dispensed resist volumes. The used resist was PAK 01.

(Eq. 1)

$$\sigma = \sigma^P + \sigma^D$$

(Eq. 2)

$$\sigma_{sl} = \sigma_s + \sigma_l - 2 \cdot \sqrt{\sigma_l^D + \sigma_s^D} + 2 \cdot \sqrt{\sigma_s^P + \sigma_l^P}$$

(Eq. 3)

$$\sigma_s = \sigma_{sl} + \sigma_l \cdot \cos \Theta$$

(Eq. 4)

$$\sigma_l \cdot (1 + \cos \Theta) = 2 \cdot \sqrt{\sigma_l^D + \sigma_s^D} + 2 \cdot \sqrt{\sigma_l^P + \sigma_s^P}$$

(Eq. 5)

$$\frac{1 + \cos \Theta}{2 \cdot \sqrt{\sigma_{sl}^D}} = \frac{\sqrt{\sigma_l^D}}{\sigma_l^P + \sigma_l^D} = \upsilon_1$$

$$\Rightarrow \sigma_l^P = \frac{\sqrt{\sigma_l^D}}{\upsilon_1} \sigma_l^D$$

(Eq. 6)

$$\frac{1 + \cos \Theta_2}{2 \cdot \sqrt{\sigma_{s2}^P}} = \frac{\sqrt{\sigma_l^P}}{\sigma_l^P + \sigma_l^D} = \upsilon_2$$

(Eq. 7)

$$\sigma_l^D = \upsilon_1^{-2} \cdot \left[\left(\frac{\upsilon_2}{\upsilon_1} \right)^2 + 1 \right]^{-2}$$

(Eq. 8)

$$\sigma_l^P = \upsilon_1^{-2} \cdot \left\{ \left[\left(\frac{\upsilon_2}{\upsilon_1} \right)^2 + 1 \right]^{-1} - \left[\left(\frac{\upsilon_2}{\upsilon_1} \right)^2 + 1 \right]^{-2} \right\}$$

(Eq. 9)

$$t_f = \frac{\mu \cdot s^2}{2 \cdot p} \cdot \left(\frac{1}{h_f^2} - \frac{1}{h_0^2} \right)$$

(Eq. 10)

$$h_f = \sqrt{\frac{s^2}{2p \cdot t_f}} \cdot \sqrt{\mu}$$

$$\Rightarrow h_f \sim \sqrt{\mu}$$

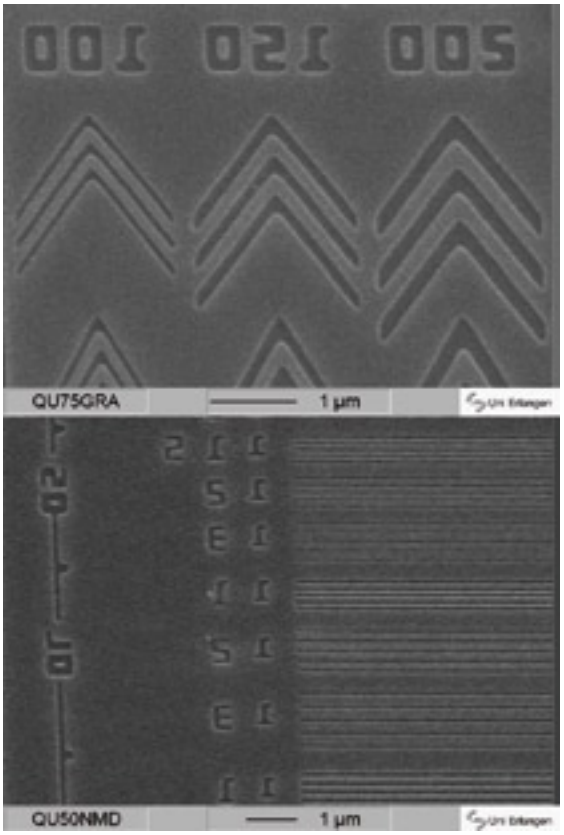

Figure 3:
SEM images of first UV nanoimprints with the imprint tool NPS 300. On the upper image, pattern sizes from 100nm to 200nm, and on the lower image, pattern sizes from 50nm to 70nm are transferred into PAK 01.

B. Residual layer thickness

The formation of a residual layer during the imprinting process is unavoidable. To minimize the thickness of the residual layer is of great importance because the layer has to be removed by a plasma etching process prior to the pattern transfer into a substrate. The plasma etching process results in a loss of dimensional accuracy and has to be minimized. The time to reach the final residual layer thickness can be calculated by the following *Eq. (9)* [12].

Here, t_f is the imprinting time, h_0 and h_f are the initial and the final resist thickness, respectively, p is the imprinting pressure, and s is the distance the resist flows, and μ is the viscosity of the resist. Within this work the influence of the parameter viscosity and initial resist volume on the residual layer thickness was investigated. In case of the initial thickness being much higher than the final thickness, *Eq. (9)* can be reduced to the following *Eq. (10)*.

To assure that the initial thickness is much larger than the final thickness, 200nl of resist were dispensed using a pipette on a Si substrate just before the imprinting processes started. With this method, the initial thickness was about a factor of 100 higher than the final thickness. The mold used did not have patterns on it to assure reproducible imprint conditions.

In Figure 1, the residual layer thickness is shown for the UV curing materials Z-Resist, PAK-01, Helioseal, Inoflex RP+, and NOA 61. The residual layer thickness increases with the square root of resist viscosity as predicted in *Eq. (10)*. With higher viscosities, the homogeneity of the residual layer decreases because of the reduced flow of the highly viscous resist. In order to determine the influence of the initial dispensed volume on the residual layer thickness, in principle, resists with the lowest viscosities should be used as well as a dispense system to generate uniform drops with small volumes that cannot be realized manually with a pipette. As the dispense system currently used is not capable to process liquids with very low viscosities, the resists NIF 1 and Z-Resist, best suited for this kind of experiment, could not be used. Instead, the resist PAK 01 was used. The resist was placed on a Si substrate using the single drop dispenser following a predefined pattern that covers the whole imprinting area just before the imprinting cycle starts. The amount of resist was increased by dispensing the pattern one, two, three, and five times, respectively. The resulting residual layer thickness after the imprinting cycle was measured with a KLA Tencor P-2 long scan profilometer.

In Figure 2, the resulting residual layer thickness for different volumes of PAK 01 is shown. The resulting residual layer thickness increases with a factor of about 2.5 when dispensing the pattern more than one time. The minimum residual layer thickness achieved for the resist PAK 01 was 400nm which is not sufficient for a feasible pattern transfer of nano-sized patterns into a substrate. We estimate that the residual layer thickness can

	σ_{polar} (mN/m)	$\sigma_{dispersive}$ (mN/m)	σ_{total} (mN/m)
Helioseal	16.1	24	40.1
Inoflex RP+	16.6	24.2	40.8
PAK 01	15.6	23.5	39.1
NIF 2	4.8	17.4	22.2
NIF 1	4.8	17.4	22.2
Z-Resist	14.8	23.3	38.1

Table V:
Surface tension of the evaluated UV curing materials.

be reduced to a feasible value of less than 100nm by using a patterned mold in combination with a low viscosity resist such as NIF 1.

C. First imprints

To demonstrate the capability of the imprinting tool NPS 300 and the validity of the investigations, first imprints into the UV curing material PAK 01 were performed. The resist pattern mentioned above was dispensed one time on a Si substrate and the curing time was 5s at 30mW/cm^2. After the separation of the mold from the cured resist, no resist stuck on the mold and no defects were observed. In Figure 3, scanning electron microscopy (SEM) images demonstrate the successful transfer of different patterns into the UV NIL resist PAK 01. The minimum resolved pattern size shown on the lower image of Figure 3 was 50nm and was limited by the size of the patterns on the mold. The successful imprints demonstrate the capability of the imprint tool NPS 300.

IV. CONCLUSION

Within this work, different commercially available UV curing materials were investigated. Their contact angles to different substrate surfaces were measured and their surface tension was determined with a method presented here for the first time. The adhesion properties of the UV curing materials to different substrate surfaces and to the mold were discussed and their curing times were determined.

Additionally, the dependence of the residual layer thickness on the viscosity and the initial dispensed volume of UV curing materials was demonstrated. It was found that UV curing materials that consist in parts of fluorinated compounds do not show appropriate adhesion properties to Si substrates or to Si substrates primed with HMDS. The use of an ARC on the Si substrates results in an appropriate specific adhesion and, therefore, in acceptable adhesion properties. Except of the Z-Resist, all investigated UV curing materials show a very good adhesion to the Si substrate covered with an ARC. For the Z-Resist, a clean Si surface shows the best adhesion property. The dependence of the residual layer thickness on the viscosity and the initial dispensed volume was demonstrated. Theoretical predictions that the resi-dual layer thickness increases with the square root of the viscosity of the resist could be approved.

Finally, first UV nanoimprints with the tool NPS 300 could be successfully demonstrated.

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Topics: Semiconductor technology, template fabrication, imprint process development, UV polymer characterization, inspection.

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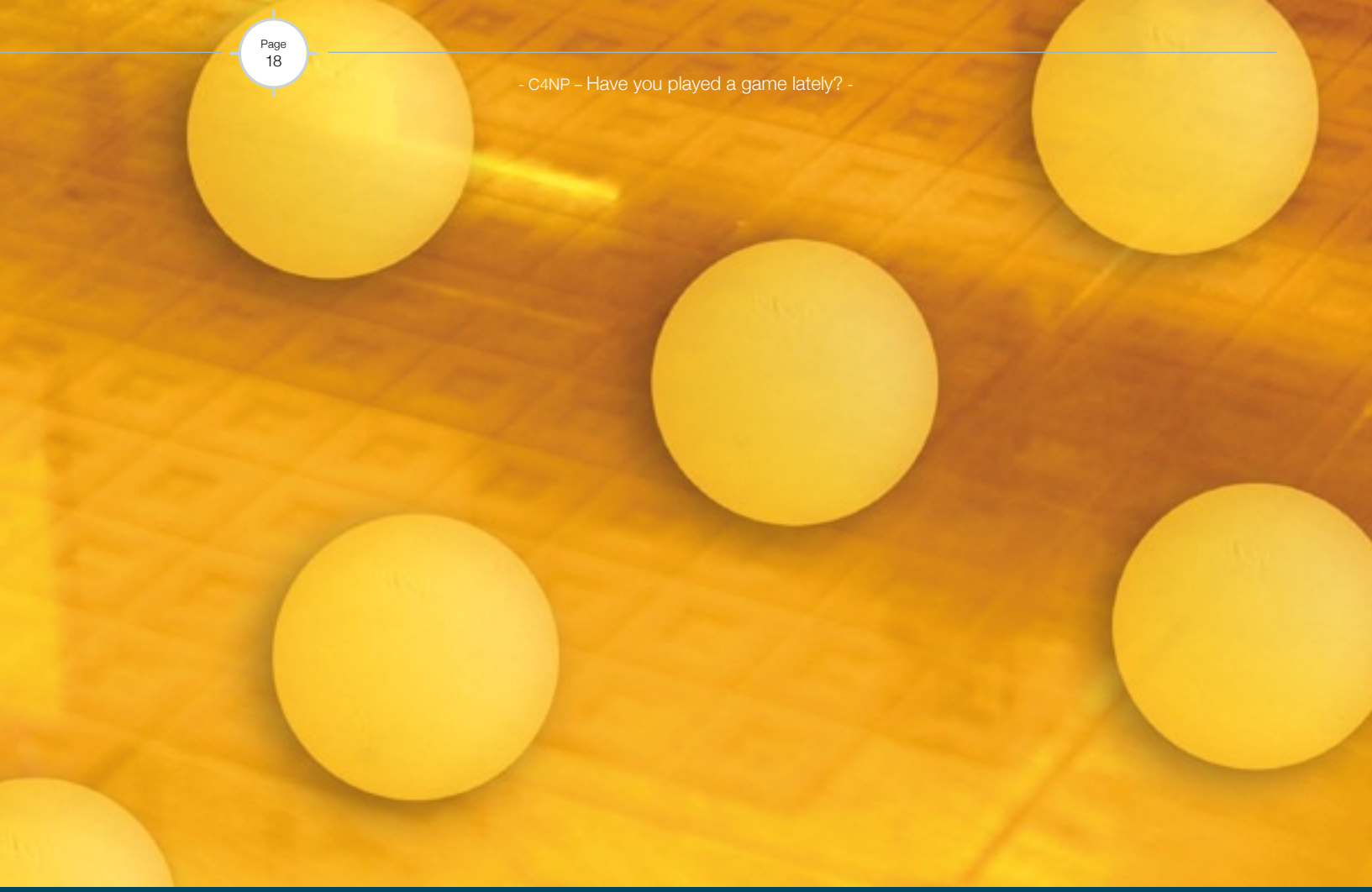

How C4NP and other SUSS Technologies affect us all

Klaus Ruhmer & Emmett Hughlett, SUSS MicroTec, Inc.

Have you played a game lately?

Each of us has played video games before. Be it at an amusement park arcade or in our own living rooms – video games have been one of the early "killer" applications for computer systems. Some of us still remember the early "Tennis" TV game. A controller allowed sliding a racket (white bar) up and down oneside of the screen. A little white square dot represented the ball, bouncing back and forth from one side of the screen to the other. Later on in the early 1980's, more advanced computer systems such as the Commodore 64 or the Atari became widely used mainly due to the variety of games available for them. Some may remember going through several joysticks by playing games like "Summer Olympics". Graphics and sound were relatively sophisticated by then.

But what about the 21st century? The video game technology of today is truly amazing. Consoles like the Nintendo® Wii, Sony PlayStation3 or Microsoft XBOX360 are pushing the limit of technology once again. Lifelike and real-time graphics, 3D sound and novel game controller technology require highly sophisticated electronic and MEMS (Micro Electro Mechanical Systems) components. In addition, game consoles are bought by "average" consumers. They have to be inexpensive, small, quiet, energy efficient and last but not least environmentally friendly. Or in other words, "lead-free".

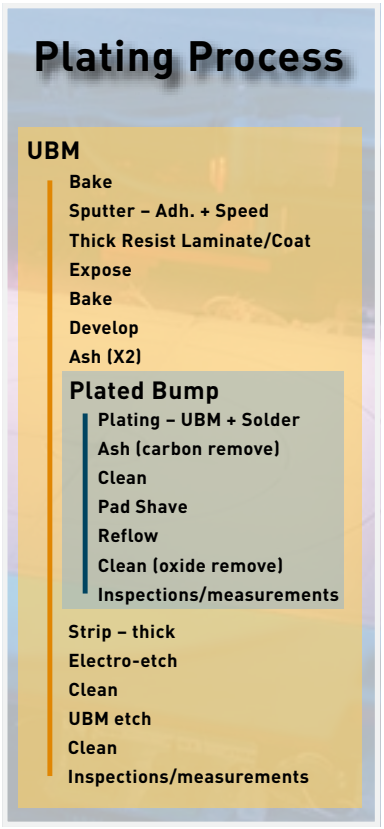

Figure 2:
Integrated UBM-BUMP process flow

An interesting fact about today's leading gaming platforms is that they are all based on IBM processor technology. For example, SONY's PS3 is powered by one of the most powerful chips available today, an 8-core IBM microprocessor (Cell processor) with over 230 million transistors Microsoft's XBOX360 and Nintendo's Wii also have "hearts" from IBM. A 3-core cell processor for the XBOX and a custom processor called "Broadway" for the Wii. In addition to mind-boggling processing and graphics performance, these game platforms also utilize unique game controllers. Nintendo has been able to outsell SONY and Microsoft largely due to its motionsensitive controller. EMS based accelerometers and gyroscopes make it possible for the computer to sense the actual motions of the player. Virtual but almost real Tennis, Bowling, Baseball or Football is the result.

SUSS MicroTec has had a lasting effect on many enabling technologies but especially on Advanced Packaging and MEMS. SUSS lithography tools, wafer bonding systems and MEMS probers are being used at MEMS fabs all around the world to manufacture those "motion sensing" chips referenced above. Again, SUSS lithography

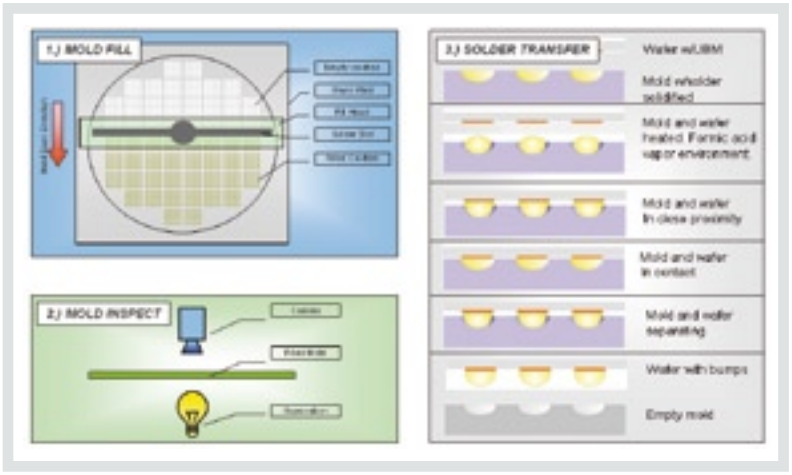

Figure 1:
3 main process steps for C4NP: Mold Fill – Mold Inspect – Solder Transfer

tools such as coaters, mask aligners and developers are performing critical process steps necessary for flip chip wafer bumping and wafer level redistribution, two main aspects of advanced packaging.

Nintendo® Wii Teardown

Source: Semiconductor Insights, 2006

In order to stay ahead on the technology curve, SUSS decided in late 2004 to engage into a Joint Development Agreement (JDA) with IBM to develop the necessary equipment for the next generation wafer bumping technology called C4NP. IBM originally pioneered the C4 (Controlled Collapse Chip Connection) process in the 1960's. An evaporation process was used to deposit solder onto a wafer through a mask. Subsequent reflow in combination with surface tension of liquid solder created the desired solder balls or spheres. Since then, the C4 process has been modified and optimized. Currently, the most common way of creating fine-pitch C4's for flip-chip applications is electro-plating of solder. Instead of a physical mask, a photo-lithography step using thick resist and broadband exposure is used to create a "soldemask" or "solder

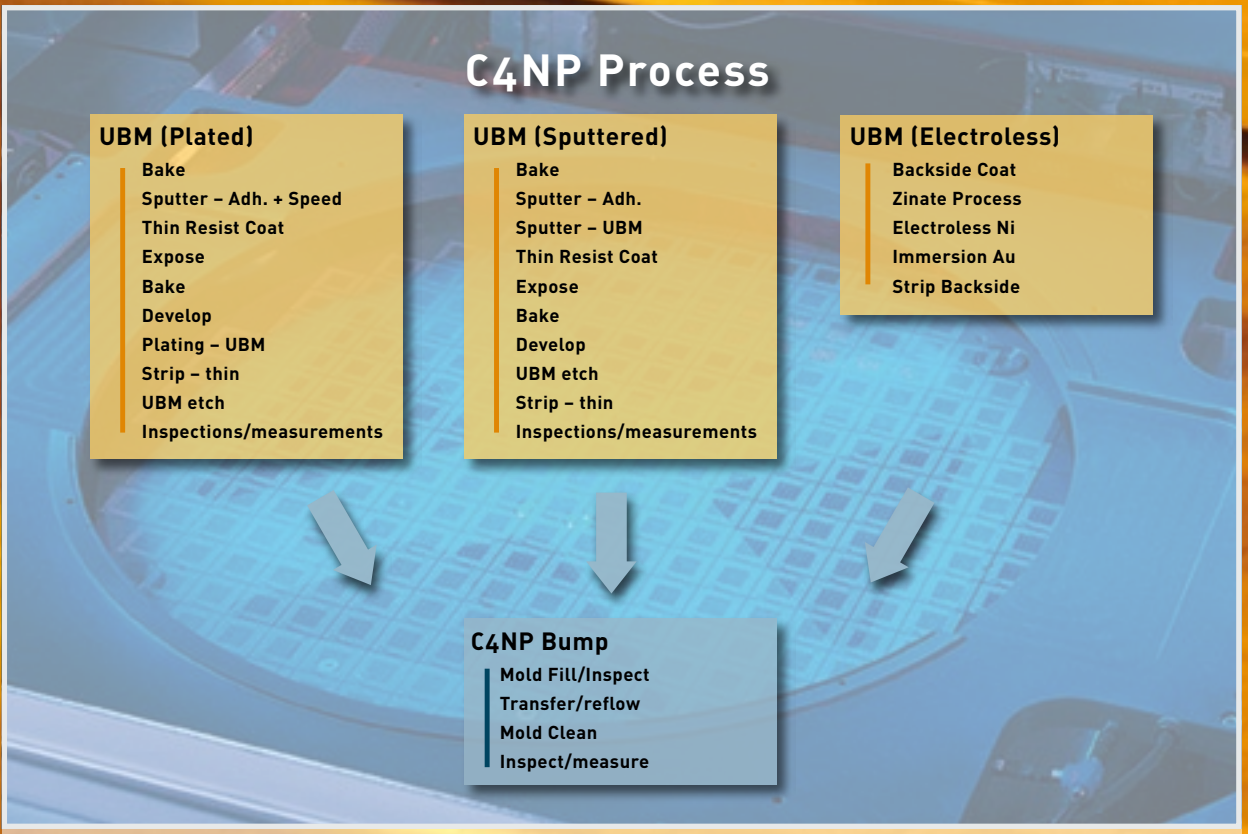

Figure 3: UBM variety in conjunction with C4NP solder deposition method

mold" on every wafer. One could call it a disposable solder mold.

After the solder is deposited using electro-plating, the photo solder mold is removed (chemically stripped) and washed down the drain. Electro-plating of solder has come a long way and has reached a high level of maturity enabling excellent bump yields. IBM's new C4NP process addresses some key deficiencies of the current state-of-the-art bumping-method. It reduces cost by utilizing a solder mold made out of glass instead of photo-resist. The glass molds are reuseable for hundreds of wafers and don't have to be created and disposed of for every single wafer. The solder is used in its bulk form (melted) and therefore very inexpensive. Alternatively, electro-plating of solder requires relatively expensive plating chemistry which in turn requires significant infrastructure to deal with the chemicals, all resulting in very high per wafer cost. However, the single biggest advantage of C4NP may be its ability to deposit any solder alloy onto any UBM (Under Bump Metallurgy). This is a huge benefit, which may ultimately be the real reason why the technology leader has adopted C4NP as the method of choice for flip-chip solder bumping. Future generation high-end logic chips such as microprocessors or graphics processors built on 45nm and 32nm process technology, will re-

Cost Factor	Comment
Personnel cost	Operators, Engineers, Management, Administrative overhead
Consumable and material cost	Bulk solder, glass molds
Equipment maintenance and support	Equipment engineering, scheduled downtime
Equipment depreciation	Function of capital required
Building overhead	Function of footprint and clean-room quality required
Wafer yield	Function of process complexity, number of process steps
NRE cost per part number/bump pattern	Function of mask cost, mold cost, number of uses per mold, number of molds required
Chemistry supply	Function of solder composition and method of deposition
Waste treatment	Function of chemistry used
IP cost/IP wafer toll	Function of IP ownership

Figure 4: Cost factors for wafer bumping line

quire new interconnect materials in order to meet the steadily increasing needs regarding reliability, current carrying ability, heat dissipation and more. C4NP allows IBM to develop and deposit these new materials. In contrast, solder electro-plating technology for lead-free currently limits the alloy to SnAg. The world's largest microprocessor manufacturer (Intel) announced recently that their solder of choice for flip-chip interconnection is going to be SnAgCu – a ternary alloy which can not be plated easily.

How does C4NP work?

The C4NP process starts with a glass mold in which the bump pattern for an entire wafer is replicated as a mirror image of cavities in the mold. These cavities are filled with solder as the mold is scanned below a fill head. The fill head contains a reservoir of molten solder and a slot through which the solder is injected into the mold cavities.

The cavity geometry determines the volume of the solder bumps that will be subsequently formed on the wafer. The filled mold is inspected automatically and then aligned below a wafer with exposed UBM pads facing the mold. Mold and wafer are heated above the solder melting point and then brought into contact. The solder forms spherical balls which transfer from the mold to the UBM regions on the wafer, where they preferentially wet and solidify. Wafer and mold are separated, and the mold is cleaned for reuse.

What about cost?

There are two main aspects contributing to the per wafer cost of a lead-free solder bumping process: the cost to create the UBM stack and the cost of building the bump by depositing solder. Prior to C4NP, the most widely used manufacturing process for lead-free flip chip solder bumping was based on electroplating of both, part of the UBM stack as well as the solder, using a single lithographic layer for patterning. This sequence makes it difficult to draw a line between UBM and bump formation as shown in Figure 2.

The C4NP process is significantly different as it decouples UBM and bump formation entirely. The UBM stack is formed using any variety of UBM processes. The bumps are formed using the C4NP process sequence. Figure 3 illustrates the UBM flexibility in combination with C4NP solder deposition.

This fundamental difference in process sequences manifests itself not only in per-wafer cost but also in non-cost related distinctions such as cycle time and process logistics.

The per wafer cost for production wafer bumping is a function of the following cost determining factors: personnel cost, consumable and material cost, equipment maintenance and support, equipment depreciation, building overhead as it relates to equipment footprint and cleanroom requirements, wafer yield, NRE cost per part number or bump pattern, chemistry supply, waste treatment and IP cost. A sophisticated cost model has been developed to investigate the impact of UBM cost on the overall per wafer bumping cost and to model the cost differences of the various UBM process methods described in this paper. Integrated Device Manufacturers (IDM) as well as bumping service providers has largely implemented some version of a plating process as described in Figure 2. Assumptions were made as to the type of equipment used, its footprint and facility requirements as well as its capital cost and throughput. Data from several leading equipment suppliers and IDMs formed the basis for this model.

The results show that the UBM-BUMP cost ratio is approximately 2:1. In other words, over 60% of per wafer cost in a typical plated bumping line is driven by the cost of the UBM. This ratio obviously depends on the specifics of the process sequence as well as the type of equipment used. By running the model under varying assumptions, the UBM-BUMP cost ratio ranged from 61%:39% to 75%:25%. From a process perspective, electroplating and photo lithography and their associated cost contributions had the biggest impact on overall per wafer bumping cost.

Figure 5: Total per-wafer cost

The results of modeling a typical wafer bumping line show that reducing the UBM cost will have the largest impact on overall per wafer cost. Unlike a plated bumping line, C4NP bumping technology enables the use of alternative, lower cost UBM process se-quences as outlined in Figure 3. This work focuses on the evaluation of a sputtered TiW/Ni UBM as well as an electroless Ni/immersion Au UBM which does not involve sputtering. No electroplating technology was utilized.

Figure 5 illustrates the per wafer bumping cost results based on the various models. The cost numbers have been normalized in order to show the differences in the various pro-

cesses without disclosing sensitive or proprietary information from tool and materials vendors. Furthermore, the absolute cost numbers also vary significantly based on regional parameters such as personnel and building cost. For the purpose of a cost comparison, a normalized view eliminates the effect of those parameters. The models were based on 300mm wafers with lead-free solder cost parameters.

A traditional plated bumping line ("Plating UBM and Bump") was modeled as the 100% reference. In comparison, the C4NP bumping line when used with a plated UBM ("Plated UBM+C4NP") resulted in a 16% reduction in overall bumping cost. Eliminating electroplating all together by replacing the UBM process with an all sputtered metal stack ("Sputtered UBM+C4NP") further reduced the per-wafer cost. The total cost is down to 74% compared to a traditional plated bumping line. The model for electroless Ni/immersion Au UBM ("ENIG UBM+C4NP) in combination with C4NP solder deposition showed the biggest impact on cost. The total per-wafer cost is reduced to 38% compared to the per-wafer cost of an electroplating bumping line.

The achievable cost reduction by utilizing a non-electroplated UBM in combination with C4NP is significant. The reduced cost is mainly driven by the elimination of electroplating and the reduced or eliminated use of photo lithography. Of course, each UBM construction must be evaluated to determine if it meets the reliability requirements for a given application.

SUSS C4NP Status

Since SUSS' engagement with IBM on the C4NP JDA, the program has come a long way. Manufacturing equipment has been ordered by IBM, designed and built by SUSS and installed earlier this year at IBM's Hudson Valley Research Park bumping facility. IBM has qualified C4NP for many of their products. Production has started.

At the same time, IBM and SUSS are continuing the JDA to further enhance the technology. ULCOAT has been qualified as a commercial mold supplier and is providing high-quality molds. One additional mold supplier should be qualified by the end of 2007.

For upcoming process generations (45nm, 32nm, etc), C4NP is IBM's recommended lead free bumping method. With strong partnerships between IBM and companies such as AMD, Free-scale, Toshiba, Sony, Infineon, Samsung, Chartered and AMKOR, SUSS is optimistic that C4NP will be widely adopted for high-end lead-free wafer bumping applications.

With all of that, please put this article down, get with your kids or friends and play a game of football on your Nintendo Wii using SUSS MicroTec technology.

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has global Sales & Marketing responsibility for C4NP wafer bumping technology at SUSS MicroTec. He has been with SUSS since 1998 starting out as an Applications Engineer for their wafer bonding and lithography products. Over the years, he has held various technical and sales related positions within SUSS. Prior to his current position, Klaus was responsible for Strategic Accounts in North America., Klaus is a native Austrian and holds a BS in Electronics and Telecommunications Technology. He came to the US in 1996.

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A Robust Broadband Calibration Method for Wafer-Level Characterization of Multiport Devices

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ABSTRACT

This paper describes the theory and practical results of the new multiport calibration procedure especially suited for wafer-level device characterization over a wide frequency range. An analysis of the currently available multiport calibration approaches was carried out. The advantages and drawbacks of each approach are demonstrated. It is shown that a robust wafer-level multiport calibration procedure should combine the strengths of both 7-term and 10-term based algorithms. It should also provide reference-match measurements on each VNA measurement port and be insensitive to the behavior of highly-reflective standards and the design of transmission standards.

Corresponding to these requirements, the definition of the advanced multiport RRMT+ algorithm is given. The results of a practical experiment proved the theory and demonstrated the advantages of the new multiport RRMT+ calibration procedure.

I. INTRODUCTION

The progress in wireless technologies and high-frequency broadband applications, the requirements for low power consumption, reduced electromagnetic interferences, increased sensitivity, and data transfer rates drive the development of high-frequency, multiport mono- and mixed-mode devices, and thus improvement of multiport measurement systems. As an example, the first 4-port 40 GHz vector network analyzer (VNA) based on a true $2n$-receivers concept has been recently reported [1]. The hybrid multiport systems already provide 4-port measurement capability up to 67 GHz [2, 3]. The expansion of the frequency range of multiport VNAs requires new approaches for their calibration, particularly for wafer-level applications.

Many different calibration procedures were developed and implemented in commercial VNAs in the past. These can be separated into two groups based on the 10-term or 7-term model. 10-term approaches can be used for low-end VNAs (with n+1 measurement receivers, where n is number of VNA ports) and demonstrate the highest potential calibration dynamic range [4]. However, the requirement to have either ideal of fully known calibration standards significantly limits the application of these procedures. Therefore, it is not recommended to use 10-term based calibrations for wafer-level measurements beyond 20 GHz.

Many 7-term procedures are not sensitive to the non-ideal calibration standards short and open. Variants of these procedures (such as 2-port and multi-

Figure 1: Configuration of thru standards for a 4-port wafer-level calibration: straight thrus (port 1 – port 2, port 3 – port 4), loop-back thrus (port 1 – port 3, port 2 – port 4), cross-over thrus (port 1 – port 4, port 2 – port 3).

port TRL[1], LRM[2], SOLR[3], LRM+[4], or TXX for general) are widely used for the calibration of broadband wafer-level measurement systems [5-8, 10, 12-14,].

However, as it was reported in [10], potential limitation of the calibration dynamic range of the 7-term-based methods may reduce the measurement accuracy, especially for differential devices under high-rejection conditions.

Additionally, multiport TXX-procedures may lead to significant calibration errors in the following cases (typical for many wafer-level setups):

- partly-known reflection (R) standards are not symmetrical (for instance, when measuring at a packaged-level);
- the rectangle, loop-back, or cross-over thru (Fig. 1) introduces a resonance at certain frequencies within the measurement range;
- the open, short, and load standards are not ideal or insufficiently modeled (for SOLR-like procedures)
- the load standard is not purely resistive and its impedance is frequency dependent;
- the load impedance is asymmetrical;

Therefore, it is necessary to develop a new multiport calibration procedure that will be free of the mentioned limitations.

The next chapter of this paper briefly describes the multiport measurement system and discusses different calibration approaches. Then, the novel generalized RRMT+ is introduced and experimental results verifying the application of this method are presented.

II. THE THEORY OF THE GENERALIZED RRMT+

A. Multiport System

A multiport VNA can be described in general as shown in Fig. 2. The schematic diagram consists of an ideal VNA, the matrices $[A]$, $[B_i]$ of systematic measurement errors, and the DUT. An example of an n-port VNA with a reference channel architecture (with n+1 measurement receivers) is given in Fig. 3.

Its error model is based on the 10-term representation: for every state of the system switch, 5 error terms can be defined for each pair of VNA ports.

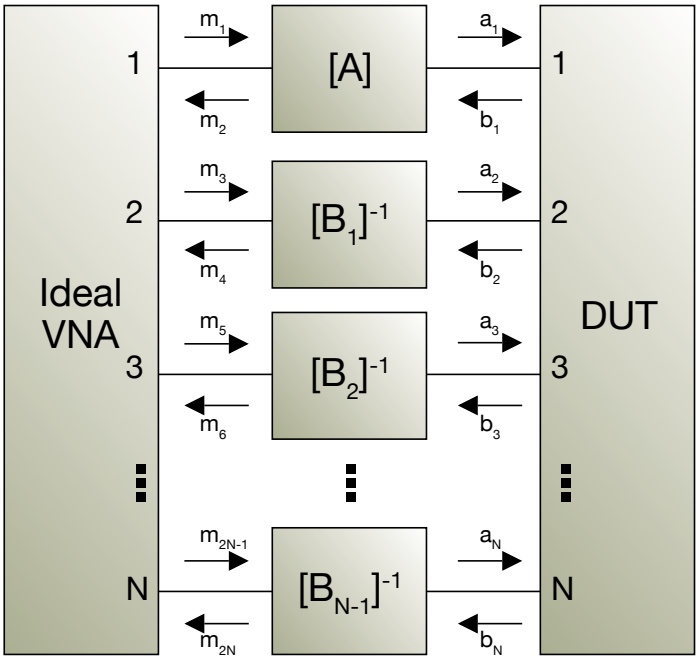

Figure 2:
Block diagram of n-port VNA that represents the ideal VNA, the matrices of error terms $[A]$ and $[B_i]$, and the DUT.

For instance, the two-port case gives terms: E_D^I, E_R^I, E_S^I, F_L^I, and F_T^I for the first state of the switch; and F_D^{II}, F_R^{II}, F_S^{II}, E_L^{II}, and E_T^{II}, for the second state of the switch (Fig. 4). Introducing matrices $[G]$, $[H]$, and so on, this description can easily be extended to the n-port case with 2^*n^2+n error coefficients.

The multiport reflectometer VNA can be described by both the 10-term and the 7-term based models. The 7-term based n-port VNA error models consists of the $4^*(n-1)+3$ coefficients.

Crosstalk between calibrating ports is not addressed in these models. Crosstalk affected systems require more sufficient modeling and include additional error terms.

It is easy to demonstrate that the relationship between the matrix $[M]$ of measured parameters m_j and the DUT's actual parameters $[Sx]$ can be represented over error-matrixes $[A]$, $[B_i]$, (or $[E]$, $[F]$, $[G]$, etc.) in a similar way for both types of the n-port VNA realization [,]. Once the measured values m_j as well as the coefficients of $[A]$ and $[B_k]$ (or $[E]$, $[F]$, etc.) are known (where j=1, 2, …, 2^*n, k=1, 2, …, n-1, and n is the number of the VNA ports), the actual S-parameters $[Sx]$ of the unknown DUT can easily be found [e.g. 10].

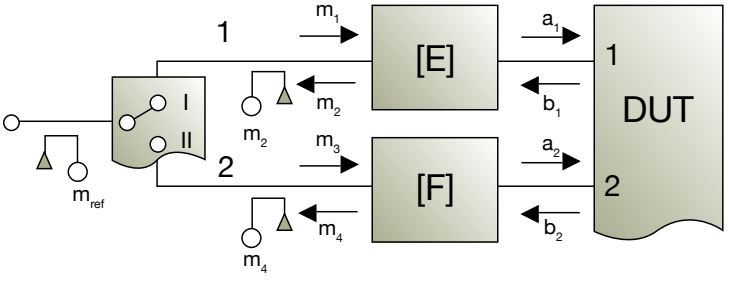

Figure 3:
Block diagram of the n-port VNA based on the reference channel architecture. For simplification, the diagram is reduced to its 2-port part. It shows the reference receiver m_{ref}, the signal source switch, the measurement receivers m_2 and m_4, and the 10-term model error matrices $[E]$ and $[F]$.

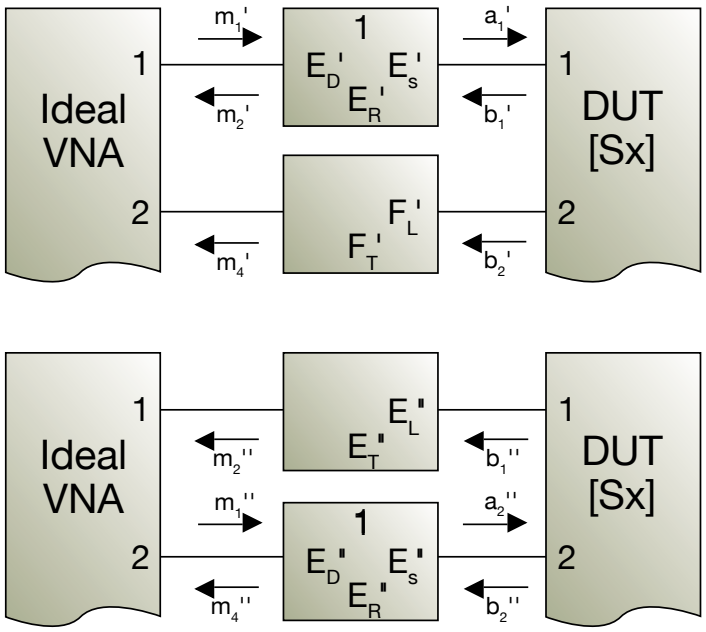

Figure 4:
Block diagram of a 2-port VNA described by the 10-term model for the first and second state of the switch.

B. Generalized RRMT+ Calibration Procedure

The fact that both 10-term and 7-term system descriptions can be applied to the multiport reflectometer VNA, gives the user enough flexibility in choosing an appropriate calibration procedure that fits to the measurement system applications in the best way possible. Since the 7-term calibration procedures are not sensitive to inaccurate reflection calibration standards, they are used more often.

Calibrating the 7-term system, some selected error terms can be calculated by different variants of the TXX calibration within a single procedure: for instance, combining LRM and SOLR (a "hybrid calibration") [14, 15]. This approach has benefits when some thru standards are difficult to characterize (e.g. at wafer level). However, hybrid calibrations are neither free of possible "port bracing" nor the limitation of the calibration dynamic range because they are based on the 7-term model [10].

The novel RRMT+[1] multiport calibration approach is free from these limitations as well as from drawbacks discussed in the introduction. RRMT+ integrates the advantages of the 10-term and 7-term calibration algorithms into one procedure and extends the algorithm reported in [11, 16] for non-ideal thru standards.

In contrast to hybrid calibrations, the RRMT+ procedure uses the 7-term-based self-calibration process to calculate the accurate behavior of partly know standards (reflects and thrus) and the 10-term process to calibrate the system. Reflect standards (partly-known open and short) are characterized by the very robust LRM+ method [8]; reciprocal thrus (loop-back, crossover, Fig. 1) are defined with the help of the SOLR algorithm [5]. Additionally, introducing at least one straight line in the measurements allows the characteristic impedance Z_0, phase, and attenuation constants of the straight thru to be found [17]. If necessary, the load can be specified.

Once all calibration standards are fully known, all error terms are calculated by the modified GSOLT procedure with non-ideal, but know standards [11]. Therefore the limitations of the multiport 10-term (SOLT), multiport 7-term (TXX) conventional and hybrid methods are overcome in one procedure.

C. RRMT+ Requirements for Calibration Standards

Depending on the number of DUT ports and their design, different configurations of the wafer-level measurement system are possible. For example, Fig. 5 shows two dual wafer probes with the same pitch. Calibrating the system like

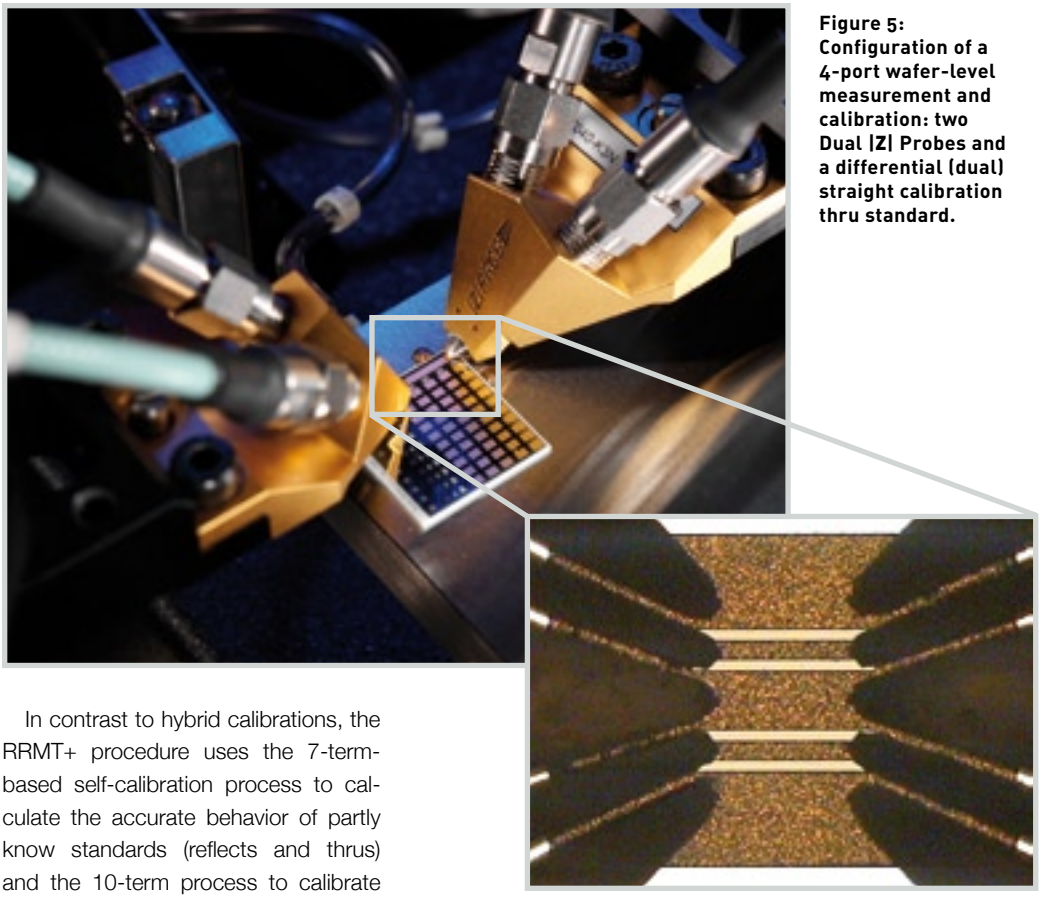

Figure 5:
Configuration of a 4-port wafer-level measurement and calibration: two Dual |Z| Probes and a differential (dual) straight calibration thru standard.

[1] *Advanced Reflect-Reflect-Match-Thru*

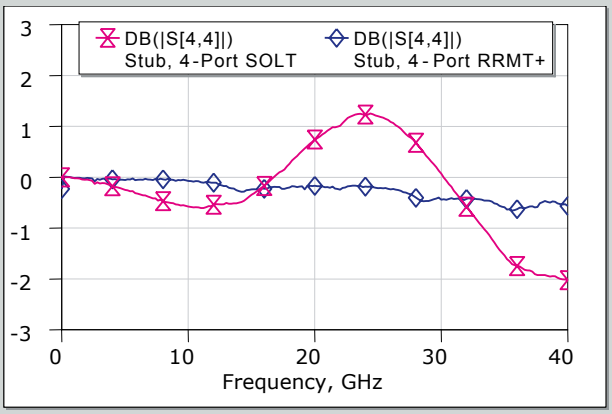

Figure 6:
Return loss measurements of the dual 6000 µm stub line on port 4 with respect to the 4-port SOLT and 4-port RRMT+ calibrations.

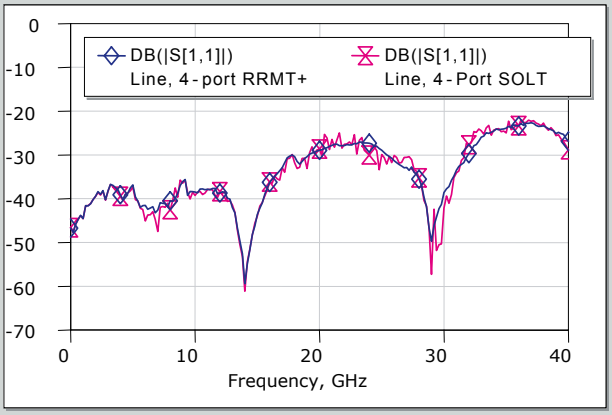

Figure 7:
Return loss measurements of the dual 6000 µm line on port 1 with respect to the 4-port SOLT and 4-port RRMT+ calibrations.

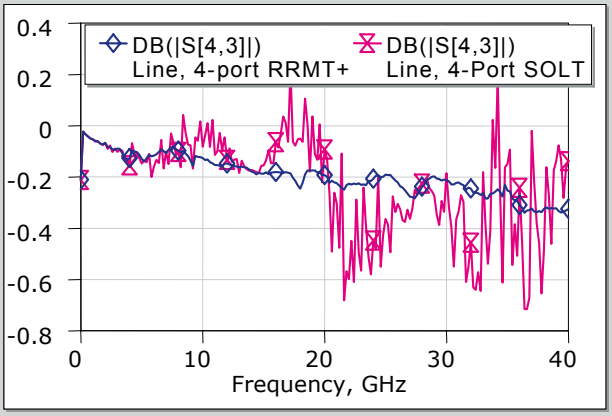

Figure 8:
Insertion loss measurements of the dual 6000 µm line between port 3 and port 4 with respect to the 4-port SOLT and 4-port RRMT+ calibrations.

this, the set reflection (open, short, load) and transmission (thru, lines) standards can be measured. Reflection standards are typically grouped into one element consisting of four same-type standards. Thus, all required S-parameters (return loss) can be obtained after just one movement and contact. All elements in this group are equal to each other.

Full 4-port calibration requires 6 thru standards, as shown in Fig. 1. However, the electrical characteristics of only 3 standards are required: straight (port 1 – port 2), loop back (port 1 – port 3), and cross over (port 1 – port 4). The others are symmetrical.

Therefore, RRMT+ requires at minimum that:

1. open and short for all four ports are partly known (only within +/- π/2 their phase);
2. load port 1 and port 2 (or port 3 and port 4) are known, but they an be represented by any impedance element and different from each other;
3. straight thru port 1 – port 2 (or port 3 – port 4) is known.

Alternatively, requirements 2 and 3 can be replaced by adding an additional straight line with known physical length.

These requirements can vary depending on the system configuration and application type.

III. EXPERIMENTAL RESULTS

The theory of the novel RRMT+ calibration approach was proven by experimental results. The experimental setup included a Rohde and Schwarz 40 GHz 4-port ZVA network analyzer; the semi-automatic PA200 probe system, the Dual |**Z**| Probe 500 µm pitch GSGSG configuration, and the GSGSG CSR-34 calibration substrate from SUSS MicroTec. Some additional test devices were used for the calibration comparison and calibration accuracy verification.

It is important to note that the probes and standards included in this setup had a very large pitch (500 µm). This presents a significant challenge for accurate broadband calibration (beyond 20 GHz).

To avoid the influence from contact repeatability error, the measured data were acquired in one measurement series in raw format and saved to an external PC. The calibration and the error correction were performed offline with the help of SussCal Professional calibration software[2].

The experimental results demonstrated a significant improvement in the measurement accuracy when the new RRMT+ calibration algorithm was used (Fig. 6-8).

Fig. 5. Configuration of a 4-port wafer-level measurement and calibration: two Dual |**Z**| Probes and a differential (dual) straight calibration thru standard.

IV. CONCLUSION

The analysis of conventional multiport calibration procedures was fulfilled. Their advantages and drawbacks for wafer-level applications were discussed and the novel RRMT+ calibration procedure was introduced.

It was demonstrated that the RRMT+ approach is not sensitive to conventional wafer-level multiport calibration problems: in general, it does not require accurate modeling of all reflection and transmission standards. This fact guarantees that the RRMT+ method is significantly less sensitive to typical calibration problems in a multiport wafer-level setup. Thus it is ideal for broadband characterization of multiport and differential devices without limitations of their sizes, frequency and design.

ACKNOWLEDGEMENT

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Alignment Mark Improvements Through Design

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Abstract

I'm sure you have all seen examples of printed pictures that have been magnified many times to the point where all you can see are small dots or pixels which represent the picture under normal view. We will show how the reverse of this procedure can be used to improve the alignment mark visibility. There are occasions when alignment marks are difficult or nearly impossible to use for automatic alignment due to process or materials changes.

For example, there are several targets in Figure 1 which cannot be automatically aligned and which should look like those in Figure 2.

So, the question is what can be done to improve the alignment marks of Figure 1 without changing or altering the current process conditions? The answer is very simple and will be explained hierin.

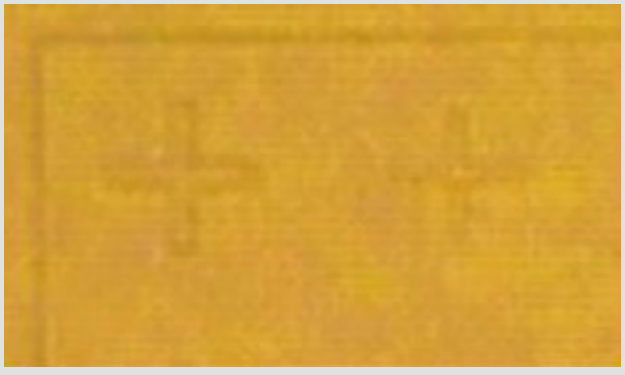

Figure 1:
Targets Difficult To See or Auto Align

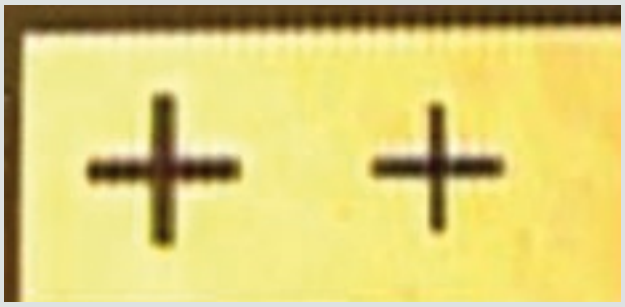

Figure 2:
Targets As They Should Look for Auto Align

Alignment Mark Design

Our procedure for improving the auto align capability of the alignment marks in Figure 1 is to lithographically produce a series of small images in such a way as to make the alignment mark visible under normal use. For example given the alignment mark like that shown in Figure 3, which is basically the design of the marks shown the Figure 2, you would design the new alignment mark with a series of small boxes equally spaced within this shape.

Figure 3 Typical Alignment Mark Design You could create a series of alignment marks which are made up of smaller objects of various sizes such as those shown in Figure 4 which are designed, left to right, as 5, 4, and 3 micron boxes and spaces. Note how the cross appears to get darker as the boxed are designed smaller and smaller, ie., the mark becomes more visible as in Figure 4. Figure 5 represents an enlarged view of one of the proposed designs.

Figure 5 Enlarged View of Mark Design The concept then is to create the alignment mark using small enough images such that the resultant image will become more visible due to the interaction of light on the edges of the small images.

Experimental Results

In the case of the images shown in Figure 1 the alignment marks have been defined in a thin layer of silicon dioxide, about 100 nm, then covered with a highly reflective metal such as aluminum to about 300 nm. Under these conditions there will be little or no difference in reflectivity between the alignment mark and surrounding area and the alignment mark will not be suitable for automatic alignment or manual alignment as was seen in Figure 1.

By creating an alignment mark comprised of five micron boxes and spaces it is possible to produce an alignment mark, similar to that shown in Figure 6

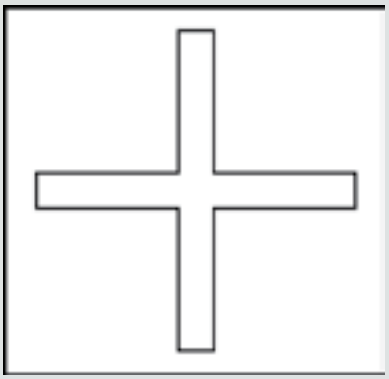

Figure 3:
Typical Alignment Mark Design

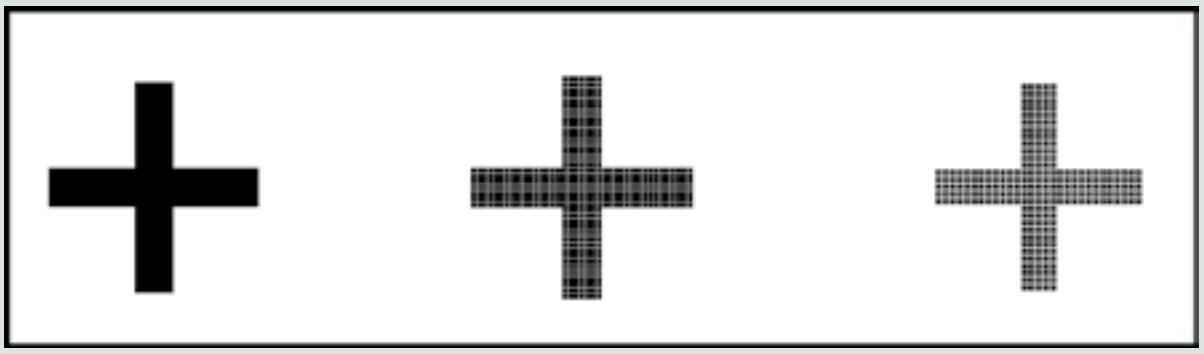

Figure 4: Modified Alignment Mark Design

that may be used for automatic alignment with little or no difficulty.

Actual testing of this mark on several production runs resulted in one hundred percent automatic alignment of the parts with no alignment failures as compared to standard production runs with less than ten percent of the wafers being automatically aligned. Additional alignment mark designs shown below were also tested with similar success.

Summary

In summary, significant improvements in automatic alignment capability may be obtained by manipulating the design of the alignment marks.

Ground Rules for Design

Lithographic process bias will determine how the marks will look on the substrate. If there is no process bias then a design where the boxes are equal size to the space between boxes is possible. However, if a box designed on the mask as five microns will grow to six microns on the substrate then the design must be compensated to take this into account. The mask would then be designed with boxes at about four microns with spaces of six microns which would result in equal size boxes and spaces of five microns. Size will be limited by the printing resolution of the tool combined with the resist film thickness. The images in this report have been designed and tested for lithographic processes using about one to three microns of resist but concept should work for even thicker films.

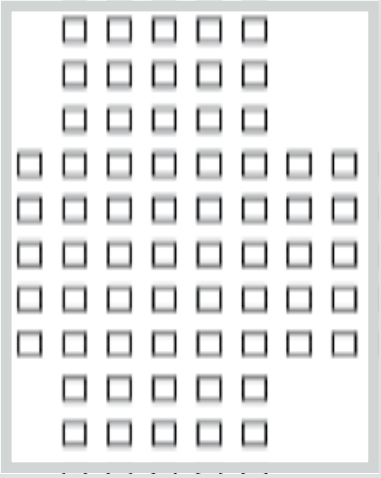

Figure 5: Enlarged View of Mark Design

Bio

Cliff Hamel is the principle applications engineer at SUSS MicroTec, Inc. for lithography processes involving full field mask aligners and automated cluster coating equipment. Over the last ten years at SUSS he has co-authored several papers in the field of thick resist processes and process optimization. He has over 26 years of BEOL process and mask fabrication experience at IBM where he was the principle engineer and inventor for lift off process development. He received his BS in chemical engineering at Trinity College of Vermont.

Figure 6: Modified Alignment Mark On Substrate

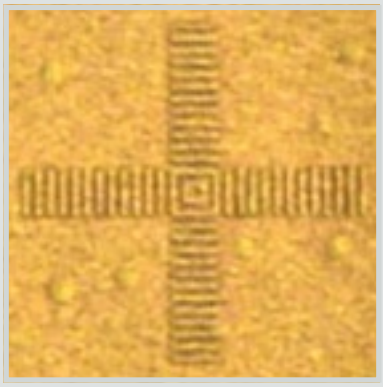

Figure 7: Alternate Target Designs That Were Functional

SUSS in the News

Here's a summary of our recent press releases. To read the entire press release, please visit www.suss.com/about_suss/latest_news

Dr. Claus Dietrich, Division Manager of the Test Systems Division at SUSS MicroTec, and Kumpanat Thonsiri, Business Unit Manager for Test Systems in the Asia-Pacific Region, strike a traditional Chinese gong, a symbol of happiness and good luck, to officially open the new Applications & Measurement Center at SUSS MicroTec Singapore.

May 15, 2007 · SUSS MicroTec AG appoints new Chief Financial Officer

SUSS has appointed Michael Knopp as the Group's new Chief Financial Officer. He will join SUSS on August 1st 2007. Michael is a business leader with proven financial expertise. "After successfully achieving the turnaround in 2006 we are looking towards a future of strategic growth. Michael's financial and managerial experience working for international high tech companies will be a great asset to the company as we move forward" said Dr. Winfried Suess, Chairman of SUSS' Supervisory Board and son of the company's founder Karl Suess.

May 11, 2007
SUSS MicroTec Strengthens Application Support Network

New Applications & Measurement Center in Singapore provides unique support for semiconductor test community in the Asia-Pacific region SUSS opened an Application & Measurement Center in Singapore. The new facility houses state-of-the-art test equipment and will provide unique application support for customers in the Asia-Pacific region.

May 9, 2007 · SUSS Unveils Next Generation Wafer Bonding Technology

SUSS announced the launch of the company's next generation, ground breaking wafer bonding technology. The ELAN CB8 is based on an entirely new design platform and is capable of achieving "best-in-class" across a wide range of performance parameters. The elite performance package offered by the ELAN CB8 includes superb force and temperature uniformity (±5% and ±1°% respectively) as well as a super clean, high-vacuum environment to improve yield even in the most critical applications. The ELAN CB8 also boasts rapid heat up and cool down times, maximizing productivity for wafer bonding customers. The ELAN CB8 integrates a number of innovative and patented technologies to deliver breakthrough performance for the most critical applications. Pressure Column Design ensures the ultimate in pressure uniformity, and is confirmed via load cell verification. SUSS is also the only company to develop and package a Wedge Error Compensation (WEC) function into its wafer bonders, which ensures true planarity before every single bond. Vacuum isolated heaters allow heat to be directed exactly where it is needed – at the wafer – while the silicon nitride heater material provides superior strength and conduction over time and under elevated temperatures. Finally, an extremely rigid 3-post load-bearing, superstructure frame evenly and predictably supports the extremely high forces required for many bonding processes.

May 8, 2007 · Grundfos Uses Spray Coater from SUSS MicroTec for Pressure Sensor Production

Grundfos, a full-line supplier of pump technology located in Denmark, has purchased, installed and qualified a fully automated Gamma AltaSpray coating cluster from SUSS MicroTec for production of Grundfos pressure sensors, which are used in its high quality pump solutions. With the AltaSpray approach SUSS MicroTec, has developed a revolutionary spray coating technology, that delivers consistent conformal coatings over various structures such as 90 degree corners, KOH etched cavities, V-grooves or lenses. SUSS AltaSpray systems are capable of achieving uniform photoresist coatings on sidewall slopes from 0 to 90 degree and even on re-entrant profiles.

May 2, 2007 · SUSS MicroTec Unveils New Metrology Equipment for MEMS Production

With the DSM200 SUSS MicroTec has developed a new automated metrology system for all emerging front to backside alignment applications. The cassette-cassette front-to-back alignment metrology system is the ideal tool for verifying alignment accuracy on wafers from 2 inch to 200mm. Incorporating state-of-the-art pattern recognition technology, the DSM200 offers the highest measurement accuracy of 0.2 microns at 3 sigma on a fully automated platform with minimized operator intervention. Based on the latest production platform of the SUSS MA200Compact Mask Aligner, the DSM200 provides reliable and accurate metrology for double-sided alignment and exposure applications frequently used in the manufacturing of MEMS devices, power semiconductors and optoelectronics.

April 23, 2007 · SUSS MicroTec unveils the KADETT; a New High Accuracy Placement and Bonding System for R&D

SUSS recently unveiled the KADETT, a new High Accuracy Placement and Bonding System especially configured for R&D laboratories, universities and pre-production environments. The new SUSS KADETT Semi-Automatic Device Bonder is a flexible and open platform for accurate assembly and bonding of devices on a large variety of substrates. The machine performs accurate Pick and Place functions. A wide range of bonding processes including In-Situ Reflow, Thermo-Compression, Thermo-Sonic and Adhesive Bonding are available for forces up to 75N. The KADETT, originally developed by the Paul Scherrer Institute, has been proven in the field for bonding Ionizing Radiation Detectors and it is also well suited for Advanced Packaging, micro-optics or MEMS assembly. Accurate alignment is automatically achieved by a vision system which uses two independent high resolution video microscopes (chip and substrate) with a high resolution (0.1µm) XY alignment stage. The robust and simple concept of the system meets the current requirements for high accuracy placement and bonding various components and its open design makes it the ideal platform for future evolution of the advanced packaging applications. The flexible architecture of the SUSS KADETT enables the integration of many processing modules such as a UV glue curing system, Ultrasonic bonding head and many others.

March 27, 2007 · Infotonics Selects SUSS Bonding Systems for MEMS Development Center

SUSS announced that Infotonics, a collaborative, world class Center of Excellence in photonics and microsystems, has selected the SUSS ABC200 wafer bonding cluster tool and FC150 device bonder as strategic investments in their MEMS packaging lab. With corporate partners such as Corning, Eastman Kodak, and Xerox, as well as relationships with over 20 universities, Infotonics has played a central role in groundbreaking work to benefit the biomedical and communications industries. Infotonics' core competencies include the design, simulation, fabrication, packaging, test and metrology for MEMS and MOEMS devices. By using the facilities at Infotonics, customers can develop and deliver innovative products at reduced risk and cost, accelerating their time to market.

March 21, 2007
SUSS and STS Launch MEMS Technology Roadshow

SUSS MicroTec and Surface Technology Systems, two of the leading providers of MEMS manufacturing solutions worldwide, announced a U.S. based roadshow called "MEMS Technology: Embracing the Future," scheduled to debut in Boston, Massachusetts on April 20th. "MEMS Technology: Embracing the Future" will include presentations on the latest critical manufacturing processes in MEMS today. Talks will cover high aspect ratio lithography and plasma etching, wafer bonding, dry release processing and wafer level test. In addition, speakers will discuss the key manufacturing issues critical for advanced MEMS device fabrication today. SUSS and STS have invited representatives from Primaxx, Inc. and XACTIX, Inc. to join the roadshow, creating a unique opportunity to listen to industry experts cover most of the key MEMS technologies used today.

February 8, 2007
SUSS Bonders Selected for MEMS Research Lab in Mexico

Munich, GERMANY February 8, 2007 – SUSS MicroTec, a leading supplier of precision manufacturing and test equipment for the semiconductor and emerging markets announced today that the University of Juarez (UACJ), Mexico has selected its advanced wafer bonding equipment for its research laboratory. UACJ is an integral member of the Paso del Norte (PDN) Regional MEMS Cluster and a key player in supporting bi-national innovation and entrepreneurial development in Mexico. The cluster consists of academia, government research labs, and industry, and is focused on commercialization opportunities in MEMS packaging. The UACJ research facility will use SUSS's SB6e semi-automated wafer bonder, BA6 bond aligner, and FC150 device bonder to develop and advance MEMS prototyping processes in Mexico.

February 5, 2007 · Epson Selects MA200Compact Mask Aligner from SUSS MicroTec for Wafer Level Chip Scale Packaging

Seiko Epson Corp. ("Epson"), world leader in printing and imaging products, has purchased an MA200-Compact Mask Aligner from SUSS MicroTec, the leading supplier of precision manufacturing and test systems, to support their Wafer Level Chip Scale Packaging (W-CSP) production. After a careful evaluation of competitive systems Epson decided on SUSS' MA200compact Aligner because it demonstrated excellent throughput and a submicron overlay and alignment accuracy. In addition, the MA200Compact has been optimized for advanced thick chemically amplified positive tone resists that allow for ninety degree resist profiles. The system that was purchased during the fourth quarter of 2006 will be delivered to Epson's facility in Japan. Mask aligners are proximity printing tools where mask and wafer are separated by an exposure gap in the range between 20 and 100 microns. Compared to steppers, where multiple shots may be necessary to expose a full wafer, the mask aligner is able to expose the wafer in one shot, which results in a significant throughput advantage. Proximity aligners offer a low cost lithography solution for high volume production. The SUSS MA200Compact combines proven mask aligner technology with innovative features such as the patent pending DirectAlign® option. With a guaranteed alignment accuracy of 0.5 microns at 3 sigma DirectAlign increases the mask aligner process window for a variety of new thick resist applications.

Below are some of the places you can find SUSS in the upcoming months:

Date	Tradeshow/Seminar	Location	Focus
July 11-13, 2007	IPFA	Bangalore, India	Failure Analysis (test)
July 11-13, 2007	Interopto 2007	Chiba, Japan	Optoelectronics
July 17-19, 2007	SEMICON West	San Francisco, CA	All
July 25-27, 2007	Micromacine Exhibition	Tokyo, Japan	MEMS
August 8, 2007	Electronic Journal Technical Seminar	Tokyo, Japan	C4NP
August 14-17, 2007	CSTC 2007	Montreal, Canada	MEMS/Nano
Sept. 2-6, 2007	COMS 2007	Melbourne, Australia	MEMS, Nano
Sept. 12-14, 2007	SEMICON Taiwan	Taipei, Taiwan	All
Sept. 24-26, 2007	MNE 2007	Copenhagen, Denmark	MEMS, Nano
Sept. 25, 2007	MEMS Technical Seminar 2007	Tokyo, Japan	MEMS
Sept. 25-26, 2007	Interconex 2007	Toulouse, France	Packaging onboard equipment
Oct. 8-10, 2007	European Microwave Week	Munich, Germany	HF Probing
Oct. 9-11, 2007	SEMICON Europa	Stuttgart, Germany	All
Oct. 10-12, 2007	NNT	Paris, France	Nano
Oct. 26-Nov. 8, 2007	SUSS Asia Tour	Asia	MEMS, Nano, ADP
Nov. 5-8, 2007	MNC	Japan	MEMS, Nano
Nov. 6-7, 2007	ISTFA 2007	San Jose, CA	Failure Analysis (test)
Nov. 13-15, 2007	IMAPS Int'l.	San Jose, CA	Litho/MEMS
Dec. 5-7, 2007	SEMICON, Japan	Chiba, Japan	All
Dec. 11-14, 2007	Microwave Show (APMC)	Bangkok, Thailand	HP Probingng

We hope you found this edition of the SUSS Report interesting and informative.
For more information about SUSS and our products, please visit

www.suss.com

or write to **info@suss.com** with your comments and suggestions.

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SUSS. Our Solutions Set Standards

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