Issue July · 2008

SUSS report

www.suss.com

Precision Wafer to Wafer Packaging Using Eutectic Metal Bonding

Eutectic metal bonding of wafers is used in advanced MEMS packaging and 3D integration technologies. A unique feature of eutectic metals is the melting of the solder like alloys that facilitate surface planarization and provide a tolerance to surface topography and particles. Advanced wafer level bonding using 2-3um thick metal layers allows precision alignment preventing the aberrant viscous flow of the metal and wafer slippage.

Also in this issue:

- **C4NP**
  Next Generation Wafer Bumping

SÜSS MicroTec

index

VLSI RESEARCH INC ® 10 BEST SUPPLIERS OF 2008 Customer Satisfaction

SUSS Scores First Place for 10th Year as Material Handling Supplier

Full View

The Age of 3D Integration

Wilfried Bair
Vice President
Strategic Business Development,
SUSS MicroTec

When commercial wafer bonders were first introduced to the industry in the early 90's the main driver for this new equipment type was the then emerging MEMS technology. Pressure sensors and accelerometers for automotive applications set off on its booming track providing the first volume market opportunity for wafer bonding in large quantities. Since the early 60's and until then the mechanical use of silicon was mainly limited to high performance, but low volume applications in aerospace.

The second phase in wafer bonding is hallmarked by the growing demand for MEMS devices in consumer electronics providing new and unique product features to a vast mass of insatiable consumers. From MEMS microphones to accelerometers being used in game consoles like the Nintendo Wii MEMS continued to penetrate and influence the appetite of the consumer world. The latest "MEMS publicity stunt" was Apple's announcement of the 2nd generation iPhone. Describing the latest unique features of the iPhone the use of (MEMS) accelerometers and smart sensors was prominently shown on the supplier's website.

Now we are looking at the third and - what we expect to be - the largest surge in demand for wafer bonding applications: We are approaching the age of 3D integration of semiconductor devices. The envisioned plan for the 3D integration includes logic, memory, mixed signal, image sensor and almost all other commercially viable semiconductor processes. A commonly used comparison of 3D integration with real estate illustrates that when silicon space is at a premium or cannot be made larger the only logical conclusion is to expand constructions into the third dimension.

Thus 3D integration technologies allow for an alternate path to Moore's law. This is now commonly referred to as "More than Moore" and shows that the continuous scaling of transistors by doubling approximately every two years can be pursued by stacking devices.

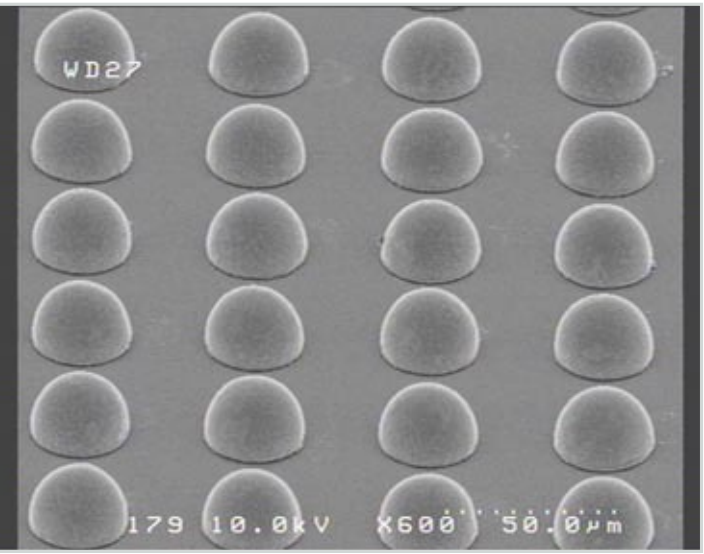
To address this new market opportunity novel equipment approaches are required to provide submicron alignment accuracy for 300mm wafers for the full product range of lithography and wafer bonding tools. The product and process development teams within SUSS MicroTec have worked on a new and unique set of tools to address this upcoming challenge. Millions of connections per stacked device will be dedicated to the use of metal bond processes with alignment accuracies in order to match the roadmaps of the continuously shrinking Through Silicon Via (TSV) sizes down to interconnect pitches of 3 microns and less.

We are approaching the age of 3D integration – in fact, we are already there. And SUSS is right ahead to help our customers maximize their wafer's real estate. And maximize their profit. As their success is our success.

Klaus Ruhmer, Sales & Marketing C4NP, and
Emmet Hughlett, VP and Business Unit Manager C4NP, SUSS MicroTec

Solder bumps were invented almost half a century ago – an eternity in today's world of micro electronics. The technology has not stood still and many advances have been made in the areas of solder and UBM (Under Bump Metallurgy) materials, solder deposition techniques and equipment technology. The basic principle however remained unchanged: A UBM feature is created on open pads of a semiconductor chip. A specific volume of solder is deposited on top of the UBM. During subsequent or in-situ reflow, the solder volume transforms into a solder sphere due to surface tension. That solder sphere is then used to connect to the outside world. Depending on the type of package, that may either be to an intermediate substrate (Flip Chip in Package FCiP) or to the board itself (Wafer Level Chip Scale Package WLCSP).

50um pitch, lead-free solder bumps (Courtesy of IBM)



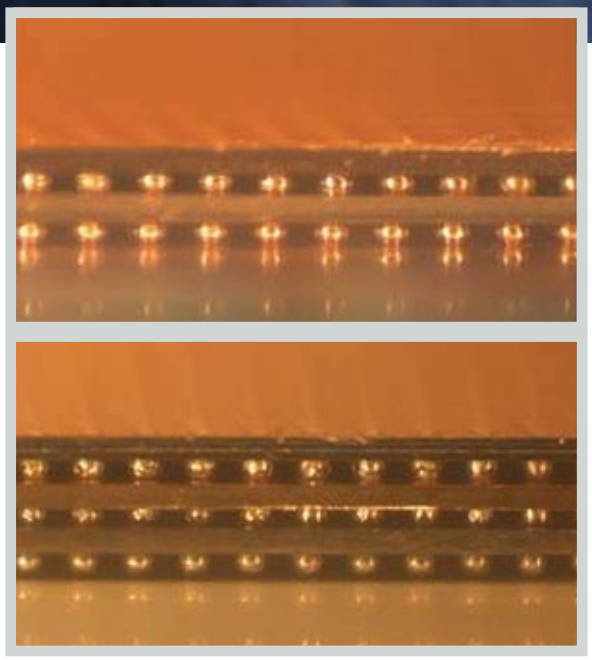
SUSS MicroTec has played a key role in Wafer Bumping since its infancy. SUSS Mask Aligners and coat/develop cluster systems are ideally suited for the specific requirements related to patterning the UBM and the resist and polymer layers for subsequent metal deposition.

Advanced packaging techniques including 3D packaging utilizing solder bumps as the primary interconnect-technology have been growing at an impressive pace since the mid 1990's. Ever higher interconnect density needs combined with increasing performance requirements are no longer a match for existing interconnect technologies such as wire bonding.

Besides the solder bump itself however, the selection of the appropriate UBM or BLM (Ball Limiting Metallurgy) materials has shown to be the primary driver for cost, reliability and electrical performance.

One key advantage of IBM's C4NP is it's capability to put bumps on essentially any UBM material as long as it wets to solder. As previously reported in this publication, C4NP also tackles other classical bumping challenges and enables environmentally friendly, low-cost, fine pitch bumping using a variety of lead-free solder alloys. With C4NP, pure bulk solder is molten and injected into prefabricated glass molds. These molds contain etched cavities mirroring the bump pattern of the wafer. Once the molds are filled, all solder bumps are transferred in one step onto the wafer. The process is quite simple and doesn't use any liquid flux. That makes it a low cost, high yield and fast cycle time solution for bumping with a wide variety of high performance lead free solders. In addition, this process also eliminates the need for toxic chemicals needed for alternative bumping techniques – C4NP is truly a "Green Technology".

Unlike other solder deposition processes, C4NP is independent of the UBM materials used. It offers full flex-



3D - Stacked chips using C4NP micro-bumps (Courtesy of IBM)

ibility to combine the proper UBM with the right solder alloy to not only fit the application but also meet cost and performance requirements of the final package.

Besides the need for lead-free, future solder bumps are also driven by 3D packaging and integration requirements. 3D requires fine pitch bumping capability to accommodate very high interconnect density.

More information about SUSS MicroTec's wafer bumping and advanced packaging solutions can be found on www.suss.com.

KLAUS RUHMER

Klaus Ruhmer has global Sales & Marketing responsibility for C4NP wafer bumping technology at SUSS MicroTec. He has been with SUSS since 1998 starting out as an Applications Engineer for wafer bonding and lithography products. Over the years, he has held various technical and sales related positions within SUSS. Prior to his current position, Klaus was responsible for Strategic Accounts in North America.
Klaus is a native Austrian and holds a BS in Electronics and Telecommunications Technology. He worked in software development before he moved to the US and joined the semiconductor industry in 1996.

EMMETT HUGHLETT

is Vice President and C4NP Business Unit Manager with SUSS MicroTec. Emmett holds a Ph.D. in electrical engineering. Emmett's career includes 24 years of engineering, sales and management in the semiconductor equipment industry, with both Kulicke & Soffa Industries and SUSS MicroTec Inc.

PRECISION WAFER TO WAFER PACKAGING USING EUTECTIC METAL BONDING

ABSTRACT

Eutectic metal bonding of wafers is used in advanced MEMS packaging and 3D integration technologies. A unique feature of eutectic metals is the melting of the solder like alloys that facilitate surface planarization and provide a tolerance to surface topography and particles. Often it is assumed that the alignment in eutectic metal bonding is compromised from the liquid phase transition and precision alignment is not possible. This is not true in advanced wafer level bonding using 2-3um thick metal layers. Precision control of bonding force and temperature prevent the aberrant viscous flow of the metal and prevent wafer slippage.

Keywords: Eutectic bonding, wafer bonding, MEMS packaging, Au-Sn, Au-Si, Cu-Sn.

Shari Farrens, Ph.D., Chief Scientist,
and Co-Author **Sumant Sood,** Sr Application Engineer, SUSS MicroTec

INTRODUCTION

Hermetic packaging of sensors has historically been achieved with glass frit and anodic bonding techniques. However, these techniques are presently limiting scaling of devices and are not appropriate for integration plans for CMOS compatible MEMS.

The widespread use of glass frit bonding can be attributed to its tolerance to particles and surface topography, hermetic quality of the seals, and inexpensive processing costs. In comparison, eutectic alloys provide better hermeticity levels, are equally tolerate to roughness and particles and enable device scaling and integration.

EUTECTIC REACTIONS

A eutectic reaction is a triple point in a binary phase diagram in which the liquid metal solidifies into a solid alloy without going through a two phase, solid + liquid equilibrium region. Because the solidification is immediately realized the atomic rearrangements necessary to establish the equilibrium distribution of phases in the alloy is not fully achieved. The morphology of the grains within the eutectic solid are very small and best described as “feather-like”. This fine grained interdigitated structure is extremely rigid and strong. The fine grain size limits interdiffusion and corrosion.

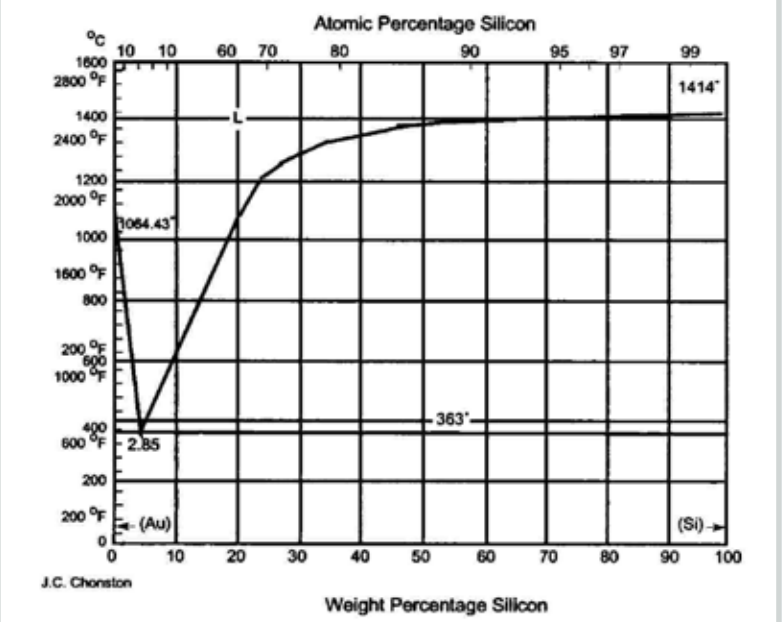


Figure 1:
Au-Si Binary Phase Diagram

Figure 1 is the phase diagram for Au-Si. This phase diagram is a classic eutectic example in which the pure fcc Au phase is denoted as α and the pure silicon diamond cubic phase is β. The diagram shows that there is very little miscibility in either Au or Si and alloys of Au and Si will consist of a two phase mixture of α and β. When an alloy of 2.85wt Si is heated the solid will immediately turn to liquid above 363C avoiding both the α+liquid and β+liquid two phase regions.

MATERIALS SYSTEMS

There are several alloys choices based on Cu or Au eutectic metallurgies. Table 1 shows the commonly used alloys along with the eutectic compositions and the eutectic temperature. All of these alloys have been used in MEMS packaging, or optical MEMS.

Table 1:
Eutectic Alloys used in MEMS Packaging

Alloy	Eutectic Temperature	Eutectic Composition
Al-Ge	419 C	49/51 wt%
Au-Ge	361 C	28/72 wt%
Au-In	156 C	1/99 wt%
Au-Si	363 C	97/3 wt%
Au-Sn	280 C	20/80 wt%
Cu-Sn	231 C	1/99 wt%

The Al-Ge system is also applicable to ternary eutectic reactions between Al and SiGe layers because Al forms a binary eutectic reaction with both Si and Ge. This system is particularly CMOS friendly.

DEPOSITION TECHNIQUES

There are two fundamental methods for creating a eutectic seal. The first method involves deposition of pure materials which then are diffused together until the eutectic composition is reached. Then the eutectic alloy can be melted and reflowed to achieve the seal. By contrast the binary alloy can be deposited as a single layer already at the composition necessary to achieve a eutectic reaction.

Eutectic alloys can be plated, sputtered or evaporated onto the substrates. There are several sources for alloy sputter targets that are ideally suited to thin layer deposition and many of the alloys can be electroplated at eutectic compositions. Because the quality of the electrical connections, as well as the reaction kinetics, are adversely affected by impurities the deposition should be done as clean as possible. Incorporation of oxygen and other gases in the thin films during deposition can lower the diffusion rates dramatically as will impurities from the electroplating bath.

It is necessary to use adhesion layers when using metal seal technologies. The semiconductor surfaces or glass surfaces should be properly cleaned to remove any previous photoresist layers or other materials remaining from earlier etching or patterning steps. Standard substrate cleaning methods before metal deposition include standard RCA1 and RCA2 or Piranha (sulfuric acid, water and hydrogen peroxide). To remove organics or to clean metal surfaces dry plasma treatments have been effective.

Typical adhesion layers include TiW, TiN, W, Cr, Ni and vary with the substrate used. The adhesion layer is very important to ensure that the strength of the interface is not limited by thin film delamination.

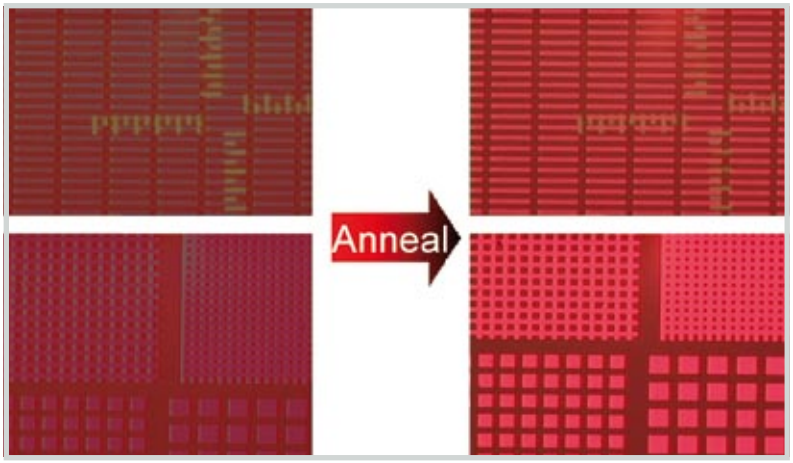


Figure 2:
Formic acid vapor cleaned Cu surface before and after heating to 400 C.

SURFACE PREPARATION

The diffusion of metals as well as the solidification of eutectic phases is inhibited by contamination and oxide layers. In most fabrication facilities the timing of the device wafer and cap wafer process are such that one or the other set of substrates may be queued up for bonding before the other. This delay time between deposition of metal layers and actual bonding can lead to surface oxidation. To achieve high yields and reproducible lots, point of use surface preparation is advised to make sure that metal layers are clean just prior to bonding.

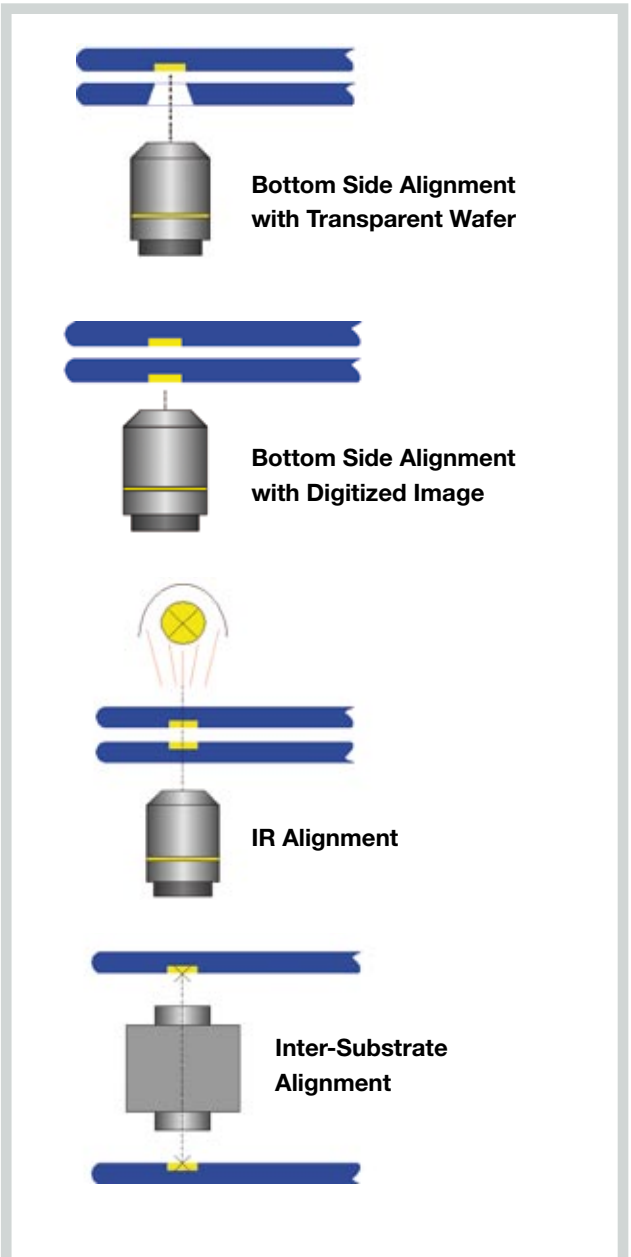
Based on experience in die-to-die and C4NP advanced bumping tools it has been established that formic acid vapor cleaning is very effective for most eutectic alloys, low temperature solders, and aluminum as well as copper in the removal of surface oxides. [2,3]

Vapor phase cleaning can be accomplished in batch processing or as a one wafer at a time, point of use, cleaning. In both cases the wafer(s) are placed in a closed chamber or cleaning station.

The formic acid vapors are introduced and the surfaces oxides are removed. The wafers are then rinsed in DI water and spun dry in the cleaning station. In automated bond cluster tools such as the SUSS MicroTec ABC200 this is done with one or two wafers simultaneously for increased throughput. The formic acid treatment passivates the surface of the metals and prevents reoxidation during the rinse, dry and alignment process that follows.

Figure 2 shows a copper surface that was cleaned with the formic acid vapor, rinsed with DI megasonic water and spun dry. Then the wafer was heated to 400C to see if reoxidation would occur. It does not and this method is used for Cu-Cu bonding in 3D integration technology.

Figure 3:
Position of optics for wafer to wafer bond alignment.



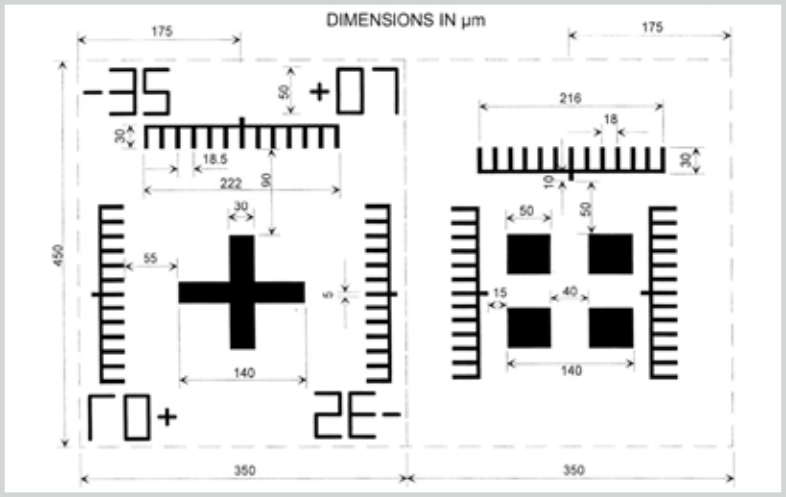


Figure 4:
Male and female alignment keys with graduate xand y- axis scales.

ALIGNMENT TECHNIQUES

Alignment techniques are separated in to methods which align to live target images and those that use stored image alignment. During live image alignment the image of both the device and the cap wafer alignment keys are viewed simultaneously. This has the advantage that throughout the alignment process any shifts that might occur because of vibration, clamping or other mechanical motions can be observed and corrected. With stored images once the position of the initial fiducial is found and captured (digitally stored to memory) the wafer is clamped into position and presumed to be stationary during all remaining teps. However, this can not be verified since the target image is no longer in the field of view.

The options for alignment techniques include BSA (backside alignment) with transparent substrates, BSA with opaque substrates, IR (infrared) alignment, and ISA (intersubstrate) alignment. Figure 3 is a schematic of the objective and substrate locations for each technique. The BAS w/ transparent substrates and the IR method align to live images. ISA also aligns to a live image however, after bonding the microscopes can not access the interface again and are not useful for post bond analysis. The BSA method can be used to verify the post bond alignment accuracy because it is possible to “look through” the transparent substrate at any time during the align and bond process. This is also true for the IR method whenever the metal layers do not obscure the field of view of the target and the wafers have a resistivity greater than 0.01 Ohm-cm (for silicon).

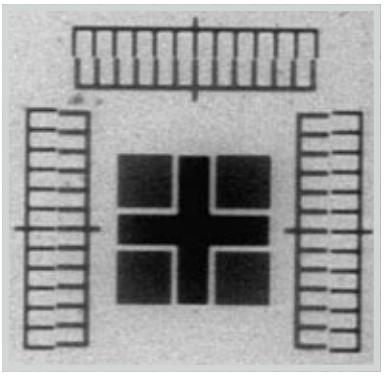


Figure 5:
Post bond IR image of male and female alignment keys in bonded silicon wafers.

Total Steps (14)	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Top Temp (°C)	40.0	40.0	40.0	40.0	40.0	40.0	220	220	300	300	90.0	40.0	40.0	40.0
Bottom Temp (°C)	40.0	40.0	40.0	40.0	40.0	40.0	220	220	300	300	90.0	40.0	40.0	40.0
Chamber Press (mBar)	1000	1.00E-3	1500	1500	1500	1500	1500	1500	1500	1500	1500	1500	1000	1000
Tool Press (mBar)	0	0	0	0	0	0	0	0	5000	5000	5000	5000	0	0
Voltage (V)	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Log Data (Seconds)	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Wait								03:00 mm:ss UNIT		10:00 mm:ss UNIT				
AlarmTime	00:30	00:30	00:30	00:30	00:30	00:30	01:00	00:30	00:30	00:30	03:00	03:30	01:30	01:30
Action														

Figure 6:
Recipe for Au-Sn eutectic bonding.

ALIGNMENT TARGETS

Alignment targets play an important role in achieving good quality bond alignment. In addition some target designs also facilitate process control and monitoring, For example, the alignment key shown in figure 4 contains both a standard cross and box style alignment key as well as graduated scales along the x- and y-axes. During process development the scales can be used to accurately determine systematic shifts and rotation that may occur during the alignment or bonding steps. Note that the graduated scales are used for analysis and not used for alignment. The standard male and female keys are used by the operator or the image recognition system for overlay alignment.

Figure 5 shows an image of one of the keys after bonding. In this example the x-axis is perfectly aligned and the center of the graduated scales is aligned. On the y-axis verniers the pattern is shifted slightly upwards and the first hash mark is aligned. If this were a 0.5 µm vernier then the measurement would imply that at most the misalignment in this example is +/-0 µm in x and +0.5 µm in y. Verniers can be scaled to give 0.1, 0.2 or 0.5µm resolution depending upon the desired precision needed.

BONDING TECHNIQUES AND KNOW-HOW

Bonding of eutectic alloys requires good control over the temperature and pressure profiles in the bonder. This is directly related to the melting of the alloy. The viscosity of the alloy is related to the temperature. As the melt becomes hotter the molten metal is more fluid. With increased fluidity come the propensity of the wafers to slide relative to one another and loose alignment accuracy.

Another reason that temperature control is essential involves ensuring that all the locations on the wafer are melted. Many MEMS structures are fragile and care must be taken that when the applied force is used the interface is soft and fluid. If any areas contain solid metal this will not be flattened by the applied force and the stress may damage underlying or surrounding structures.

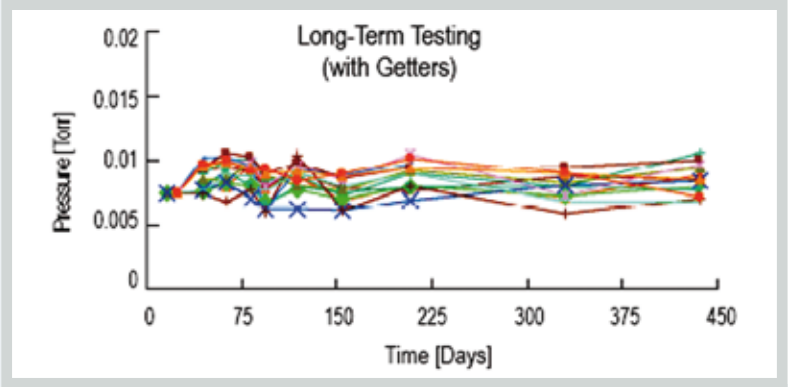


Figure 7:
Hermeticity results from 14 Au-Si eutectic sealed devices from reference 5 and 6.

Equally important is the uniformity of the applied force and the parallelism of the bond chucks to the surface of the wafers. If the force is not applied directly perpendicular to the interface the molten alloy will squeeze into unwanted areas and distortion of the bond lines will result. In extreme cases the molten alloy can be extruded in to the cavity or die structure and prevent device functionality.

In many applications the parts that are being bonded have cavities. To ensure that the cavities are filled with the proper atmosphere, separation flags or spacers are used to maintain a gap between upper and lower substrates. Spacers are thin shims of metal that are placed between the wafers at three locations.

The spacers range from 50-100 µm in thickness and only penetrate the outer most 2-3mm of the wafer perimeters. The spacers allow gases to be purged to and from the cavities throughout the interface via the vacuum pump system in the bonder. Once the proper atmosphere is established within the cavities, the spacers must be removed prior to bringing the wafers in contact for final annealing. Removal of spacers has been identified as a source of mechanical motion that can lead to shifting of the substrates.

Early generation bonders used an all at once removal methodology to retract the spacers. This was accomplished by using a center pin to come down from the upper pressure plate and press the wafers together in the center. This fixed the position of wafers together in the center only. Then the clamps were lifted and the flags pulled out one at a time from the wafer edge. Later generation equipment enabled the flags to be pulled one at a time, however a fundamental problem still existed; if the wafer stack is pinned only in the center it is still free to rotate about the z-axis.

In addition many times the center pin causes harm to delicate dice in the center of the wafer. The solution is new control software that allows for only one clamp to be lifted leaving the other two clamps available to confine the wafers in two locations along the edge of the wafer stack. After the first clamp is lifted the spacer is removed and the clamp is put back down on the stack. Then the next clamp location is released still leaving two locations pinned in position. This improved flag retraction method has been shown to reduce shifting by seven times.[4] This method, called sequential clamp removal is only possible when there are at least three clamp mechanisms on the bond fixture.

The bond recipe itself will resemble the example shown in figure 6. There may be some pump and purge cycles in the initial stages of the recipe to exchange the atmosphere inside the bond chamber with one that is typically inert or reducing. Forming gas, hydrogen mixed with either nitrogen, argon or helium has been shown to dramatically improve yield by suppressing oxidation and metal film contamination. The atmosphere also aids in heat transfer and is preferred to vacuum annealing unless the device requires vacuum sealing.

The temperature as well as the force should be ramped in a controlled fashion. Force is used to establish physical contract between the surfaces. By gradually applying the force the metal will flow between the wafers and remain confined to the pattern seal ring area.

The reaction time is generally short for eutectic bonds when the reaction is driven from melting an alloy layer. When the diffusion reaction is used the recipe may be lengthened by several minutes. Once the material is in the liquid state only a few minutes are required to equilibrate the composition and reflow the interface. Cooling can be done as rapidly as stress conditions in the device or sample will allow.

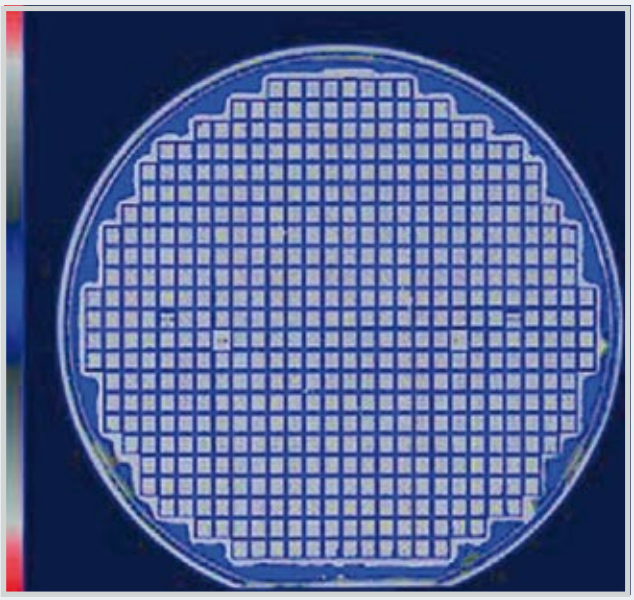


Figure 8:
Sonoscan image of 6" wafers bonded using Au-Si diffusion based Eutectic bonds.

APPLICATIONS AND RESULTS

Eutectic bonds are used for a variety of inertia devices such as accelerometers, gyroscopes, and applications such as RF switches and resonators. A recent publication presented a lengthy study of Au-Si eutectic bonded pressure sensors.[5,6] It is rare to find published hermeticity data and these tests used encapsulated pirani gauges within the device to monitor the leak rates of the seals over more than one year. The study included several eutectic alloys and data in Figure 7 is for a diffused Au-Si eutectic bond showing excellent results.

Several examples of successfully bonded wafers are shown in figure 8-11. Figure 8 shows an example of a Au-Si eutectic bond on 6" MEMS wafers. This particular example was driven from a diffusion reaction and Sonoscan acoustic imaging found no voids within the seal ring area. The blue in this figure indicates a void free bond line.

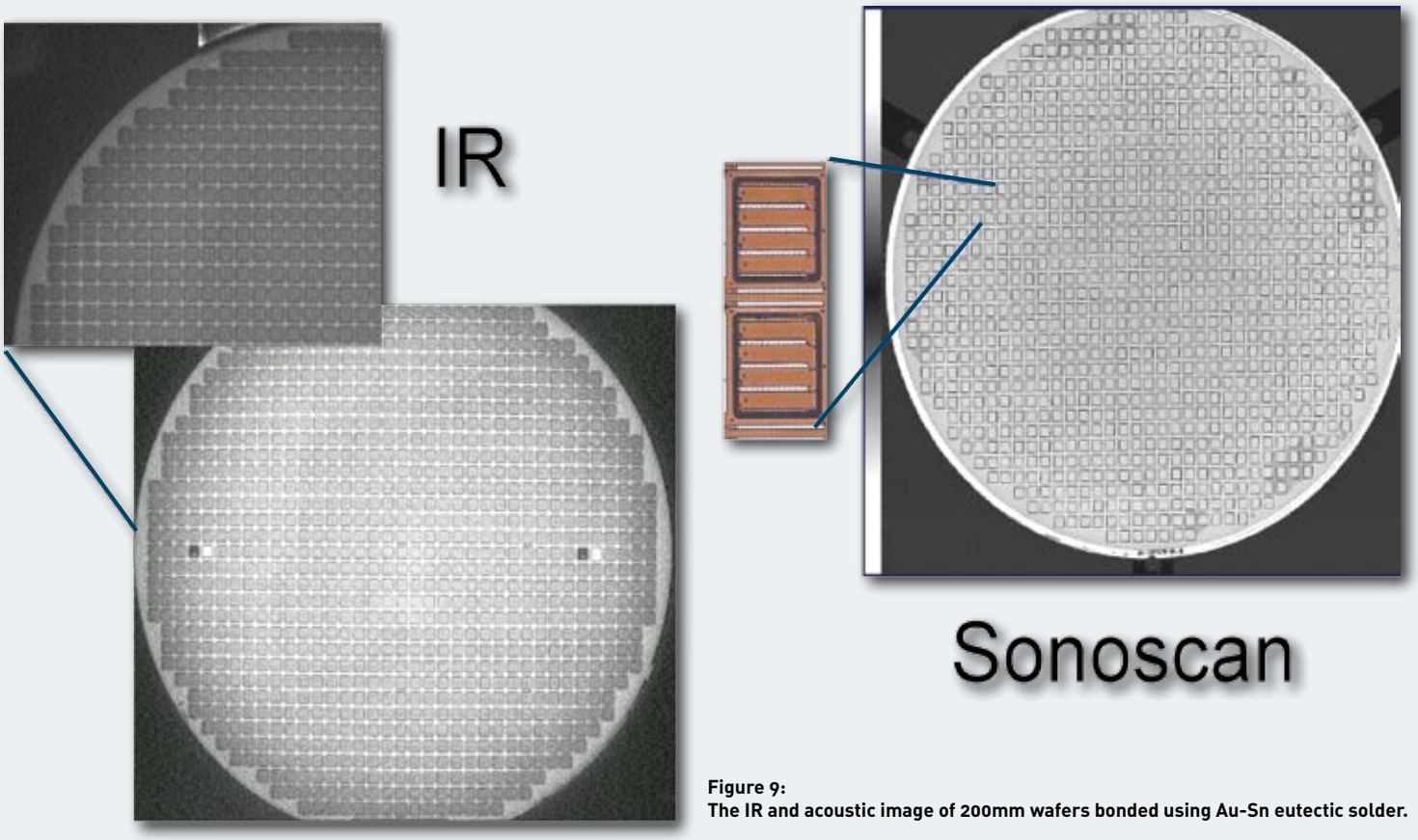


Figure 9:
The IR and acoustic image of 200mm wafers bonded using Au-Sn eutectic solder.

Another feature to point out is that the edge of the wafer is sealed. This is very important if acoustic imaging is used for void detection because when the edges of the wafer are not sealed, capillary action will draw fluid into the areas between the die and complicated post bond process flows.

Gold tin eutectics have been the most requested alloy system in the demo facilities of Suss MicroTec. Shown in figure 9 is an example of the IR and Sonoscan acoustic image of the bonded 200mm wafers. The dice were uniformly bonded at all locations within the wafer.

The gold tin system has also been used on ceramic packages as shown in Figure 11. Due to the surface waviness of the ceramic substrate the conformal nature of a eutectic sealing technology was a desired benefit of this bond method.

The last example is a Au to SiGe eutectic bond. Whenever a eutectic forms between two binary phases it will be possible to form a ternary eutectic phase as well if the remaining binary system also has complete solubility or exhibits a eutectic reaction. In the case of Au a simple eutectic exists between Au-Si at 363C and 2.65wt% Si and between Au-Ge at 419C and 28 at%Ge. Meanwhile, Si and Ge are completely miscible. In figure 11 we show a 200mm wafer bonded by eutectic alloy formation between Au and a SiGe alloy layer on silicon substrates. This process was completed at 420C.

Because eutectic alloys melt and are therefore, self planarizing there is no need to CMP (chemical mechanical polishing) the metal layers. The wetting behavior of the alloy to its adhesion layer will assist with confinement of the molten flow as long as the force is applied gradually. This eliminates one of the costly processes normally associated with metal bonds.

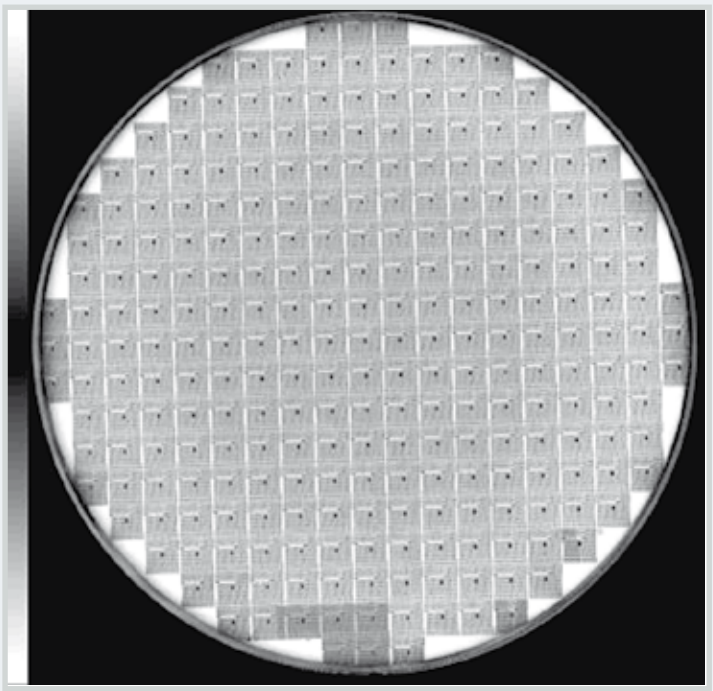


Figure 10:
Au to SiGe eutectic bond on 200mm silicon wafer. Acoustic image shows no voids or unbonded areas.

CONCLUSIONS

Eutectic alloy bonding is widely used in advanced packaging and MEMS device fabrication for hermetic seals. The processing temperatures of the various alloy choices are below 400C (except the Au-Ge system) and the selfplanarization of the molten metal make this type of bond a very surface topography tolerant method. Alignment methods can include IR, intersubstrate alignment, or backside alignment. The accuracy of the aligned features depends on the choice of alignment method, quality of the targets and thickness of the alloy layer. However, for metal layers 1µm thick or less alignment accuracies of ~2 µm can be expected.

It is expected that eutectic alloys will gradually replace some of the glass frit sealing technologies in applications that require device scaling to smaller packages and for integrated devices. The methods and materials systems described here should give some insight into what the possibilities can include.

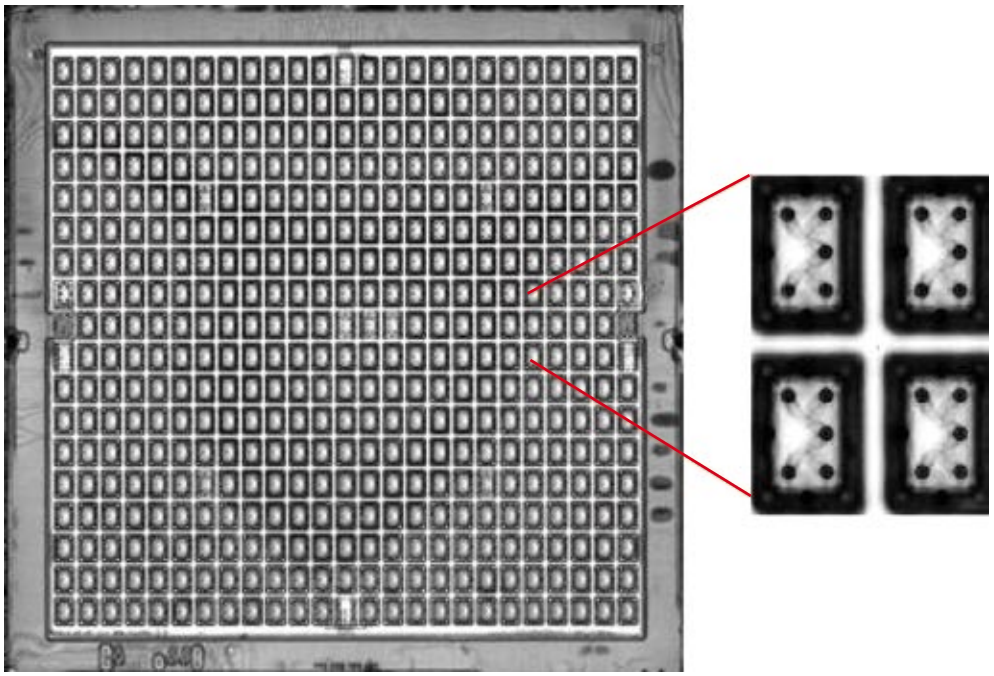


Figure 11:
Ceramic packaging using Au-Sn eutectic bonds

DR. SHARI FARRENS
is the inventor of plasma activated substrate bonding and holds several patents for this enabling technology. Dr. Farrens has authored and co-authored over 100 publications on SOI, wafer bonding and nano-technology. With over 15 years of hands-on, worldwide experience in academia and industry she is considered an expert on MEMS and wafer to wafer bonding technologies.

SUMANT SOOD
is the Senior Applications Engineer for Wafer Bonders at SUSS Microtec Inc.. His recent experience includes development of plasma enhanced wafer bonding processes for SOI and strained silicon on Insulator (sSOI) applications. Sumant has authored and co-authored more than 15 papers in wafer bonding, SOI, strained silicon and related areas. He received his B.Tech in Electrical Engineering from Punjab Technical University, India and MS in Microelectronics from University of Central Florida.

REFERENCES

1. Thaddeus B. Massalski, Binary Alloy Phase Diagrams, 2nd Edition, ASM International, Materials Park, Ohio, Vol. 1, 1990, p. 434.
2. Eric Laine, et.al., “C4NP – Reliability and Yield Data for Lead Free Wafer Bumping”, IMAPS Device Packaging Conference, Doubletree Hotel, Scottsdale, March 17, 2007.
3. K. Ruhmer et al., “C4NP: Lead-Free and Low Cost Solder Bumping Technology for Flip Chip and WLCSP”, IWLPC Pan Pacific Conference Oct. 2006, Wyndham Hotel, San Jose, CA.
4. S. Farrens, “Processing Solutions for Reproducible Submicron 3D Integration”, 3D Architectures for Semiconductor Integration and Packaging Accessing Technological Developments, Applications, and Key Enablers, Oct 22-24, 2007, Hyatt Regency San Francisco Airport Hotel, Burlingame, California. Proceedings to be published.
5. Mei Y, Lahiji G R, Najafi K 2002” A Robust gold-silicon eutectic wafer bonding technology for vacuum packaging”, Solid-State Sensor, Actuator and Microsystem Workshop, Hilton Head, SC, USA, pp. 772-4.
6. Mitchell J S, Lahiji G R, Najafi K., “Reliability and characterization of micropackages in a wafer level Au-Si eutectic vacuum bonding process”, Proc., ASME/Pacific Rim Tech. Conf. Exhibit Integration and Packaging of MEMS, NEMS, and Electronic Systems, InterPack05, San Francisco, CA, July 2005

Application Notes

Tips To Get The Most Out Of Data Viewer

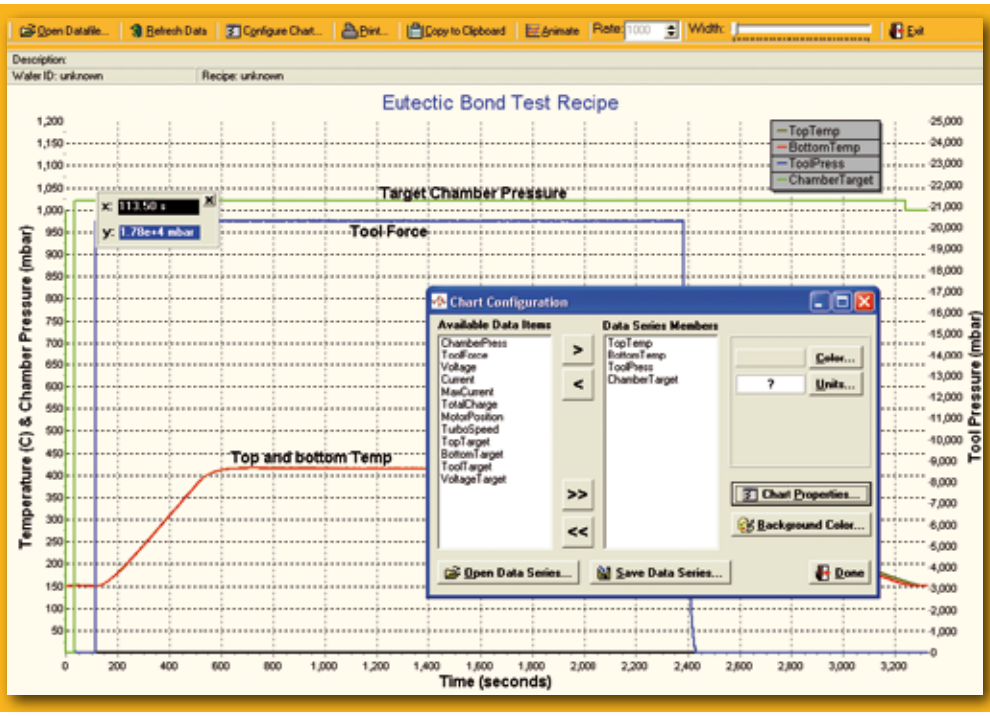


Figure 1:
Data Viewer Plot and Chart Configuration Window

The graphical user interface for all SUSS bonder products is called the Process Control Program (PCP) Navigator. One of the lesser used components available in this navigator is the "Data Viewer". It is accessed by clicking the Navigator Data button. The Data Viewer graphically displays the contents of selected process data files and allows customization and export of process data. This note will discuss the common and not-so-common but helpful functions available in the Data Viewer.

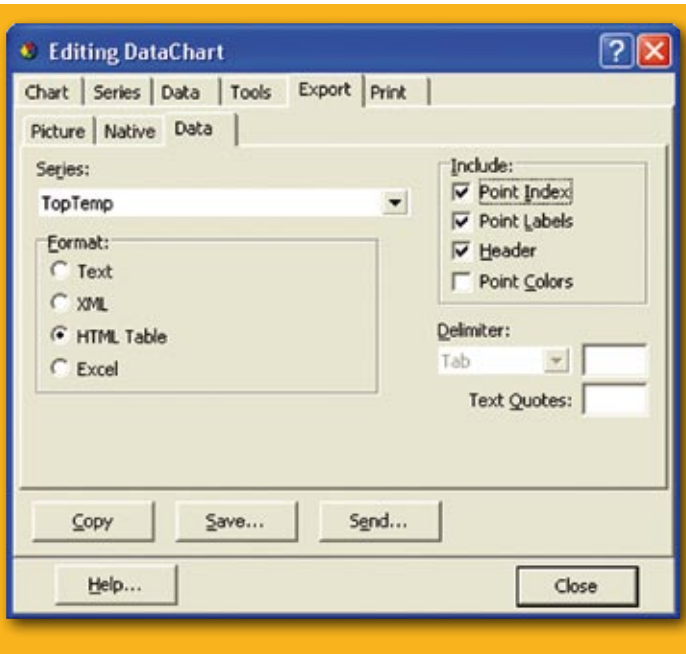


Figure 2:
Data Export

When the data viewer is first opened, all buttons are disabled (grayed out) with the exception of '*Open Datafile*' and '*Exit*'. Importing a data file to the viewer enables the remaining buttons.

CONFIGURING DATA VIEW

The Chart configuration window (Figure 1) is accessed by clicking the '*Configure Chart*' button. This window enables the user to plot the 'actual' and 'target' values of selected process data items vs. the bond recipe time. In addition to common bonding process parameters (top and bottom tool temp, chamber pressure and tool force), the user can also plot other data items such as Recipe Steps (RcpStep) and Recipe Action (RcpAction). RcpStep provides an easy way to view the actual process time spent at each step of the bond process and can be used to refine the bond recipe and improve overall process throughput. The actual value (X, Y value) of any plotted parameter can be viewed on the chart by directly clicking the line on the plot for that parameter.

EDITING CHART PROPERTIES

The '*Editing DataChart*' (Figure 2) window is accessed by clicking on the chart properties button in the '*Chart configuration*' window (Figure 1) and enables easy customization of chart data. All general chart edit functions such as data formats, axis titles and scales, and all plotted parameters can be edited by accessing the Chart and Series tabs in '*Editing DataChart*' window. The axis for any plotted data items can be changed by first selecting the relevant data series in the '*Series*' tab and then selecting the horizontal and vertical axis in the '*General*' subtab. In addition, the user has an option to plot the chart in 3D by accessing the '*3D*' subtab under the '*chart*' tab.

Figure 3:
Chart Tools Gallery

The '*Editing DataChart*' window also has extra chart customization tools that can be accessed by clicking on the '*tools*' tab (Figure 3). These tools allow the user to add extra legends, lines and text to the plotted chart without the need to export and customize the chart in an external application.

EXPORTING AND PRINTING DATA

Data export functionality is available from the Export tab on the '*Editing DataChart*' window as shown in Figure 2. Data Viewer allows export of process data in the following formats:

(a) Common data types (XML, HTML, Excel or delimited text).
(b) as an image (windows metafile or bitmap)
(c) native format

Using the functions of the Data Viewer discussed above will enable the SUSS bonder users to get the most out of their Data Viewer.

SUMANT SOOD
is the Senior Applications Engineer for Wafer Bonders at SUSS Microtec Inc.. His recent experience includes development of plasma enhanced wafer bonding processes for SOI and strained silicon on Insulator (sSOI) applications. Sumant has authored and co-authored more than 15 papers in wafer bonding, SOI, strained silicon and related areas. He received his B.Tech in Electrical Engineering from Punjab Technical University, India and MS in Microelectronics from University of Central Florida.

Anton Wolejnik, Managing Director, SUSS MicroTec Reman GmbH

New Office in USA

Introducing the Certified Remanufactured line of SUSS quality products now in the United States.

SUSS Remanufactured and Certified tools are completely reconditioned by expert technicians who use genuine spare parts and state-of-the-art testing methods to assure 100% conformity to original specifications. Tools are fully upgraded to meet today's safety standards, include current and licensed system software, warranty and may offer technology not available when the original equipment was sold.

SUSS MicroTec opened its North American Remanufacturing division on May 5 in a location only a few miles from the SUSS Wafer Bonder production facility in Waterbury, Vermont. The new site and staff will focus primarily on the remanufactured equipment business, such as locating and repurchasing SUSS tools and supporting North American sales of remanufactured SUSS equipment.

Technical support will also play an important role for this office enabling the SUSS service teams to focus on current models of equipment platforms. The Reman division will provide the full spectrum of support on all remanufactured and older models of SUSS tools.

The site will be managed by Glenn Walker in his function as Business Manager Remanufactured Equipment North America. Glenn works closely with the SUSS ReMan headquarter in Oberschleissheim, Germany and SUSS MicroTec Inc. in Waterbury, Vermont.

Though spare parts for remanufactured and older tools will be provided by the German site, North American customers will be working with the new office in Waterbury to get a quotation for the parts they need. The offices will also support each other in tool location and sales worldwide.

North American customers interested in purchasing SUSS Remanufactured and Certified Equipment should contact their local Sales Account Manager. If you are not sure who that is, please visit www.suss.com or email info@suss.com. Customers who need technical support on older SUSS equipment should contact our Technical Support Hotline at 1-800-TOP-SUSS (867-7877), please give the attendant the model and serial number of your tool and you will be directed to the specialist for that piece of equipment. Customers wishing to trade-in or sell a piece of older equipment can either contact their local Sales Account Manager or Glenn Walker at glenn.walker@suss.com.

Remanufactured MABA 6

Clif's Notes

You Can Define That Exposure Dose In One Wafer!

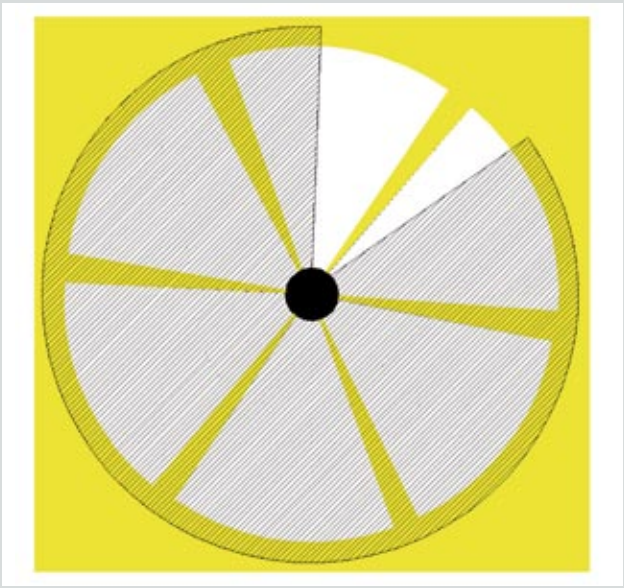


Figure 1: SUSS Exposure Test Dial View

INTRODUCTION

There are many ways to determine the best exposure dose for a SUSS 1X full field aligner. Many times it seems easiest to just run a group of wafers each at a different exposure time. This method however takes time and resources which adds cost to process. There are some very simple and easy methods to reduce the cost of an evaluation yet still provide the most information at the least cost.

One method which may be used for thin resist films involves the use of the SUSS exposure test dial while the second method uses a simple low cost step wedge. This second method also makes short work of those thick film exposures taking sixty or more seconds. Each of these methods will be discussed in detail.

SUSS EXPOSURE DIAL

This unit is comprised of two pieces of metal held together in the center slightly larger than the wafer to be exposed. The lower piece has six cut outs in the shape of a wedge while the top piece has one wedge shaped cut out. The top piece may be rotated about the center to allow light to pass thru each individual wedge, Figure 1 for example, shows a test dial with top piece rotated between two wedges. The beauty of this method is that you can do all of your testing with the mask of your choice, no special mask is required. You may do up to six exposures on one wafer with each exposure at a different time or condition. For example, suppose you wish to evaluate the changes in sidewall profile under different exposure conditions such as proximity gap of say 0, 15, 20, 40, 80, 160 µm. You simply place the dial on top of the mask of your choice, set the wedge position, cycle the wafer thru the tool then rotate the dial and repeat until all six conditions are completed. You now have one wafer which has been exposed with your mask pattern at six different conditions! If only the exposure time is to be changed SUSS has a special feature on its aligner called 'exposure test mode'. Using the mask of your choice with this mode a wafer is brought to exposure gap and will remain there for as many exposure cycles as you wish. Thus you simple place the exposure dial at one wedge position and cycle the shutter for the desired time. Rotate the wedge to the next position, change the exposure time and cycle the shutter again. This is repeated for each wedge until you have obtained your six exposures and unloaded the wafer. Develop the images and you now have six exposure conditions on one wafer.

For thin films this procedure works very nicely and takes a very short time, however, with thicker films requiring sixty or more seconds each this could be a very time consuming operation. There is no doubt that it will work, it is just that it will take such a very long time. There must be a faster way to do this and there is!

THE STEP WEDGE

When time is of the essence and you can do only one exposure cycle then you need to use a step tablet which has been used in the printing industry for many years. It is basically a strip of plastic with different levels of transmission similar to that shown in Figure 2 where amount of light passing thru the tablet will be reduced in steps from zero to one-hundred percent.

In normal use the tablet is placed on the object to be exposed i.e. your mask then the shutter is turned on for a given time thus producing as many exposu-

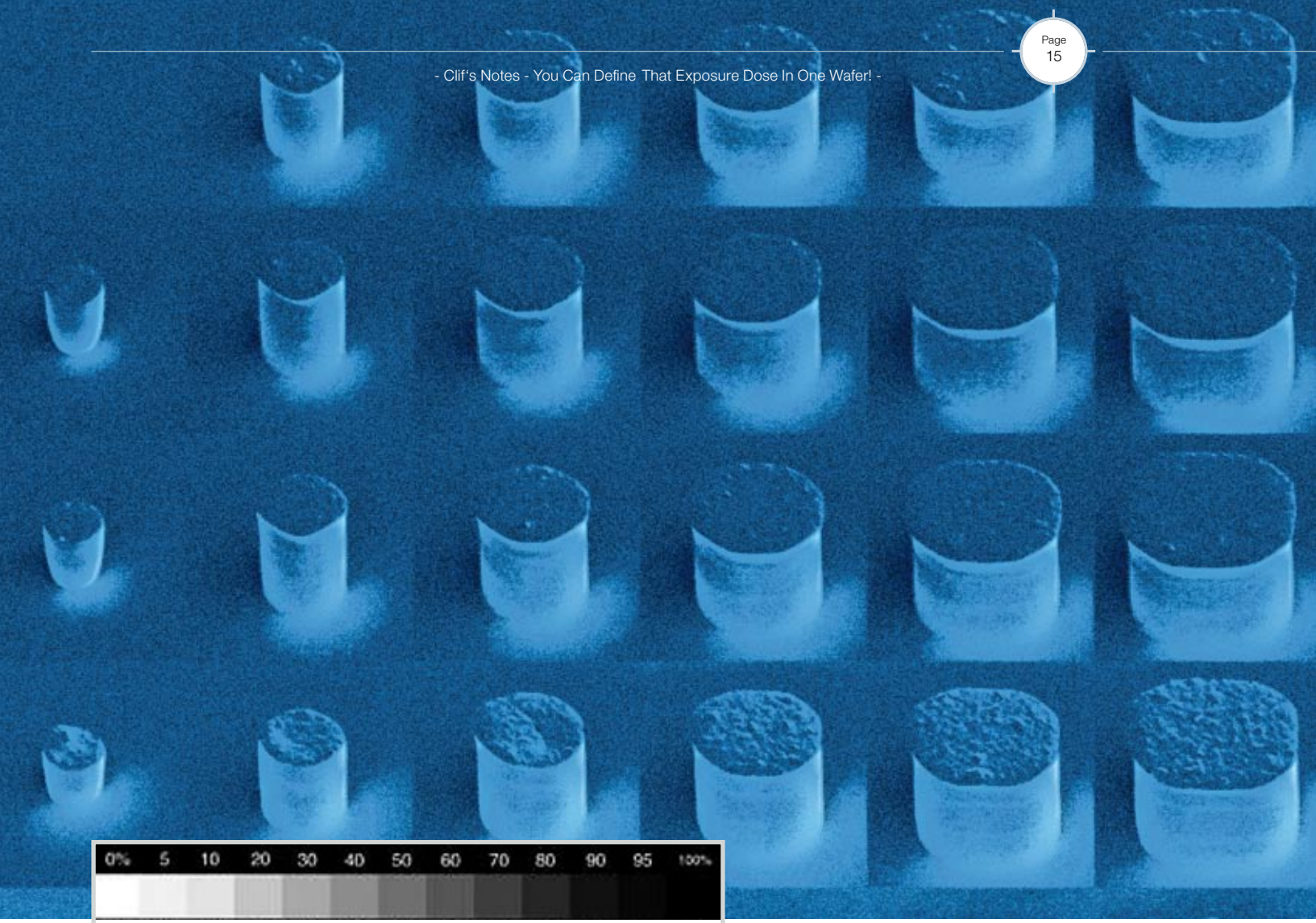


Figure 2: Transmission Step Tablet

re levels on the substrate as there are steps on the tablet. Thus if you need to evaluate your mask pattern with say three exposure modes, proximity, soft and hard contact, as a function of exposure dose you only need three substrates to complete the test!

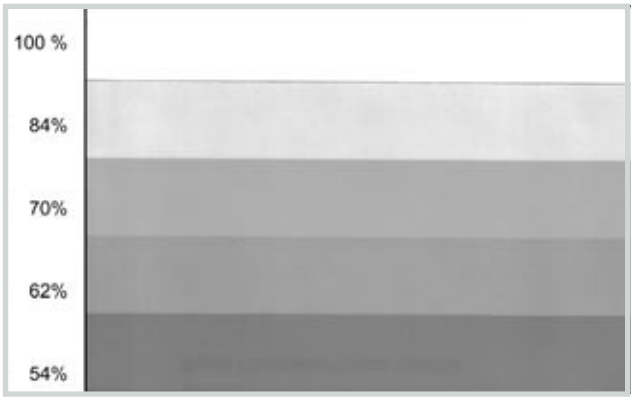
For semiconductor use ten exposure steps is far too many to be practical so SUSS has modified the step tablet1 to have at most four to six steps similar to those shown in Figure 3. The four step tablet has been defined in the shape of a pie chart similar to the exposure test dial. These step tablets will allow for an investigation of exposures from about fifty to one-hundred percent of the incident exposure intensity.

Typical changes in exposure intensity for each step tablet type that SUSS uses are shown Table 1.

WHAT EXPOSURE TIME?

A most important question is how to define the proper exposure steps to be used with the test dial or the step tablet. In most cases it is quite easy and may require you to use at most two wafers to find the correct range. First, most thin resists of say one to five microns thickness will require about 75 mj/cm^2 dose per micron of resist. Thus, simply multiply this value times the film thickness and divide by the light intensity to obtain the nominal exposure time. The light intensity will be measured as the broad band ultraviolet light covering a range between 330 to 450 microns, typically the SUSS 405nm probe. This nominal exposure time will be midway between the lowest and highest exposure times to be used with the test dial or step tablets. A sample calculation for a typical thin and thick film is shown in Table 2 below using the percent transmission values from Table 1. The goal is to insure that the steps used will cover a range of about fifty percent of the total exposure time. The steps will typically be about twenty percent of the nominal exposure. Smaller steps have not proven to be any more useful while larger steps may be used if the characteristics of the resist are not well known.

Figure 3:
SUSS Step Tablet



	Step Wedge, % Trans	
	Pie	Steps
None	100 %	100 %
1	81 %	81 %
2	66 %	68 %
3	54 %	63 %
4	-	53 %
5	-	46 %

Table 1: Typical Light Intensity By Tablet Type

CLIFF HAMEL

is the principle applications engineer at SUSS MicroTec, Inc. for lithography processes involving full field mask aligners and automated cluster coating equipment. Over the last ten years at SUSS he has co-authored several papers in the field of thick resist processes and process optimization. He has over 26 years of BEOL process and mask fabrication experience at IBM where he was the principle engineer and inventor for lift off process development. He received his BS in chemical engineering at Trinity College of Vermont.

SUMMARY

In summary, using one of two possible methods on the SUSS 1x field aligner it is possible to evaluate the exposure dose on your mask using only one wafer, for an example see Figure 4. Using the SUSS exposure test dial also allows you to evaluate up to six exposure modes on a single wafer.

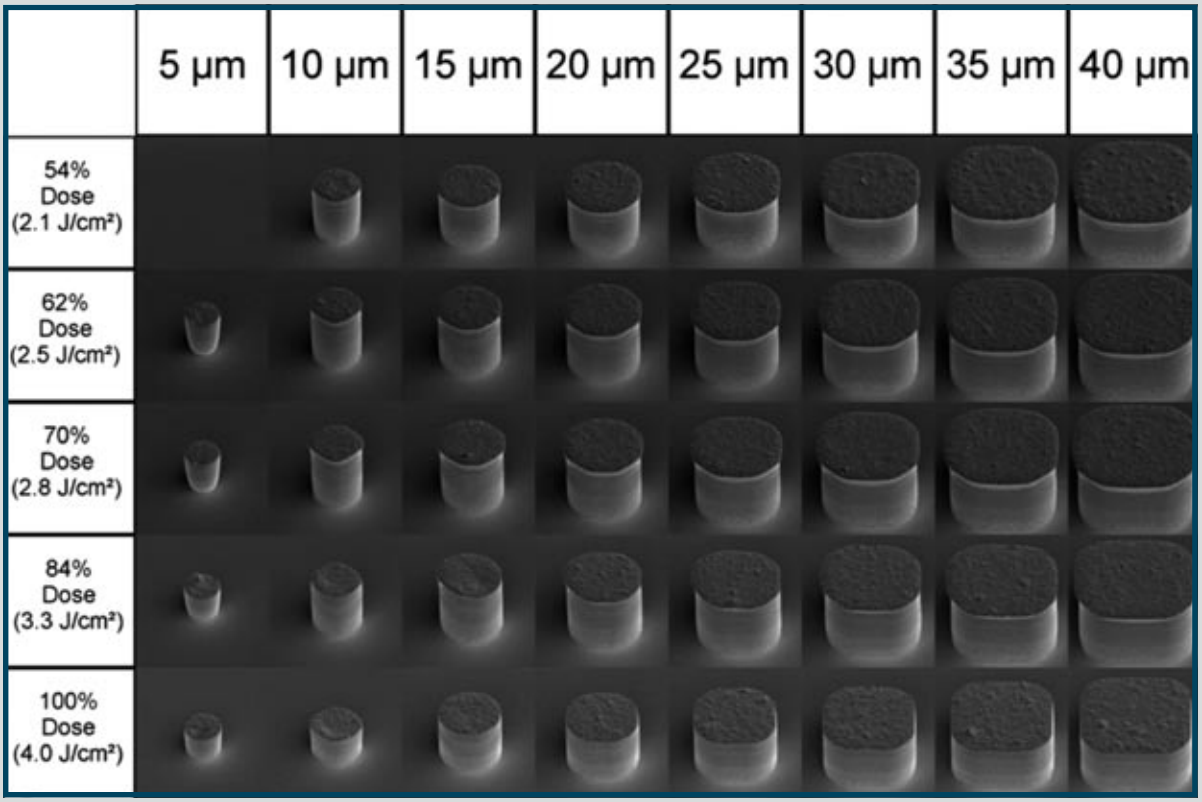


Figure 4:
Step Tablet Image Size Evaluation AZ50XT, 50µm Thickness, Copper Plate, Design to Substrate Image is approx +13µm.

Table 2:
Calculating the Steps

	Resist Film		
	Thin	Thick	Units
Film Thickness	1.2	20	µm
Dose per Micron of Resist	75	55	mj/cm²/µm
Nominal Dose	90	1100	mj/cm²
UV Light Intensity	70		mw/cm²
Nominal Exposure Time	1.3	15.7	seconds
Using Percent Transmission from Table 1			
No Step	1.9	24.9	seconds
1	1.6	20.2	seconds
2	1.3	17.0	seconds
3	1.1	15.7	seconds
4	-	13.2	seconds
5	-	11.5	seconds

Scaling in 3 Dimensions

Maximize Your Wafer's Real Estate

Your success in the third dimension relies on innovative technology. SUSS technology is leading the way in the advancement of 3D applications with innovative equipment solutions enabling the development of production-ready 3D processes. Our commitment to superior performance will prepare your business for the next dimension.

- **3D Lithography**
- **Micro-Bumping**
- **Wafer-to-Wafer-Bonding**
- **Thin Wafer Handling**

SÜSS MicroTec

SUSS in the News

Here's a summary of our recent press releases. To read the entire press release, please visit www.suss.com/about_suss/latest_news

Jan 14, 2008 · SUSS MicroTec Lithography Quality Management Now Certified According to ISO 9001 : 2000

SUSS MicroTec Lithography GmbH now holds the globally recognized ISO 9001 certification for having established a high level process- and system-oriented quality management (QM) based on ISO 9001 quality standards. The certificate is evidence of SUSS MicroTec Lithography's commitment to provide consistent high-quality development, production and service processes at both German manufacturing sites in Garching (near Munich) and Vaihingen/Enz (near Stuttgart).

Jan 16, 2008 · Freescale Selects 200mm SUSS Tool Set for MEMS Facility

SUSS MicroTec announced it has shipped and successfully installed several microelectromechanical systems (MEMS) production tools at Freescale Semiconductor. The equipment included a new DSM200 Series Front-to-Back Alignment Verification System, the latest generation SUSS MA200Compact Mask Aligner as well as a SUSS ABC200 series Wafer Bond Cluster system for use in MEMS sensor applications.

With shrinking design rules, MEMS devices must be produced with higher precision and accuracy to ensure reliability and the required performance. With an accuracy of 0.2 micron at 3 sigma, the DSM system demonstrates excellent measurement results in automated mode. Working in concert with the SUSS Compact series mask aligner, these two machines represent the perfect package for double-sided alignment and exposure applications frequently used in the manufacturing of MEMS, power semiconductors and optoelectronic devices.

Feb 12, 2008 · SUSS MicroTec AG appoints new VP Sales

SUSS MicroTec has appointed Thomas Breser to the position of Vice President Sales. Thomas Breser comes to SUSS with almost 20 years international experience within the semiconductor industry. He has held positions in general management, sales management, business development, product planning and strategic marketing.

March 3, 2008 · SUSS MicroTec Boosts Nanotechnology with New Toolset for Mask Aligners

SUSS MicroTec has launched an advanced nanotechnology toolset for its Mask Aligners. The new Nano Imprint Lithography (NIL) tool enables SUSS Aligners to print resist thicknesses from less than 100 nanometers to a few hundred microns with a printing resolution down to a few nanometers. UV-NIL is a low-cost production technology that is based on UV-curing. It has been developed as a cost-effective alternative to high-resolution e-beam lithography to print sub-20 nanometer geometries. UV-NIL applications with promising perspectives include semiconductor, MOEMS, NEMS and optoelectronic technologies.

April 8, 2008 · SUSS MicroTec Installs First 300 mm WLR Test System in Japan

SUSS MicroTec announced the installation of its PM300WLR, the world's most advanced 300 mm wafer-level reliability (WLR) test system, at a leading Japanese manufacturer of semiconductor devices. It will be used for testing the reliability of current and next-generation devices.

As the technology and design of semiconductor devices advance, the need to test their reliability and gauge their lifetime becomes acuter. Common reliability tests, such as electromigration (EM) and time-dependent dielectric breakdown (TDDB), require the device under test (DUT) to be put under thermal and electrical stress over long periods of time to accelerate failure mechanisms. Before the PM300WLR, these measurements were carried out after the DUT had been packaged, a costly process that delays time to data and lengthens the device design cycle. By moving these tests to wafer level with the PM300WLR, reliability data is obtained sooner, and the device design cycle and thus time to market can be improved significantly.

April 29, 2008 · SUSS MicroTec Signs License Agreement with Philips Research to develop a New Nano Imprinting Technology: Substrate Conformal Imprint Lithography (SCIL)

SUSS MicroTec has entered a license agreement with Philips Research, Eindhoven/The Netherlands, for a new enabling technology called Substrate Conformal Imprint Lithography (SCIL). The aim of this cooperation is to bring an existing equipment platform with this additional Nanoimprinting (NIL) feature to the market, enabling new approaches to large-area imprint applications along with excellent printing resolution and repeatability.

This new imprint technology for sub-50nm patterning is bridging the gap between small rigid stamp application for best resolution and large-area soft stamp usage with the usual limited printing resolution below 200nm. SCIL is an enabling technology offering the best of two worlds – large-area soft stamps with repeatable sub-50nm printing capability, avoiding stamp deformation as no contact force is applied, non-UV based curing at room temperature and allowing high aspect ratios even up to 1:5 and more.

May 29, 2008 – SUSS Automated Bond Cluster Selected for MEMS Foundry in Korea

SUSS MicroTec,announced that u-ITC, Korea, has selected the advanced wafer bonding equipment of SUSS for its MEMS foundry.

u-ITC is a world class MEMS foundry specializing in MEMS sensors. The Incheon facility will incorporate design, manufacture, assembly and test within one location for the growing fabless MEMS market.

"The SUSS ABC200 Automated Bond Cluster is a key acquisition for our foundry operations," said Suh, Dong-Ryang Ph.D, Director at u-ITC, "we can easily meet our customers' needs by using a cluster tool that can be quickly reconfigured for changing process conditions."

"The flexibility of the SUSS bond cluster to quickly reconfigure process parameters from small runs to full production is a big advantage of the toolset, especially in the case of a foundry serving new markets," said Daniel T. Hurley, International Product Manager, Wafer Bonder Division, SUSS MicroTec. "We are pleased to support u-ITC as they establish themselves as the primary best in class MEMS foundry in Korea."

The ABC200 is a 200mm Automated Bond Cluster. It delivers superior post-bond alignment accuracy resulting from precision mechanics, uniform force capability and leading edge temperature control. SUSS MicroTec offers advanced wafer bonding solutions for the MEMS, SOI, Optoelectronics, and 3D Interconnect markets.

June 26, 2008 · SVTC Technologies Selects Processing Tools from SUSS MicroTec

SUSS MicroTec, Inc. announced that a suite of processing tools that enable new generations of micro-electromechanical systems (MEMS) has been selected for SVTC Technologies' facility in Austin, Texas.

As a key supplier to SVTC, SUSS MicroTec also will provide joint development and support for process and tooling. The SUSS toolsets at SVTC include manual and automated platforms to perform lithography and bonding - two of the critical process steps in the creation of MEMS devices. SVTC, a leading independent semiconductor process-development foundry, will use these tools to provide process solutions and a prototyping foundry for emerging MEMS and other devices.

"The SUSS toolset represents the latest technology - giving our customers the opportunity to lead the way for emerging MEMS devices," said Dave Bergeron, chief executive officer of SVTC.

MEMS devices have been instrumental in creating many state-of-the-art products for the consumer, healthcare, automotive and entertainment industries. Expected to increase at a 13 percent compound annual growth rate through 2010, MEMS are the enabling technology behind many well-known applications such as inkjet printing, automobile air bags, global positioning systems and motion sensing game controllers. Future markets to be opened by MEMS technology include fuel cells, combustion optimization, drug discovery and delivery systems, as well as next-generation navigation and gaming systems.

"We are very pleased to be chosen by a high-quality organization such as SVTC and are excited about the possibilities that this partnership brings to SUSS MicroTec and our customers", said Dr. Stefan Schneidewind, CEO

of SUSS MicroTec. “The MEMS industry has long been a focus for our company. The opportunity to partner with such highly respected forward-looking organization as SVTC will only strengthen our ability to service our growing customer base and our position as a leading equipment supplier to the MEMS market.”

July 1, 2008 · SUSS MicroTec Leads Ranking of 10 Best Material Handling Suppliers for the 10th Year

SUSS MicroTec has been ranked again among the best suppliers in the 2008 VLSI Research 10 BEST Customer Satisfaction Awards. Customers rated SUSS Micro Tec first among the Material Handling Suppliers and fifth among Small Suppliers of Wafer Processing as well as eighth among the overall category Focused Supplier of Chip Making Equipment. The survey’s respondents represent 95% of the world’s semiconductor market.

By securing a number one ranking for the tenth year in the category Material Handling Suppliers in which the company’s probe systems are featured SUSS MicroTec has significantly extended its lead in the field of customer satisfaction. Customers selected SUSS as best in Cost of Ownership, Uptime, Build Quality, Usable Throughput, Quality of Result, Product Performance and Commitment thus making SUSS first in seven of the thirteen categories.

In the category Small Suppliers of Wafer Processing Equipment SUSS MicroTec was awarded fifth. Again, customers rated SUSS best for Build Quality and ranked SUSS among the first three within the categories Quality of Results, Uptime and Product Performance.

“Our continuous success shows that our customers highly value the quality and customer support from SUSS.” said Dr. Stefan Schneidewind, CEO of SUSS MicroTec AG.” Clearly, our customers appreciate our high-level application expertise and superior performance they have come to expect from us. We are dedicated to further proving ourselves as reliable partner and returning their trust with on-going commitment.”

Are TSVs the Future of Advanced Packaging?

by Julia Goldstein, Ph.D.

Julia Goldstein, Ph.D. has been technical editor of Advanced Packaging magazine since 2001. She received a B.S. in engineering from Harvey Mudd College, and M.S. in materials science from Stanford, and a Ph.D. in materials science from U.C. Berkeley. Julia has worked as a process development engineer at nCHIP, where she developed a flip chip process for multichip modules. Since 1996, she has been a technical consultant in areas ranging from flip chip bumping to thin film coatings. Julia has authored 11 technical publications, and is a member of IMAPS and MEPTEC.

May 22, 2008 San Jose, CA

The “3D Integration North American Tour” came to San Jose on May 15 after stops in Durham, NC and Dallas, TX. The event, hosted by **SUSS MicroTec, Surface Technology Systems** (STS) and **NEXX Systems** outlined the current state of the art in through silicon vias (TSVs) and related technology. An overview by consultant Phil Garrou, Ph.D. of MCNC describing various process steps involved in 3D TSV technology led naturally into detailed presentations on processes and materials.

The primary application for this technology today is CMOS image sensors, with DRAM stacked memory as the next high volume application. Garrou showed a roadmap that predicted completely heterogeneous stacks with via sizes around 2 µm by 2014. As Garrou noted, many industry leaders, ranging from image sensor and memory manufacturers to IDMs, foundries and SATS companies, are involved in or have included roadmaps for 3D activity.

Stephen Vargo, Ph.D., applications manager at STS, discussed the via etching process. He focused on methods to improve etch rates without producing rough sidewalls that negatively impact via fill. Designs with a variety of via sizes are still a major challenge.

The via fill process is the most expensive step in the TSV process and the most time-consuming. Advances in Cu plating chemistry, as presented by Dr. Yun Zhang, R&D and technical marketing director at **Enthone**, improve throughput for a wide range of via sizes while producing void-free vias. Arthur Keigler, VP of technology at NEXX Systems, explained how agitating the plating fluid near the wafer promoted bottom-up filling, eliminating voids at the bottom of vias. He also advised using electrochemical deposition to deposit the seed layer, reducing overall cost. For very large vias, Bob Forman of **Rohm and Hass** discussed a combination of Cu-plated liner and polymer plug to reduce total fill time. Forman also mentioned indium plating as an option for applications that require lower temperature processing.

Memory manufacturers emphasized performance limitations of wire-bonded stacked die solutions for future generations of DRAM. Kyle Kirby, senior process integration engineer at **Micron**, showed a roadmap of TSV trends for memory with via sizes decreasing below 5 µm and density increasing to 1000 I/O per device. Challenges in moving toward this goal include routing between die on different levels (design tools are not really ready for 3D integration) and overcoming thermo-mechanical stresses as via spacing decreases. Bob Patti, CTO of **Tezzaron**, proposed a solution that de-couples the controller from the memory functions in separate layers, decreasing the number of TSVs required. He also discussed increased use of built-in self test and stacking using a template, achieving a hybrid between wafer-wafer and die-wafer bonding that allows the use of KGD with reasonably high throughput. Both of these approaches improve overall yield of a wafer stack.

The current state of the art in wafer aligning, bonding and thinning, also discussed at the seminar, seem sufficient to enable further development of 3D processes. Kirby stated that, “TSVs are the future of advanced packaging.” That may be true, but it remains to be seen whether 3D IC integration will bring about the death of wire bonding, as flip chip promised to do years ago.

This column is reprinted with permission from Advanced Packaging Magazine.

Some of the opportunities to meet with SUSS MicroTec in the upcoming months:

July

- **IPFA** · July 07 - 11, 2008
- **Semicon West** · San Francisco, CA, USA · July 15 - 17, 2008
- **MIG** (MEMS Industry Group) **Education Series** · San Francisco, CA, USA · July 18, 2008
- **Micromachine** · MEMS · Tokyo, Japan · July 30 - August 01, 2008

August

- **Nano Korea** · Nano · Seoul, Korea · August 27 - 29, 2008

September

- **ESTC** · Greenwich, UK · Sept 1 to 4, 2008
- **Semicon Taiwan** · Taipei, Taiwan · Sep 09-11, 2008
- **LED Seminar Semicon Taiwan** · Taipei, Taiwan · Sep 11, 2008
- **MNE08** · Athens, Greece · Sep 15 to 18, 2008
- **Micronora** · Besancon, France · Sept 23 to 26, 2008
- **MME** · Aachen, Germany · Sep 28 to 30, 2008
- **ESREF** · Maastricht, Netherlands · Sep 29 - Oct 02, 2008

October

- **Semicon Europa** · Stuttgart, Germany · Oct 07-09, 2008
- **ABMS Seminar** · Kitakyushu, Japan · Oct 8-10, 2008
- **ECS Fall Meeting/PRIME** · Honolulu, Hawaii · Oct 12-16, 2008
- **European Microwave Week** · Amsterdam, Netherlands · Oct 27-31, 2008
- **SUSS Seminar** · Tokyo, Japan · Oct 29, 2008
- **SUSS Seminar** · Shanghai, China · Oct 31, 2008

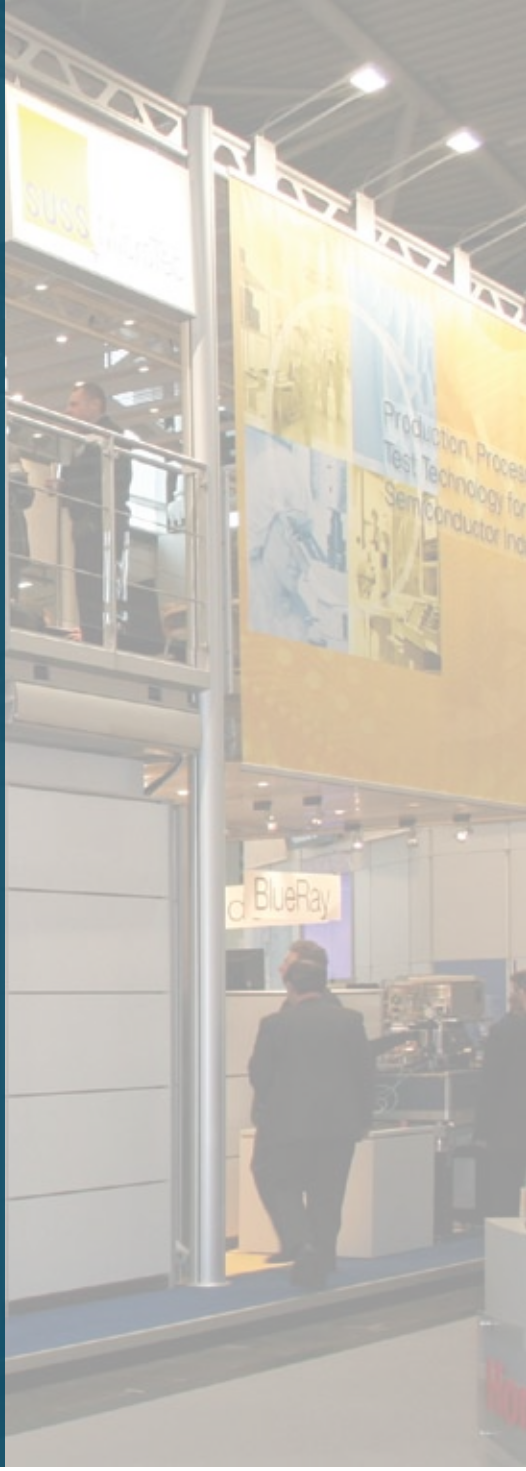
November

- **ISTFA** · Portland, OR, USA · Nov 2-6, 2008
- **SUSS Seminar** · Seoul, Korea · Nov 3, 2008
- **SUSS Seminar** · Taipei, Taiwan · Nov 5, 2008
- **MEMS Executive Congress** · Monterey, CA, USA · Nov 5-11, 2008
- **SUSS Seminar** · Singapore · Nov 7, 2008
- **RTI-3D** · Burlingame, CA, USA · Nov 17-19, 2008
- **Microwave** · Yokohama, Japan · Nov 26-28, 2008

December

- **Semicon Japan** · Chiba, Japan · Dec 03-05, 2008
- **ARFTG** · Portland, OR, USA · Dec 9-12, 2008
- **Sponsor MRS** · Boston, MA · Dec 12, 2008
- **APMC** · Hong Kong · Dec 17-19, 2008

Please check our website for any updates: www.suss.com/events



We hope you found this edition of the SUSS Report interesting and informative.
For more information about SUSS and our products, please visit

www.suss.com

or write to **info@suss.com** with your comments and suggestions.

SUSS MicroTec AG
Schleissheimer Strasse 90
85748 Garching near Munich
Germany

SUSS. Our Solutions Set Standards

SÜSS MicroTec