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Process Solutions for Wafer Level Camera Manufacturing

have led the way in the adoption of 3D interconnect using through silicon vias because of the enhancement in image quality and the reduction in size that is possible using this technology. 3D integration has enabled improvements in image sensor technology that would not otherwise be possible.

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Full View

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Vice President
Strategic Business Development,
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Taking a Snapshot

The Wondrous World of Wafer Level Cameras

Digital cameras have revolutionized the way we take pictures. We can now take instant, high quality photos that can be edited quickly and easily at a low cost. Taking digital photos with our phones has changed our lives. Experiences we have can be transmitted to anyplace in the world within seconds.

Whether we take a photo on vacation and want to instantly share it with co-workers miles away, or need to take a photo of a car part and send it to a mechanic because we are unable to identify the part, camera phones allow us to capture images at any time and the wireless connection allows for immediate transmission of content.

According to CTIA research, camera phones are the fastest growing consumer electronics product in history. By 2003 more camera phones were sold worldwide than stand-alone digital cameras. In 2004 Nokia emerged as the brand with the most digital camera sales. In 2006 half of the world's mobile phones had a built-in camera. The decline of 35mm film has accelerated quickly and in 2008 Nokia sold more camera phones than Kodak sold film-based cameras. These conditions helped make Nokia become the biggest manufacturer of any kind of camera. The growth spurt of cameras does not only apply to mobile phones but extends to notebooks, PDAs and other devices.

However, in spite of its popularity there are shortcomings in the current generation mobile phone camera. Picture quality is sufficient for viewing on the mobile device but lacks the resolution for viewing on larger screens or printing. Light sensitivity and contrast need to be improved when compared to dedicated digital cameras. This is where advances in technology come to the rescue. The well described backside illumination for CMOS image sensors significantly improves the contrast and light reaching the sensor compared to conventional designs. Wafer to Wafer bonding is the enabling technology for this application and this marks its entry into the manufacturing process.

Size of the image sensor has been a compromise between form factor for integration and performance of the image sensor. New packaging technologies, in particular wafer level cameras (WLC), are the path to very compact, high performance cameras. A WLC, in a simplified definition, is manufacturing and stacking wafers with micro lenses and attaching the lens wafers to the CMOS image sensor wafers. The camera wafers are then separated into the individual camera modules.

Not only do these wafer level cameras provide the performance required for mobile phone integration, but they also significantly drive down the cost. This in turn will increase the adoption rate of cameras in mobile phones.

The next development we will see in this fast moving market is secondary cameras in mobile phones for video calls. While a camera on the back of the phone is for taking pictures, cameras on the front will show video during a call. Solution providers like SUSS MicroTec make this advance in technology possible by developing a complete solution suite that includes manufacturing equipment and test systems for image sensors. We are only one click away from another wonder in the world of wafer level cameras.

Process Solutions for Wafer Level Camera Manufacturing

Made by SUSS MicroTec

Margarete Zoberbier and Kathy Cook, Business Development Manager, SUSS MicroTec

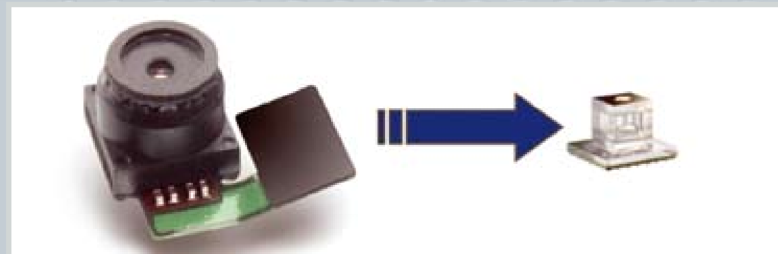


Figure 1
On the left:
Camera module made by using traditional semiconductor and packaging technology,

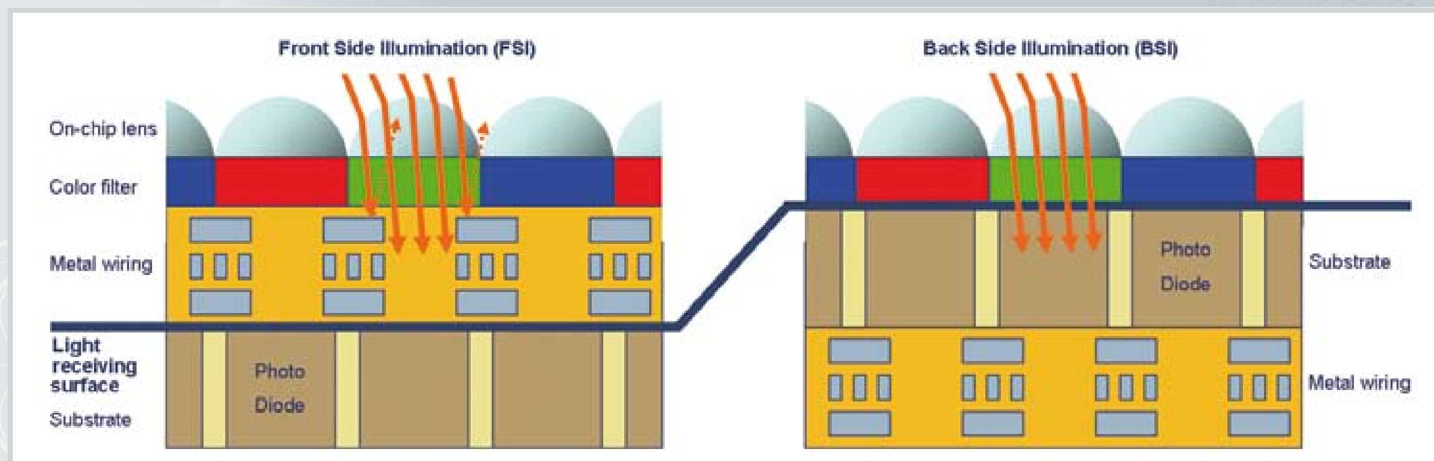
On the right:
A camera module made using 3D interconnect technology. (Source Tessera)

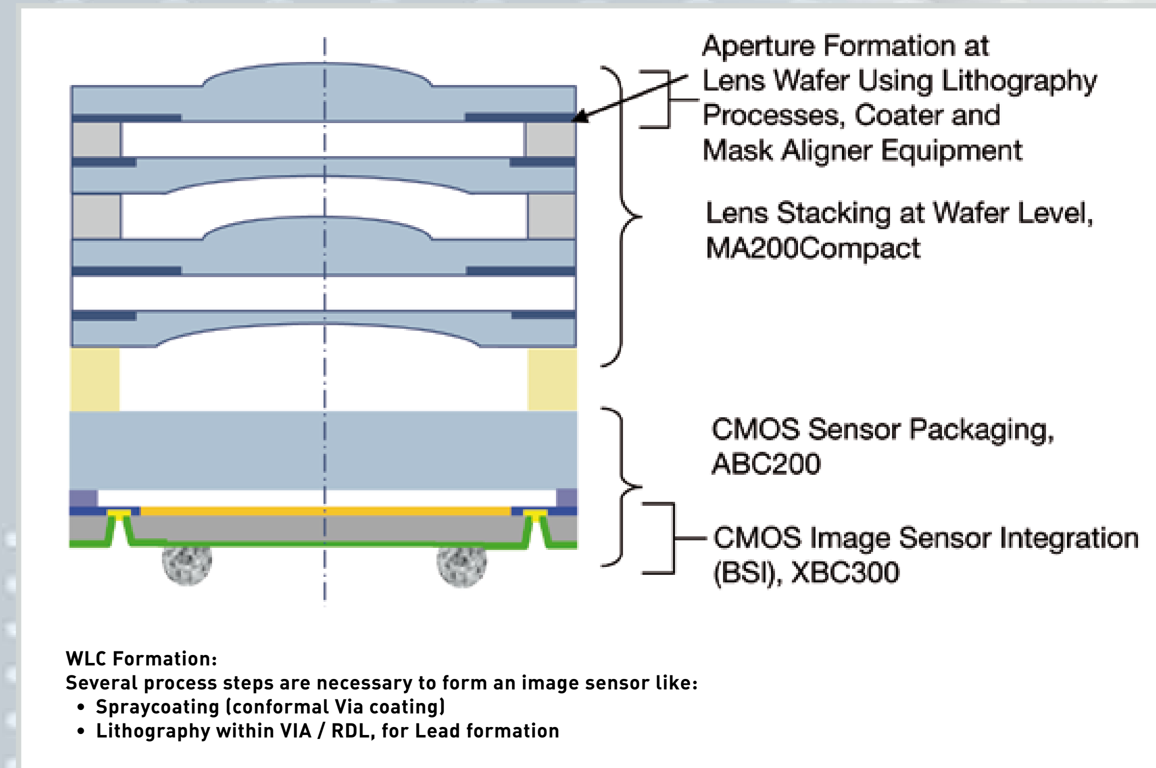
Due to increasing interconnect densities and the rising cost of IC manufacturing in leading edge technology nodes, 3D architectures for IC integration and packaging are becoming viable alternatives to traditional semiconductor manufacturing. Through silicon vias (TSV's) are a key component in 3D integration technology. TSV's improve electrical performance, reduce power consumption, shrink device sizes and potentially lower costs.

3D interconnect user applications include CMOS Image Sensors, Memory, Mixed Signals, FPGA (Flexible Program Gate Array), and Microprocessors. CMOS image sensors have led the way in the adoption of 3D interconnect using through silicon vias because of the enhancement in image quality and the reduction in size that is possible using this technology (Figure 1). 3D integration has enabled improvements in image sensor technology that would not otherwise be possible.

For CMOS image sensors, the main motivation for using 3D integration is the improvement in image quality that can be gained by enabling the sensors to be illuminated from the backside of the device (Figure 2). In traditional image sensor manufacturing, the metallization layers cover the sensors reducing the total light that hits the sensors. Wafer bonding eliminates the need for the metal layers to cover the sensors, thus allowing more light to be collected. In addition, as can be seen in Figure 1, there is a form factor benefit that is realized when using TSV technology and Lens Stacking. Figure 3 shows a cross section of a Wafer-Level Camera (WLC). There are many steps involved in the manufacturing process, and SUSS MicroTec provides equipment solutions for most of these steps.

Figure 2
Principle of Back-Side Illumination





WLC Formation:
Several process steps are necessary to form an image sensor like:
- **Spraycoating (conformal Via coating)**
- **Lithography within VIA / RDL, for Lead formation**

Figure 3
Cross-section of a Wafer Level Camera

Image Sensor Formation:

Several different Lithography processes are part of an Image Sensor Formation. Coating, Exposure and Development steps are required to form a via, to process within the via itself, for Redistribution (RDL) and Lead formation. In some CMOS image sensors designs a conformal coating, done with a spray coater, is required.

CMOS Image Sensor Integration (BSI):

A novel technology, where the sensor is back side illuminated. Here a handling wafer needs to be bonded, using a low temperature direct bonding, to the device wafer.

Lens Stacking at Wafer Level: This is a UV-Bond process, done in a mask aligner, e.g. MA200Compact, where immediately after the alignment the UV-curing step is done.

CMOS Sensor Packaging:

Here the active sensor area needs to be encapsulated with a cover glass. This is typically done in a substrate bonder, e.g. using a adhesive and bond the glass to the CMOS wafer at wafer level.

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Ramm, Peter and Armin Klumpp, "3D-IC Fabrication Challenges for More Than Moore Applications," Presentation at Sematech Workshop, September 2008.

Margarete Zoberbier,

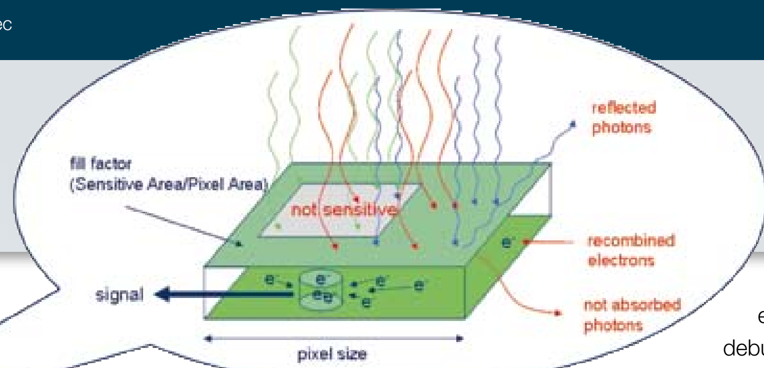
started at SUSS MicroTec in 2001 as Application Engineer Bonder, responsible for development and improvement of bonding processes. After being responsible for the Bonder Business Development in Europe, Margarete moved to the Business Development Group of 3D integration in 2008. Margarete co-authored several papers in wafer bonding and related areas. Zoberbier received a Master degree in Precision- and Microengineering field from Georg Simon Ohm University of Applied Sciences in Nuremberg, Germany.

Kathy Cook

has worked in various positions in the semiconductor industry before joining SUSS MicroTec five years ago. In her current position as Business Development Manager one of Kathy's primary points of focus is the emerging and rapidly growing 3D IC market. Kathy holds a Master of Materials Engineering degree at Auburn University.

CMOS Image Sensor Test at Wafer Level

Volker Hänsel, Product Engineer, SUSS MicroTec



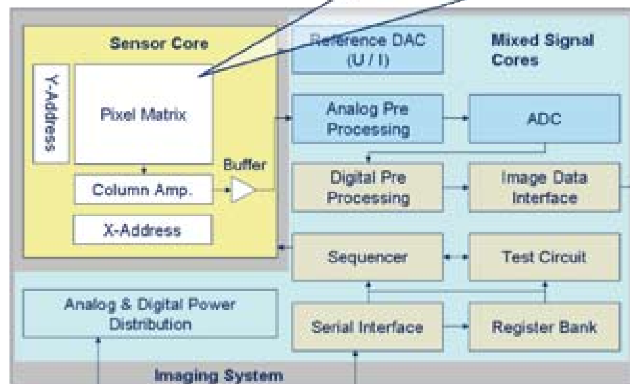


Figure 1
The mixed-signal system structure of the CMOS image sensor.

In the last few years, CMOS image sensors have conquered more and more applications in industry and automotive engineering. Optical test procedures provide valuable data to control processes more precisely and conserve resources. In automotive engineering, additional sensors in driver assistance systems contribute to higher safety and comfort. Image sensors capture street signs, road markings, detect objects in darkness and monitor the driver's alertness to prevent dangerous microsleep.

The detection, identification and monitoring of objects require image sensors, which are able to capture fast moving objects but also cope with difficult light conditions. A prime example of the extreme light conditions that can be encountered is during night-time driving situations. In such dark conditions, the headlights of oncoming traffic could overexpose the sensor.

The semiconductor manufacturing processes currently used to produce CMOS image sensors enable application-specific and customized sensors to be manufactured with minimal effort. Of course, the costs for such specially developed sensors are a central concern. Design cycles must be minimized and semiconductor circuit samples should be tested as soon as possible. This ensures that the system is debugged at a very early stage and provides design engineers the possibility to correct problems as soon as possible.

The test engineer's task is to fully characterize the IC at wafer level regarding its functions and parameters in all its conditions and operating speeds. A significant challenge in this process is handling the mixed signal system structure (Figure 1) of the image sensor. The pixel matrix converts the optical information to small electrical charges in each pixel. An ADC (Analogue-Digital Converter) transforms the analog information into digital data. The integrated pre-processing unit then transforms, corrects and/or compresses this data.

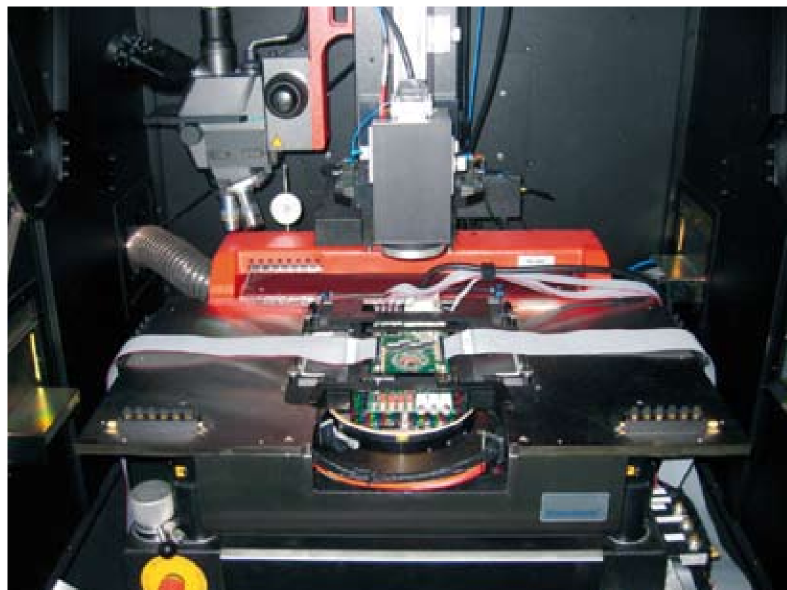


Figure 2
The integration of a SUSS MicroTec PA200 probe system and the measurement equipment from aSpect Systems.

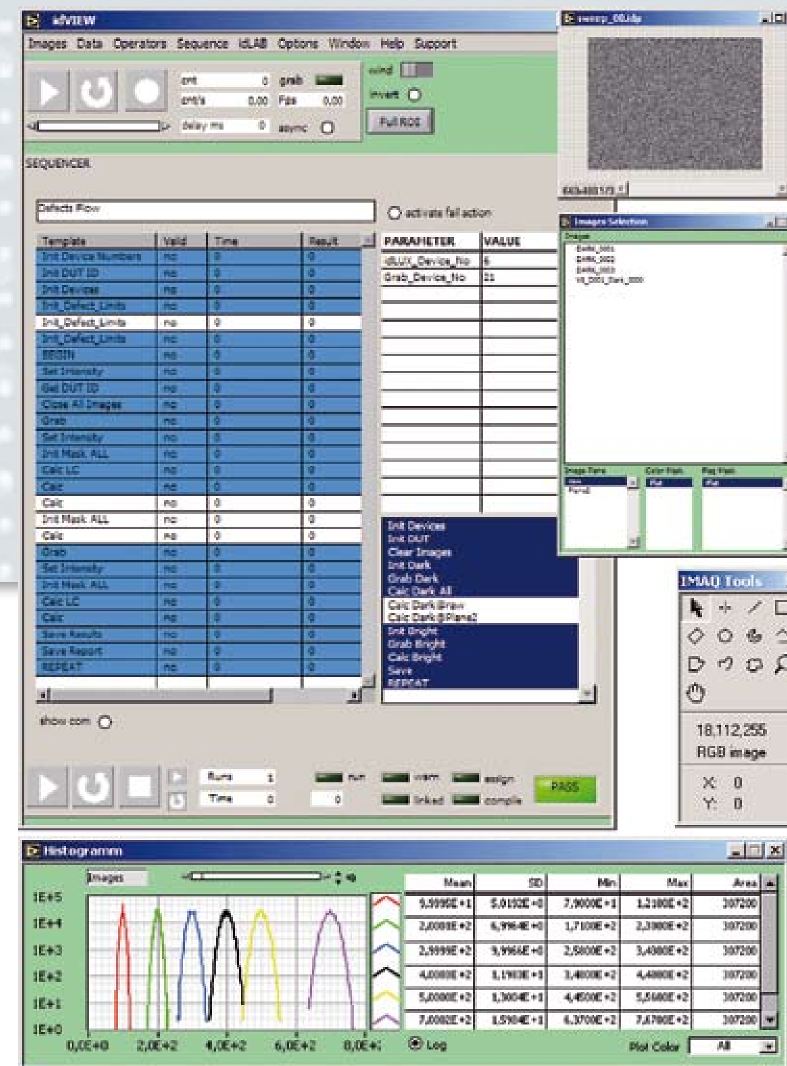


Figure 3
The measurement and analysis software works from aSpect Systems works seamlessly with the ProberBench™ Operating Environment from SUSS MicroTec.

A high-bandwidth serial interface serves as the link between the image sensor and its peripheral devices. For all these sub-components, a complete measurement solution must be developed, otherwise a separate test system would be necessary for each component.

For all these measurement tasks, SUSS MicroTec Test Systems offers an integrated test solution in cooperation with aSpect Systems (Figure 2). The system is specially designed for setting-up operation at wafer level. The key function is the innovative probe card design with add-on signal conditioning and test modules (idFlex). Short signal paths to device under test (DUT) enable full speed test under real operating conditions.

The integrated light source allows a uniform intensity and wavelength controlled illumination of the active sensor area. The probe system accomodates up to two light sources, either an integrating sphere or the LED-based illumination solution (idLux). Optionally the SUSS prober can be equipped with a thermal chuck to enable a controlled environment for testing at temperatures from -60 to 300°C.

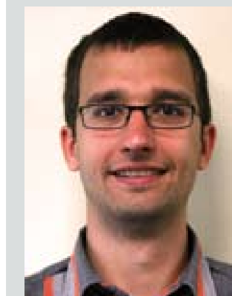
SUSS ProbeShield® Technology is the perfect solution for an EMI/RFI-shielded and light-tight environment for measuring ultra-low currents down to the fA (10^{-15} A) range. This unique measurement capability allows the system to characterize leakage currents in the analogue subcomponent and sensor core.

To execute tests and evaluate the collected data, the user can work with the integrated software environment. It provides the user a flexible interface to create test sequences to analyze the sensor in terms of defect pixel, pixel noise, cross talk and many other parameters (Figure 3).

This package gives the test engineer a tailored set of tools for characterizing CMOS image sensors. Now the engineer is able to shorten the evaluation cycles and provide valuable feedback to design and semiconductor processes much quicker than before.

With this cooperation, SUSS MicroTec and aSpect Systems are providing a complete solution, designed for special customer needs and total customer satisfaction.

➔ SUSS MicroTec and aSpect Systems provide unique, complete wafer-level test solutions for image sensor development including probe systems, temperature-controlled EMI/RFI-shielded, and light tight environments, intelligent probe card solutions, LED color illuminators and test software.



VOLKER HÄNSEL
is responsible for the segment Optoelectronic and Production Test for the Test Systems division at SUSS MicroTec. After receiving his degree in electrical engineering from the Technische Universität Dresden (Dresden Technical University) in 2001, Volker began his career at a company specializing in systems integration. There he developed measurement solutions for semiconductor test. In 2005, Volker joined SUSS MicroTec as a product engineer in the sales department. He has held his current position in marketing and product management since 2007.

The SUSS MicroTec MA/BA8 Gen3 Mask Aligner – Enabling the Wafer-Level Camera

Reinhard Voelkel, CEO, and **Martin Eisner,** CTO, SUSS MicroOptics,
Ralph Zoberbier, International Product Manager Mask Aligners, SUSS MicroTec

ABSTRACT

The Wafer-Level Camera (WLC) is a novel approach to manufacture low-cost CMOS cameras. The optical components are fabricated on glass wafers by Microlens Imprint Lithography (SMILE). Opto-Wafers and CMOS-Wafer are mounted by Wafer-Level Packaging (WLP). SUSS MicroTec has recently presented a new generation of Mask Aligners, the MA/BA8 Gen3 and an enhanced version of the highly successful MA200Compact. The third generation MA/BA8 SUSS MicroTec Mask Aligner is a big step forward in excellence and user-friendliness and a key enabling tool for the Wafer-Level Camera market. The MA/BA8 Gen3 provides ±0.25 µm alignment accuracy, optimized thick resist lithography, Nano Imprinting (UV-NIL), Microlens Imprint Lithography (SMILE), UV Bonding and Wafer-Level Packaging (WLP). The MA/BA8 Gen3 enables quick and effective development on industry-standard equipment. Processes developed on the MA/BA8 can be quickly transferred onto the SUSS MicroTec automated mask aligner platform for high volume production. The enhanced MA200Compact allows fully automated and highly accurate Wafer-Level Packaging of Microlenses to manufacture the camera module via UV-bonding.

Special focus of this SUSS MicroTec report is on Microlens Imprint Lithography (SMILE), Wafer-Level Packaging of Lens Wafers and CMOS Image Sensor related technologies.

WAFER-LEVEL CAMERA (WLC)

Today's mobile phone cameras consist of some 10 to 20 different components such as plastic or glass molded lenses, pupils, baffles, actuators, lens holders, barrel, filters and the image sensor. These components are manufactured and assembled piece-by-piece. (Fig. 1) The Wafer-Level Camera (WLC) approach is rather simple:

All components are manufactured on 8" wafer, the Opto-wafers are mounted together with the CMOS wafer, and the wafer stack is diced into some 2'000 individual camera modules. The complete mobile phone camera, including the optics, is manufactured and packaged on wafer-level using standard semiconductor technology.

Recently, major mobile phone companies promoted WLC as being the ultimate technology for next generation low-cost mobile phone cameras. Despite WLC technology is still not mature; all major camera suppliers are now investigating WLC solutions. (Figure 2)

The WLC concept has a high potential to reduce manufacturing and packaging costs and to improve quality by replacing manual working steps with fully automatic wafer processing.

The simplicity of the WLC concept often leads to the conclusion that CMOS manufacturers just have to use their highly developed semiconductor technology to manufacture the 8" Opto-Wafers. Compared to CMOS manufacturing, the WLC with some bulky lenses should be rather simple to do. In semiconductor industry, "everything is possible" and further miniaturization is only a question of time. Unfortunately, these assumptions are not valid for Wafer-Level Optics:

- Standard semiconductor technology is not suitable for the manufacturing of bi-convex aspherical lenses with up to 200µm lens sag on 8" wafer level.
- Well-established materials from semiconductor industry cannot be used for wafer optics.
- Most polymer materials suitable for optics do not survive reflow processes at 260°C.
- In the WLC approach, the CMOS sensor is covered by the glass Opto-Wafers. Electric contact pads have to be placed on the backside of the CMOS chip and Through Silicon Via (TSV) technology or Backside Illumination (BSI) of the CMOS is required.
- Fundamental physical laws limit a scaling down to ultra small cameras with high resolution.

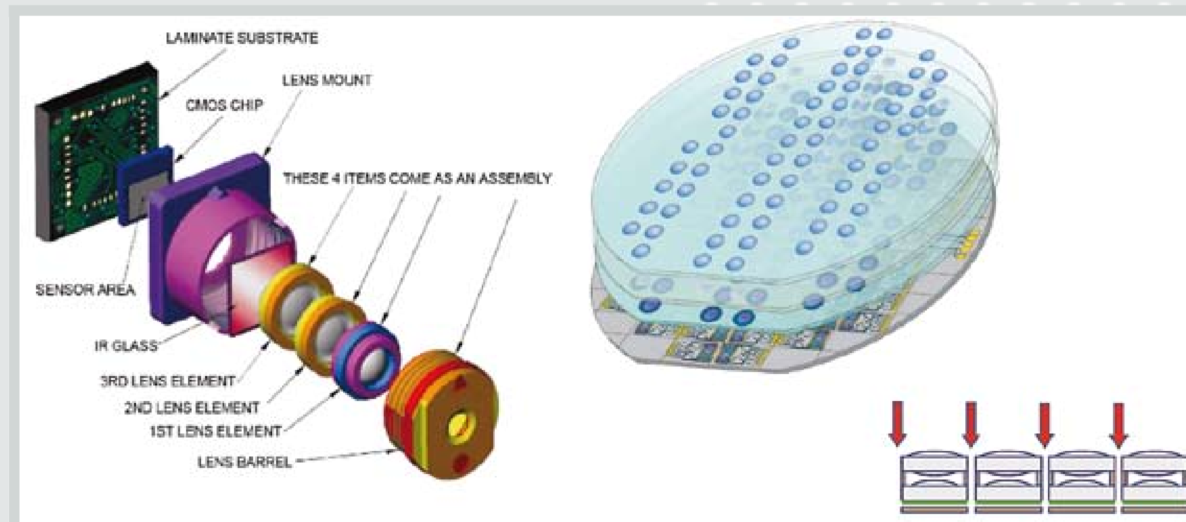


Figure 1 (Left) Conventional mobile phone camera fabrication and (right) Wafer-Level Camera (WLC). Opto-Wafers and CMOS wafer are mounted together and diced into individual camera modules. (Graphs (left): Visera, (right) Fraunhofer IOF)

Figure 3 SUSS MicroTec Mask Aligner MA/BA8 Gen3 dedicated for Wafer-Level Camera (WLC) development and production.

Novel technology has to be developed and existing production tools have to be modified for WLC. The WLC approach requires a close co-operation of optics and semiconductor industry with equipment suppliers. SUSS MicroTec, as one of the world's leading equipment suppliers, has optimized its manufacturing equipment for Wafer-Level Optics since more than a decade. The new MA/BA8 Gen3 provides all key enabling technologies in one machine and gives you a head start in this very promising market. SUSS also offers a highly sophisticated MA200Compact for fully automated wafer level packing of Opto-Wafers.

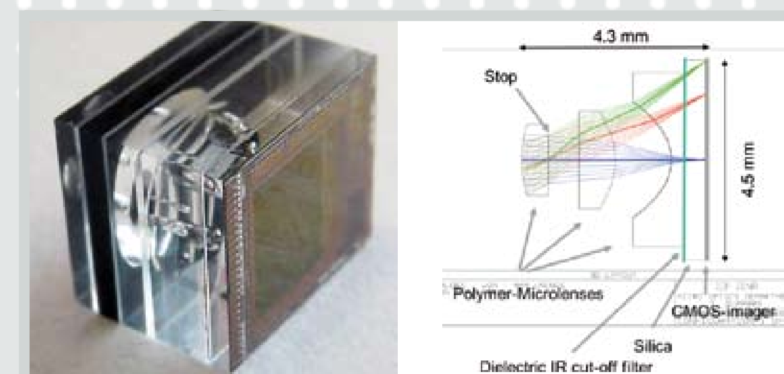


Figure 2 Wafer-Level Camera (WLC) built within European Research Project WALORI in 2005. Backside illumination (BSI) through thinned CMOS image sensor, 5.6 µm pixel VGA. [Partners: Fraunhofer IOF, CEA LETI, ATMEL, IMT Neuchatel, Fresnel Optics and SUSS MicroOptics]

MICROLENS IMPRINT LITHOGRAPHY (SMILE)

SUSS Microlens Imprint Lithography (SMILE), where lenses are imprinted by using a transparent stamp or mold and UV-light for curing, is the most promising technology of low-cost manufacturing of lens wafers for WLC. (Figure 3)

Microlens Imprint Lithography allows the manufacturing of lens arrays with a sub-micron lateral accuracy on wafer level. The MA/BA8 Gen3 combines all three technologies required for WLC:

- Microlens Imprint Lithography
- Stamp manufacturing
- Wafer Level Packaging of 8" Opto-Wafers

Accurate wedge error compensation and gap setting are crucial for microlens imprint lithography. The SUSS MicroTec MA/BA8 provides an active wedge error system that employs piezo-electric linear actuators, a highly accurate gap measurement system and a force detector. The precise double-sided microlens imprinting is realized with an exact lateral and axial alignment of the stamp, both with sub-micron precision.

Requirements for high volume wafer level packaging of Opto-Wafers are

Figure 4 (Left and top left)
Stack of five 8'' lens wafers mounting in SUSS MicroTec MA/BA8 Maskaligner with ± 1µm precision in x, y and z.

At SUSS Competence Center for Microlens Imprint Lithography, Wafer-Level Packaging of Opto-Wafers, Lens Master Wafers, Stamps and lens testing at IMT/EPFL Neuchâtel, Switzerland.

addressed by a modified and improved version of the latest production aligner platform from SUSS MicroTec. The MA200Compact has been enhanced with additional edge handling capability to safely transport and process wafers with imprinted sensitive microlenses. The system also provides latest state of the art alignment techniques to achieve excellent alignment and post bond results. As high exposure doses are required to cure UV epoxy, the SUSS MA200Compact provides intensities up to 300mW/cm². All this ensures highest yield, best possible throughput and lowest cost of ownership for WLC production.

SUSS has recently established a Competence Center for WLC at IMT/EPFL Neuchâtel which is available for SUSS customer demos and training, for prototyping, technology improvement and also provides stamps and lens wafers for research and development. (Figure 4) Fill-factor enhancement is usually applied by thin photoresist lenses directly at the CMOS fab. Lens arrays are manufactured by resist spinning, photolithography and lens melting. Typical lens sag is on the order of 2-3 µm. SUSS MicroOptics and CSEM Basel provide flexible fill-factor enhancement arrays for small series of image sensors as used for metrology or high-quality imaging applications.

MASTER LENS ARRAYS

For full 8"wafer Microlens Imprint Lithography the master tool generation is a critical key technology. Usually, smaller master arrays are used to build a larger lens master in a step-and-repeat procedure using, e.g., a NPS 300 Nano-Imprint-Stepper. Recently Kaleido Technology presented a first 8" diamond milled lens master in brass, providing spherical, aspherical and free-form lenses with better than 2 µm lateral position accuracy. For master lens arrays with a sag height below 100 µm, high-quality microlens wafers manufactured by resist reflow and reactive ion etching (RIE) are provided by SUSS MicroOptics (Neuchâtel, Switzerland).

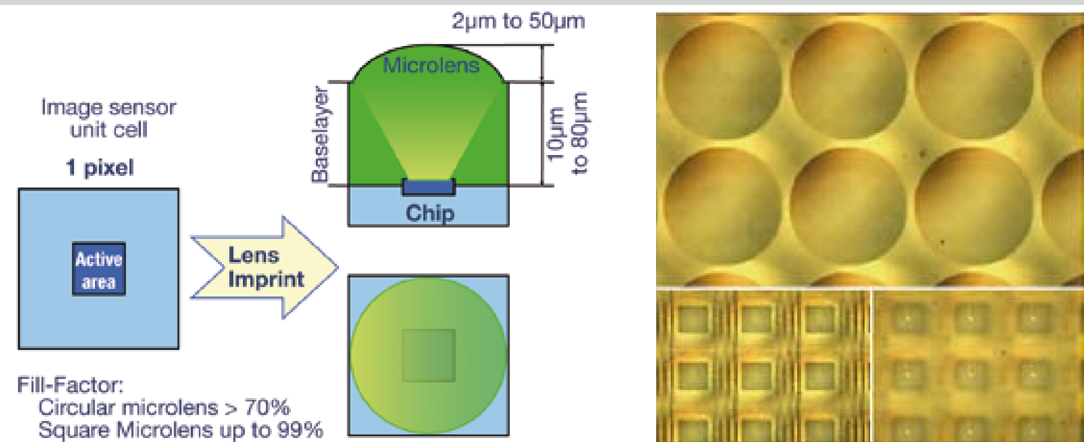


Figure 5
Fill-factor enhancement for CMOS and CCD image sensor chip. SUSS Microlens Imprint Lithography allows flexible lens and base layer variation on both wafer- and chip-scale.

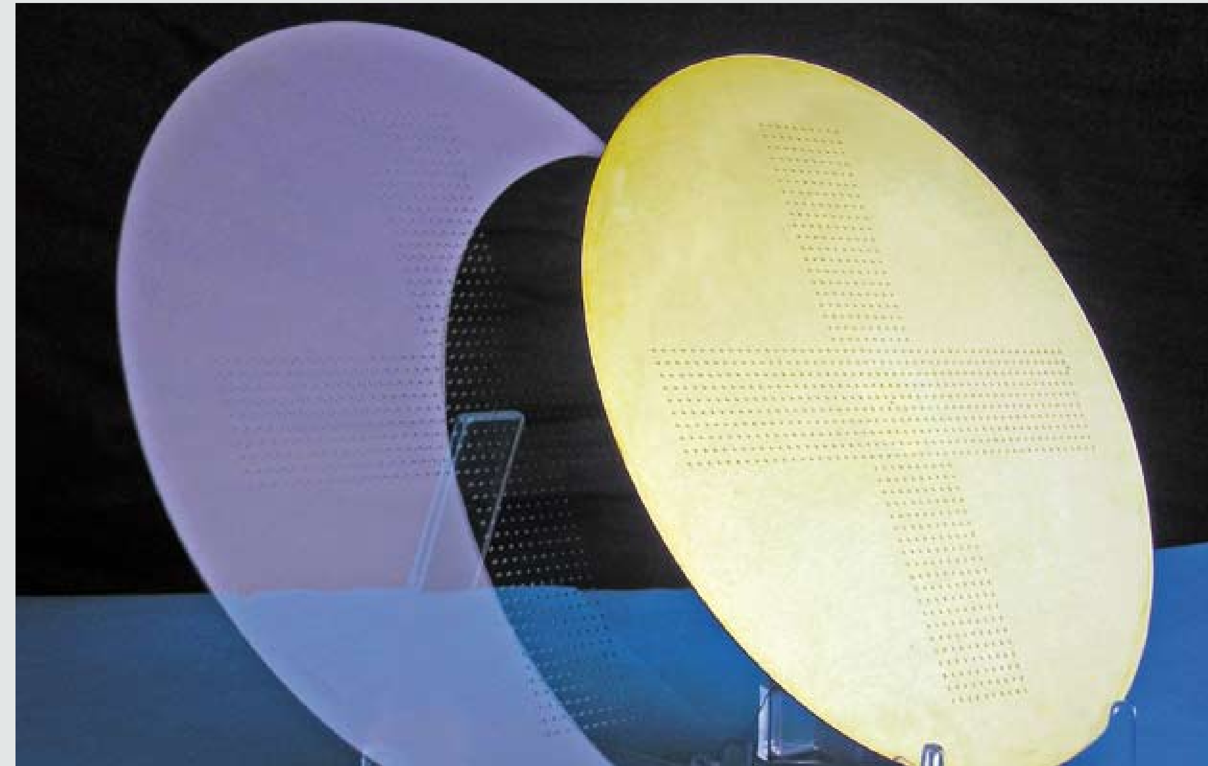


Figure 6
Master lens array (8'', brass, by SUSS partner Kaleido Technology) and 8'' lens wafer manufactured by SUSS Microlens Imprint Lithography (SMILE) in MA/BA8 Gen3 mask aligner.

Master lens arrays consisting of aspherical microlenses with profile deviation below 50 nm (rms) and surface roughness below 2 nm (rms) were demonstrated on full 8" wafer scale. (Figure 6) The wafer-scale master arrays are then transferred into a soft stamp, usually made of Polydimethylsiloxane (PDMS) by casting. The PDMS layer serves as a stamp. The polymer lens material must be suitable for high throughput imprint lithography, reflow-able at 260°C and must have long-time stability in harsh environment (heat, humidity and sunlight). For the lens design, a choice of different lens materials with high refractive indices and different Abbé numbers is required. Today, the choice of commercially available materials is very limited. Some companies have developed their own material, but do not share information.

SUSS MICROTEC – SOLUTIONS FOR THE WAFER-LEVEL CAMERA MARKET

SUSS MicroTec is the only semiconductor and electronics equipment manufacturer who has in-house Wafer-Level-Optics expertise, prototyping and small-series manufacturing capabilities. Its core-scientists have a more than 20 years record in micro-optics design, manufacturing and testing. (Figure 7) SUSS MicroOptics has established a Competence Center for customer demos and training, and provides lens master wafers, stamps, prototype lens wafers and wafer-level packaging. Together with its research partners and external consultants SUSS provides complete solutions for the Wafer-Level Camera market.

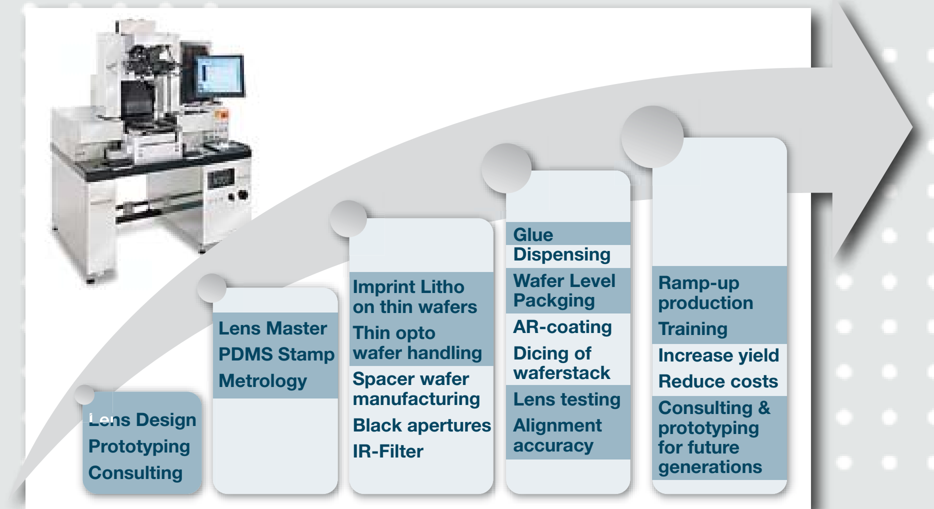


Figure 7
Ramp-up of Wafer-Level Camera development and production. SUSS MicroTec and its partners (yellow) provide solutions for the most critical steps and give you a head start to this very promising market.

ABOUT THE AUTHORS:

Reinhard Voelkel is CEO of SUSS MicroOptics SA, Neuchâtel, Switzerland

Martin Eisner is CTO of SUSS MicroOptics SA, Neuchâtel, Switzerland

Ralph Zoberbier works as product manager for mask aligners at SUSS MicroTec Lithography, Garching, Germany

Strong Partners for Technology Leadership

UV-embossed micro-optics using a SUSS MicroTec Mask Aligner. Sol-gel microlenses for collimation were imprinted on top of VCSELs. (Photos: CSEM Zurich)

Award Ceremony in Erlangen, Germany:
Dr. Ralf Süss, SÜSS MicroTec, Gilbert Lecarpentier, S.E.T, Dr. Matthias Rommel and Holger Schmitt from Fraunhofer IISB, Dr. Dietrich Ernst (Chairman of work group)

Pioneers in Wafer Level Optics

In 1999 SUSS MicroTec launched an 8" wafer fab for high-quality micro-optics in Neuchâtel, Switzerland. SUSS MicroOptics, was a spin-off from the Institute of Microtechnology (IMT), University of Neuchâtel, Switzerland, and the Applied Optics Institute of the University Erlangen-Nürnberg, FRG. Design expertise, process know how and measurement technology were transferred from the well-known research institutes to industry. SUSS MicroTec was not only the investor and business angel, but – and far more important – the equipment supplier who never stopped until the all SUSS MicroTec manufacturing systems were optimized for this new challenge. Today, SUSS MicroOptics provides leading edge micro-optics to more than 100 customers worldwide, amongst them Carl Zeiss SMT AG, who nominated SUSS MicroOptics as "preferred supplier" for DUV Wafer Stepper illumination optics.

First experiments to imprint micro-optics on wafer level using a modified SUSS MicroTec Mask Aligner MA6 have been carried out at the CSEM in Zurich, Switzerland, within the Brite-Euroam Project DONDODEM from 1998 to 2001. CSEM's microlens imprint technology has been later transferred to Heptagon, also based in the Zurich area in Switzerland. Heptagon developed proprietary processes for reflowable micro-optics and is regarded as one of the pioneers in WLC technology. Recently Heptagon opened a WLC manufacturing facility in Singapore. Another pioneer in this field is the Fraunhofer IOF in Jena, Germany. Fraunhofer IOF successfully developed replication and imprint technologies for low-cost wafer-level optics and presented fully operable prototypes of ultra-flat cameras, endoscopes cameras and WLC systems.

SUSS MicroTec, SUSS MicroOptics, Fraunhofer IOF Jena, Fraunhofer IZM Berlin and others, are partners in the German BMBF-VDI Research Project COMIKA, investigating Wafer-Level Camera (WLC) solutions for next generations of CMOS image sensors.

Awarded - Innovations in UV-Nanoimprint Lithography

For almost 60 years SUSS MicroTec has been at the forefront of companies combining consistent high quality with innovation. Recently SUSS MicroTec has been awarded with the "Innovation Award Microelectronics" in 2008 for its achievements in the development of UV-Nanoimprint Lithography (UV-NIL). The award (Georg-Waeber Georg-Waeber-Innovationspreis) was presented to a team of four scientists that jointly worked on the UV-NIL project. The nominees were Dr. Michael Hornung, project manager for UV-NIL at SUSS MicroTec, Gilbert Lecarpentier from S.E.T, a SUSS MicroTec spin-off, as well as Dr. Mathias Rommel and Dr. Holger Schmitt from Fraunhofer IISB (Integrierte Systeme and Bauelemente-technologie). The award ceremony took place on October 16 2008 in Erlangen, Germany, during the annual convention of Fraunhofer IISB.

Today's transistor densities have increased to the point where half a million or more transistors could fit within the dot maybe by a pencil. Modern chips have structures, which are even smaller than the wavelength of lithographic light. Low-cost production UV-NIL solutions for nanostructures are in development today that may be the enabling technique for next generation semiconductor; MOEMS and optoelectronic technology. In particular, nano-imprint lithography and its variations have been developed as cost-effective imprint techniques that provide higher throughput than the expensive high resolution e-beam lithography to print sub-50 nm geometries. UV-NIL is based on the principle of mechanically modifying a thin polymer film with a stamp that contains nano patterns. In cooperation with Fraunhofer IISB, SUSS MicroTec and S.E.T. have developed equipment that supports novel, cost-effective micro/nano replication technologies It is capable to replicate structures in the micro and nanometer scale with structures and layer thickness varying from sub 50 nm to several 100 µm. The main process parameters are UV light and pressure. Current imprinting challenges were analyzed with the aim to find technology solutions that can replace traditional optical lithography for the production of nanoscale devices.

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In the Spotlight

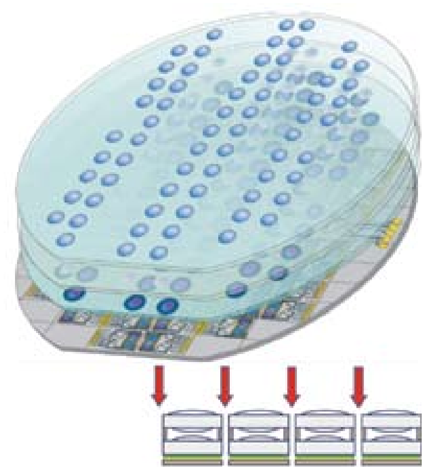
MA200Compact

THE ENABLING MASK ALIGNER PLATFORM FOR NEXT GENERATION TECHNOLOGIES: MEMS, ADVANCED PACKAGING, COMPOUND SEMICONDUCTOR, MICRO OPTICS

Ralph Zoberbier, International Product Manager Mask Aligners
Brigitte Wehrmann, Marketing Communications Manager Lithography Division, SUSS MicroTec

Mask aligners continue to be the system of choice for many existing and emerging technologies. Today the MEMS (Micro Electro Mechanical Systems), Advanced Packaging, Compound Semiconductor and Micro Optical Industry rely on mask aligner technology for production and process development alike. With the MA200Compact SUSS MicroTec has designed a new state-of-the-art mask aligner platform that has set standards in respect to alignment accuracy, high resolution, 3D patterning over topography and a new level of automation incl. SECSIIGEM interface. Since the introduction of the MA200Compact in December 2003, SUSS MicroTec has sold numerous systems to customers all over the world. Within the last months more than 45 systems have been successfully installed and are now used in high volume production and in R&D environments alike.

Figure 2



Opto-Wafers and CMOS wafer are mounted together and diced into individual camera modules.

The MA200Compact combines proven mask aligner technology with a variety of innovative features that helped to increase the mask aligner process window for a variety of new applications. Today the MA200Compact is the system of choice for thick resist MEMS applications (i.e. Inkjet Heads, accelerometers, HDD), Advanced Packaging (i.e. Electroplating Bump Process, RDL), Compound Semiconductor (i.e. HBLED) and the Micro Optics (i.e. Wafer Level Camera) world.

THE MA200Compact FORMULA FOR SUCCESS

The MA200Compact is a highly modular system that can be easily customized and is a solid production aligner platform for current and future 1x lithography applications. On the one hand the MA200Compact can be operated as stand alone mask aligner, on the other hand as cluster module directly linked with a SUSS ACS200Plus coater and developer system. Various configurations and options offer customers a wide selection to configure a system that perfectly matches their specific applications and requirements.

THE ULTIMATE MEMS TOOL

With its high accuracy, low cost of ownership and its flexibility of processing wafers of different sizes and photo resist thicknesses the MA200Compact is ideally suited to meet the technology requirements of advanced, thick resist MEMS applications

For thick resist processing the MA200Compact can be equipped with large gap exposure optics enabling near vertical sidewalls at highest aspect ratios. The highly precise DirectAlign technology combined with the SUSS ThermAlign option enables cost efficient mask aligner technology to meet even most demanding overlay criteria. In recent time more and more device layers have been transferred from expensive 1x stepper equipment back to SUSS Mask Aligners.

SUBMICRON ALIGNMENT

The SUSS patented DirectAlign technology allows an alignment accuracy below 0.5 µm (3 s) in production environments. DirectAlign actively measures and optimizes the final alignment result of mask and wafer. Advanced pattern recognition allows distinguishing mask and wafer targets synchronously in a live image and is the basis of this new technology.

SUBMICRON OVERLAY

The tight alignment accuracy combined with the SUSS ThermAlign technology offers the capability to optimize and achieve sub-micron overlay results by compensating run-out effects, which results in a new level of performance for 1x full field photolithography.

WAFER EDGE HANDING

In the production of MEMS and optical devices wafers typically require handling contact on the outer edge exclusion zone, due to most sensitive structures on both wafer sides or for substrates that cannot be processed with conventional handling. The MA200Compact can be equipped with sophisticated transport plates, robot end-effectors, prealigners and chucks that enable SUSS Mask Aligner Technology to successfully support even most critical MEMS applications, i.e. wafers with high topography on the backside, substrates for the production of ink jet heads with through holes or through channels or adhesive bonded wafers for optical lens stacking.

MASK ALIGNER TECHNOLOGY FOR ADVANCED PACKAGING AND 3D INTERCONNECT

3D integration and stacking using through-silicon-vias (TSV) is considered the next generation packaging revolution for ICs pushing front-end and back-end closer together and enabling compact, advanced electronic circuit designs. In addition to the standard topside alignment with accuracies down to 0.5 µm (DirectAlign) the MA200Compact offers bottom side and infrared alignment. Both methods offer unsurpassed precision for three-dimensional (3D) packaging lithography applications such as lithography of etch masks for TSVs and dicing streets, backside redistribution layers (RDLs) or bumping applications. While bottom-side alignment enables the MA200Compact to process double-sided structured wafers, the infrared alignment option allows the handling of opaque, yet IR-transparent materials such as adhesives, in particular for thin wafer handling or encapsulation applications.

The MA200Compact can be equipped with a post exposure bake module, that optimizes mask aligner technology for processing of advanced thick chemically amplified positive tone resists. These resists allow for steep resist profiles, especially in fine pitch wafer level packaging applications, such as gold bumping. The post exposure bake module can be directly linked to the mask aligner, offering maximum process control for chemically amplified photo resists that typically require well timed post exposure bakes. After an exposure takes place the wafer is directly transferred into a hot and cool plate stack for the tempering processes.

MASK LIBRARY FOR PHOTOMASK STORAGE

To further enhance the level of automation the MA200Comapct can be retrofitted with a mask library system. The library can store up to 20 photo masks in a controlled environment. At recipe start the system automatically detects and chooses the correct mask layer. This prevents operation failure and maximises productivity.

UV BONDING FOR WLC

Whenever it comes to a process in which high accurate alignment and UV exposure is needed, the MA200Compact mask aligner platform is the system of choice. New trends in the manufacturing of low-cost CMOS camera systems require the assembly of Opto-Wafers (optical components are fabricated on glass wafers by Microlens Imprint Lithography) on wafer level (i.e. Wafer Level Cameras).

For this specific application the MA200Compact has been enhanced with additional edge handling capability to safely transport and process wafers with imprinted Microlenses. The system accurately aligns both Opto-Wafers and bonds them via UV-bonding. As high exposure doses are required to cure UV epoxy, the SUSS MA200Compact can provide intensities up to 300 mW/cm².

ABOUT THE AUTHORS:

Ralph Zoberbier
is responsible for product development as well as international business development for the SUSS Mask Aligner portfolio.

Brigitte Wehrmann
works as Marketing Communications Manager Lithography Division.

Clif's Notes

Would You Like To Swing Curve or DOE?

INTRODUCTION

How many times have you heard the question, "What spin speed do I need to use to get a 7.5 µm thick resist film"? And the typical answer was, "Gee, I don't know, I'll have to go into the lab and run some tests".

There are many ways to determine the desired spin speed of a resist including but not limited to using :

- The SUSS coater option for 'swing curve'.
- The 'sequence stacking' option and design of experiments (DOE) to characterize the resist.

The benefits of using Swing Curves and DOE's for the characterization of polymer coatings on the SUSS automated coaters will be reviewed.

SWING CURVE

Swing curve is a term that typically refers to the sinusoidal variation of the time to clear (Eo) as a function of resist thickness. Resist manufacturers sometimes use this term to describe the change in film thickness as a function of spin speed as in Figure 1.

The data for this type of plot is obtained by setting up a coating program similar to that shown in Table 1 wherein several wafers are coated, each at a different spin speed using Step 3 of Table 1. The typical manner in which a thickness versus spin speed curve is most often obtained by the brute force method; a wafer is coated, the spin speed changed then another wafer coated and so on. (Table 1)

SUSS has an option on their automated spin coaters, ACS200 Plus and Gamma tools, called "Swing Curve". With this option one simply activates the function, sets a desired increment of speed change and then starts the coater.

For example suppose you wanted to do a spin speed curve starting from 1000 rpm up to 4000 rpm in steps of 500 rpm. Simply activate the swing curve option, input the desired speed increment, then load and start a cassette of seven wafers. The first wafer will be spun on Step 3 above at 1000 rpm, then the second wafer at 1500 rpm, and so on. You simply measure the film thickness of each wafer and plot the results to obtain a graph as in Figure 1.

In summary, the swing curve option allows the user to coat each wafer in a cassette at a different spin speed using only one recipe.

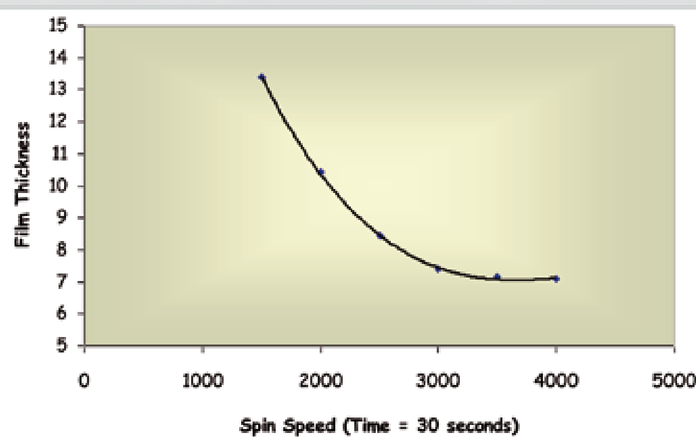


Figure 1
Classic Film Thickness Graph

Step	Function	Time (sec)	Speed (rpm)
1	Move Arm to Position	2	20
2	Dispense Resist2	6	20
3	Swing Curve Spin Speed	30	1000

Table 1
Simple Polymer Coating Recipe

	Spin Conditions		Film Thickness	
	Speed	Time	Estimate	Actual
AZ4620	900	10	24	24
AZ10XT	1950	35	10	11
AZ10XT	900	10	25	26
AZ12XT	1500	50	11	12
AZ12XT	900	10	23	25
AZ40XT	1180	30	42	42

Table 3
Comparison of Estimated versus Actual Thickness
For each resist material shown the film thickness for a certain speed and time were predicted and compared to actual results from spin tests.

SEQUENCE STACKING

In the simplest definition 'sequence stacking' allows the user to process each wafer in a cassette with a different set of conditions. In the case of the swing curve tests a user could define seven sequences and recipes where the spin speed of Step 3 in each recipe would be changed to the desired setting.

The procedure used for this method is to first scan a cassette of wafers, load the first sequence, then de-select all wafers but the first one. Select the next wafer not yet processed and assign the next sequence to be used and then start that sequence. Repeat this procedure for each sequence and wafer to be coated then start the tool.

Trial	Speed	Time
1	1122	131
2	2678	131
3	1122	520
4	2678	520
5	800	325
6	3000	325
7	1900	50
8	1900	600
9	1900	325
10	1900	325
11	1900	325
12	1900	325
13	1900	325

Table 2
Statistically Designed Experiment

DESIGN OF EXPERIMENTS (DOE)

Although swing curve and sequence stacking are fine methods of obtaining thickness data there will always be a problem with these methods. One is that the results are valid for only one spin time that was used in the test. To obtain the film thickness for a different spin time yet another group of wafers would need to be coated. If you use six wafers for each test you now have data for each of those spin times but only at the expense of processing twelve wafers. Using only thirteen wafers the statistically designed experiment shown in Table 2 will provide all the information you would ever need for this resist.

The method of 'sequence stacking' allows the engineer to define and load each trial as a separate sequence, start the process and walk away from the tool. Upon returning to the tool each trial shown in Table 2 will be completed and a summary report written to confirm that the sequence was run. After a quick statistical analysis of the measurements a set of response equations is defined and which now may be used to estimate the level of any of the responses that were measured.

For example, given several resist materials as shown in Table 3, you could reliably predict the thickness for any film thickness within a few microns!

So now when someone asks you what conditions are needed to obtain such and such a film thickness you can respond with "and would you like the edge bead height and width with that?" in just few minutes.

SUMMARY

SUSS automated coater options such as 'swing curve' and 'sequence stacking' are very useful tools in search for optimum coating conditions. These options combined with the even more powerful capabilities of statistically designed experiments (DOE) will always enhance and improve the capabilities of SUSS coaters.

CLIFF HAMEL
is the principle applications engineer at SUSS MicroTec, Inc. for lithography processes involving full field mask aligners and automated cluster coating equipment. Over the last ten years at SUSS he has co-authored several papers in the field of thick resist processes and process optimization. He has over 26 years of BEOL process and mask fabrication experience at IBM where he was the principle engineer and inventor for lift off process development. He received his BS in chemical engineering at Trinity College of Vermont.

Enabling Next-Generation MEMS Devices with Metal Eutectic Bonding

Kathy Cook and Keith Cooper, Business Development Manager, SUSS MicroTec

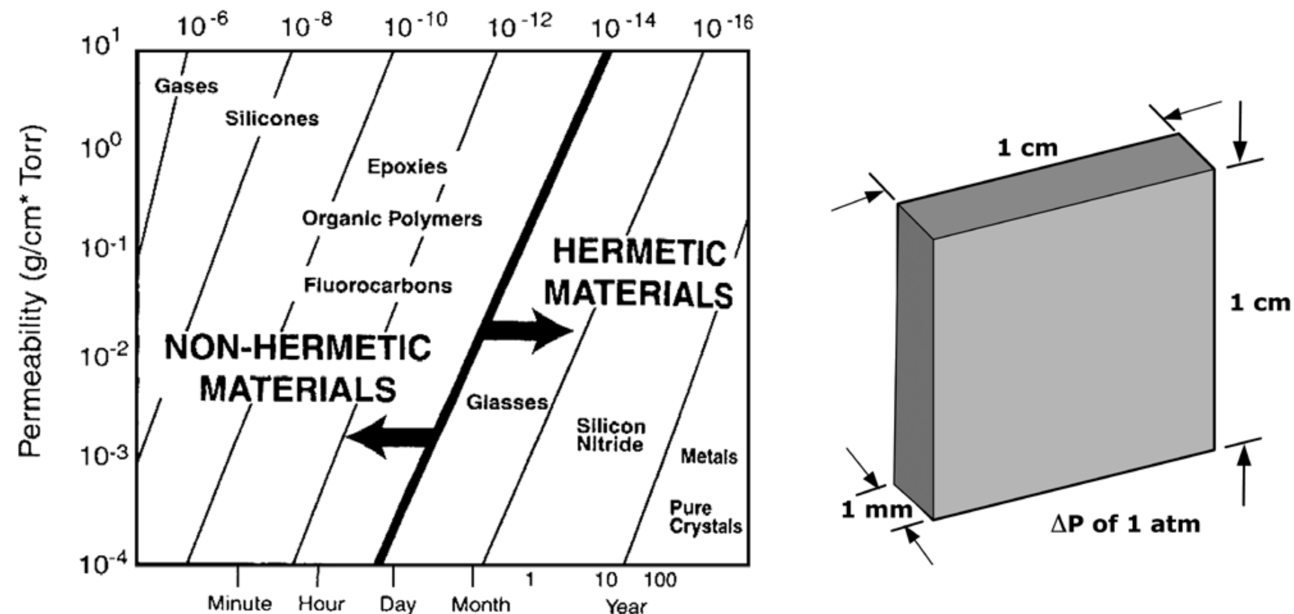
Micro-Electrical-Mechanical Systems (MEMS) devices have experienced impressive and steady growth as they are integrated into people's everyday lives. Since their conceptualization in the 1970's, they have progressed from laboratory curiosity to integration in high-end systems, and to widespread application in popular consumer devices.

A number of factors have fueled this growth in demand for MEMS devices, ranging from gains in performance and functionality, to new processes to lower the manufacturing cost for the devices, to fundamental changes in the technology and materials used in the device manufacturing.

As the demand and product offering grows, a segmentation process often takes place whereby products are separated into categories marked by price and performance. This process may be quite intentional on the part of the suppliers, where they seek to create and conquer segments where they can thrive, or it may be simply a natural flow of the market as evolutionary forces shape the direction and desires of the end consumers.

Since MEMS contain by definition some sort of mechanical function, they present special challenges to fabrication and packaging technologies. But while fabrication technologies have largely kept pace with market demand, the enormous difficulties in packaging such devices have weighed down its progress, resulting in an inappropriate proportion of costs – for some devices up to 80% - being relegated to the packaging area. Wafer level bonding for MEMS for first level packaging combined with through silicon vias is widely regarded to be the next enabling technology for the semiconductor industry. The first step is the adoption of metal bonding methods compatible with first level packaging and front and back end fabrication.

Figure 1
Permeability of Materials



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As any MEMS device progresses from lab to fab, there must be a coordinated effort between the scientists, device engineers, process and assembly technologists, and the business group to carefully mark a path to pursue. Market requirements, device performance, material and process capabilities all play an important part in deciding what the final MEMS architecture will be. If the goal is widespread use of a commodity part, the product's life cycle will likely be marked by evolutionary steps to revise the materials and production methods to ultimately lower the production costs to compensate for shrinking profit margins. If, however, the goal is to capture a higher-performance segment of the market with higher profit margins, the product's life cycle will contain incremental gains in performance that have been enabled by progress in the technology, materials and methodology to build the device. In either approach, the equipment must be capable of delivering consistent results over the entire progress of the device.

In the MEMS world, several substrate bonding techniques have been successfully applied in production. Each method has its advantages and disadvantages, owing to the material and processing costs, tolerance of manufacturing process variations process, and final device performance. The first two techniques to find wide acceptance were anodic bonding and glass frit bonding. The first used an electric potential between a pyrex and a silicon substrate to enable an electric field assisted diffusion bond and requires no intermediate layer, while the second requires the deposition of a frit material onto one substrate prior to alignment and bonding.

Though either technique could be used for a relatively low-cost bond, glass frit proved to be more tolerant of surface variations, since the screen-printed frit material would fill in any voids or gaps between the two substrates being bonded and reflow during the thermal steps self-planarized the interface.

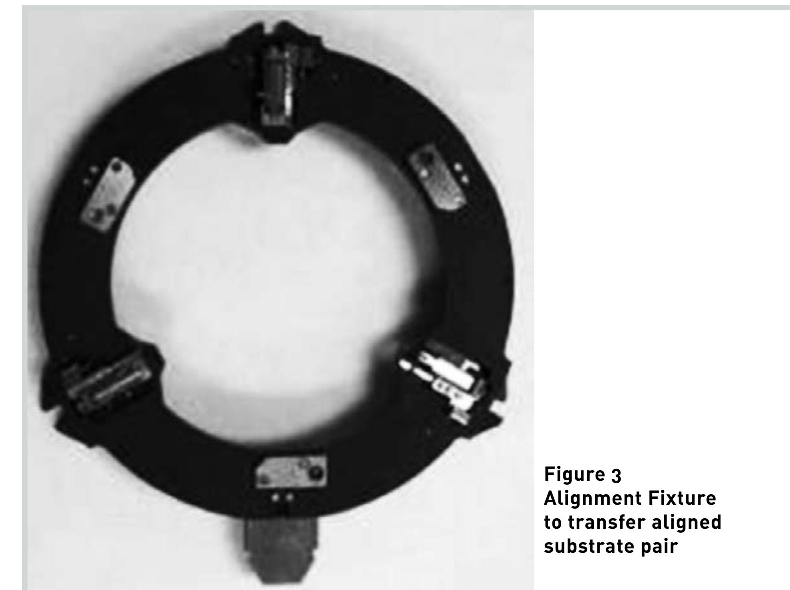

Figure 3
Alignment Fixture to transfer aligned substrate pair

Unfortunately as the frit material was densified during the bond process, its shrinkage led to non-uniform bond line thicknesses which could cause variations in device performance. And because the deposited frit material required real estate on the wafer, its use hampered device scaling which would help to lower manufacturing costs. A wider bondline to provide better protection from the environment and higher device performance was simply incompatible with device economics. And the viscous nature of the frit material during high-temperature bonding could lead to mis-alignments and non-uniform bondline thicknesses which would limit the design of smaller dice.

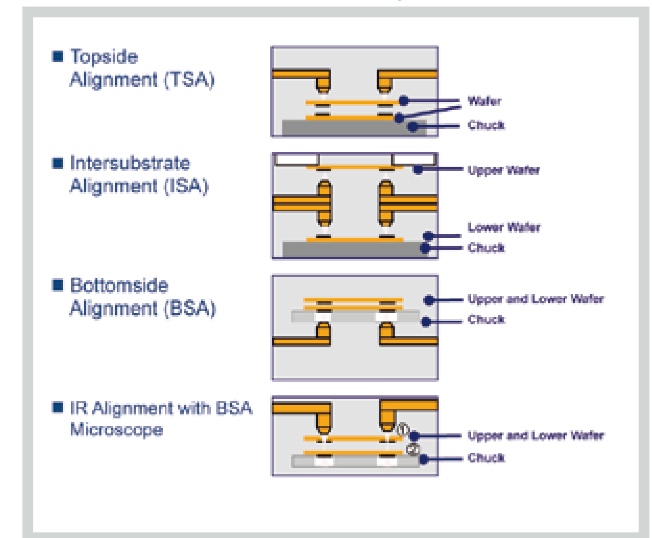

Figure 2
Various Alignment Methodologies for Substrate Bonding

Another popular bonding method is fusion bonding, also called direct bonding. Like anodic bonding, it requires no intermediate layer between the two substrates, but unlike anodic methods, it can used with a wide range of substrate material types. Because fusion bonding depends on intimate contact between bond surfaces on an atomic scale, the requirements for surface finish are rigorous. Pursued initially for unpatterned Si wafers to make Silicon-On-Insulator (SOI) substrates, fusion bonding requires a surface roughness of about 0.5nm. After the initial bonding at room temperature, the bond must be annealed at temperatures at or above 1000C, though this annealing temperature can be lowered substantially by plasma pre-treatment of the surfaces. Direct bonding has shown extremely strong bonds on Si-Si, Si-GaAs, Si-Ge and many other materials combinations, but the surface

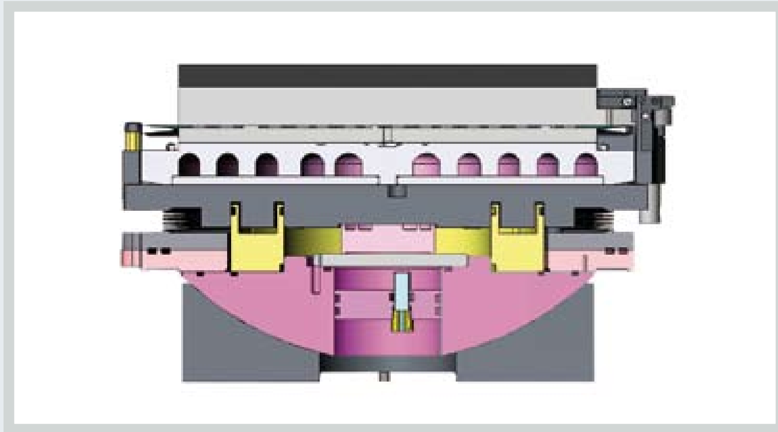

Figure 4
Self-Leveling Force Column for Bonder

requirements can be very challenging to achieve on processed surfaces. And since there is no intermediate layer to compensate between substrates, even very small particles between substrates will lead to large voids in the bond.

A more recent bonding methodology is to use metal alloys as the bonding medium. Since their deposition characteristics are well characterized as back-end bumping and assembly processes, the thickness and uniformity of the metal deposition process is well understood. Adoption of these materials in wafer level packaging lay the ground work for multilayer chip stacking and integrated packing scenarios with through silicon vias. Eutectic reactions are a triple point in the phase diagram where solid alloys mixtures transform directly to a liquid phase. This mimics the reflow processes that are so desirable in glass frit sealing. Upon cooling a very special microstructure evolves which is both strong and hermetic. Eutectic metal compositions have several benefits as sealing materials, including the ability to accurately deposit and define the metals in desired patterns, the tolerance to surface deviations, roughness and particulates, plus metals' inherent hermeticity and conductivity

Hermeticity is the degree of airtightness for a vessel or package; it's especially important for MEMS packages because the mechanical and electrical functionality of the device within the package relies on critical environmental control. Any change in the atmosphere inside the package can bring about a shift in performance or even a total failure of the device.

Many technologists have thought of hermeticity as a binary measure – a package is either hermetic or it's not. The reality is that hermeticity is a continuum, even though many have accepted an arbitrary line drawn at a permeability of about 10 - 14 gm/cm-s-Torr. Hermeticity determines the lifetime for a MEMS device, due to the interference of the permeating gas with the device's functionality. For some MEMS devices, water vapor may be the invading culprit which corrodes the moving parts, while for other MEMS devices, any gas which permeates the package will spoil the inert or vacuum environment necessary for any device function. One of the most areas most vulnerable to leakage is the bond layer which seals the MEMS device to its corresponding substrate.

In Figure 1, various materials are plotted permeability as a function of the seal surface width. Though no material is 100 % hermetic, dense materials such as metals provide much greater protection against any gas intrusion and therefore provide much greater device performance and lifetimes. Since metals are much more difficult to permeate, a thin metal bondline will provide good protection against leakage, sometimes orders of magnitude better than glass frit materials of greater thickness and width.

Metal materials for bonding layers include elements such as gold, copper or aluminum which, when joined with high temperature and high force, form a diffusion bond. To lower the process temperatures eutectic alloys such as Au-Sn or Au-In have been pursued and characterized. These alloys melt at reasonable temperatures – these two examples at 282°C and 156°C, respectively - making the bonding process easier, faster, and ultimately lower cost.

In order to fully realize the advantages of thinner metal bond lines the alignment of the two substrates prior to the bonding step must be very precise; generally the alignment must be ~10 of the metal width (75 - 80% overlap of upper and lower seals).

An enhanced bonding system offers the necessary performance to utilize all the advantages of eutectic metal bonding. In the tool scheme, the two substrates are aligned using a configurable microscope system which images the substrates' fiducial marks by visible or IR illumination Front and back side alignment of the patterns buried within the substrates, is depicted in Figure 2. Auto alignment software has been successfully employed to align various target designs and material types in a production scenario, delivering micron or sub-micron alignments.

After alignment in the bond aligner, the two substrates are held by a fixture, then transferred to a bonding chamber where the two substrates are bonded

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Die Size (mm x mm)	3	5	7	10
Effective Die Area w/ 50 µm Seals	10.1	26.8	51.5	103.5
Effective Die Area w/ 25 µm Seals	9.8	26.3	50.8	102.5
Effective Die Area w/ 10 µm Seals	9.6	26.0	50.3	101.9
Max Added Die/wfr (100 µm > 50 µm)	187	44	17	6
Max Added Die/wfr (50 µm > 25 µm)	101	23	9	3
Max Added Die/wfr (25 µm > 10 µm)	63	14	5	2

Figure 5 Changing a 100µm Glass frit seal tor a 10µm metal seal would allow for an extra 351 die for 9mm2 die.

using a combination of force, temperature and a variety of ambient conditions. Since the bonding process may include force and temperature – up to 600°C and many kN of force – this bonding fixture must precisely maintain the accurate alignment of the substrates under extreme conditions. The design of these bonding fixtures has been optimized over several tool generations, and they have demonstrated sub-micron performance in numerous bond processes. A typical alignment fixture is pictured in Figure 3.

Once inside the bonding chamber, a force column is used to bring the wafers together at a programmable force and temperature profile; each parameter can be ramped to meet specific material and process requirements. Before the force column, shown in Figure 4, begins to press the wafer stack together, it is first allowed to level itself to the stack to minimize any alignment shift caused by any deviation from the normal direction. This leveling function, coupled with a rigid design of the force column, ensures that alignment errors are not induced while compressing the bond line. This is a very a critical task considering the viscous nature of the softened metal alloy. For temperature uniformity, a sintered SiN heater coupled with SiC pressure plates provide rapid and uniform heating and cooling of the substrates, and the CTE of the pressure plates closely matches that of commonly bonded substrates. Excellent temperature and force uniformity ensure consistent bonding over the entire wafer surface.

If a metal sealing ring were to be integrated into an existing MEMS device replacing a glass frit or polymer sealing technology this one change in device layout would drastically increase the number of dice/wafer. Consider the example described in Figure 5, where a 3 x 3 mm die is currently using a 100 µm wide bondline made of glass frit or polymer. Replacing that 100 µm feature with a 10 µm wide bondline made of a eutectic metal alloy would produce a device with equal or better hermeticity, with 351 additional dice/wafer. With this new physical layout, not only would the device performance be enhanced, but the economics of producing the device would be much more favorable. This change alone could easily shift a device line's profit margins from an unattractive to a very attractive regime, without changing any of the device's active regions.

The scenario portrayed above applies directly to several MEMS devices types, particularly inertial sensors and gyroscopes. After their initial use in expensive, specialized systems such as early automotive airbag systems, they underwent a maturation and miniaturization process whereby costs were greatly reduced to expand the available market. More recently, they have been enhanced by some of the technologies described here to improve the device performance while reducing overall costs. Applications for these devices have now been expanded from airbag sensors to include vehicle stability control systems, image stabilization for cameras, and many types of low-end and high-end gaming systems.

As markets develop and mature, a natural segmentation of devices takes place, characterized by a price/performance curve. Lower performance devices will always experience price pressures and methodologies must be refined to maintain a market position without ceding market share to lower-cost suppliers. Higher functioning devices, enabled by such technological enhancements as eutectic metal bonding with best-in-class equipment, will serve the high-performance needs of the market, providing higher selling prices at sustainable margins.

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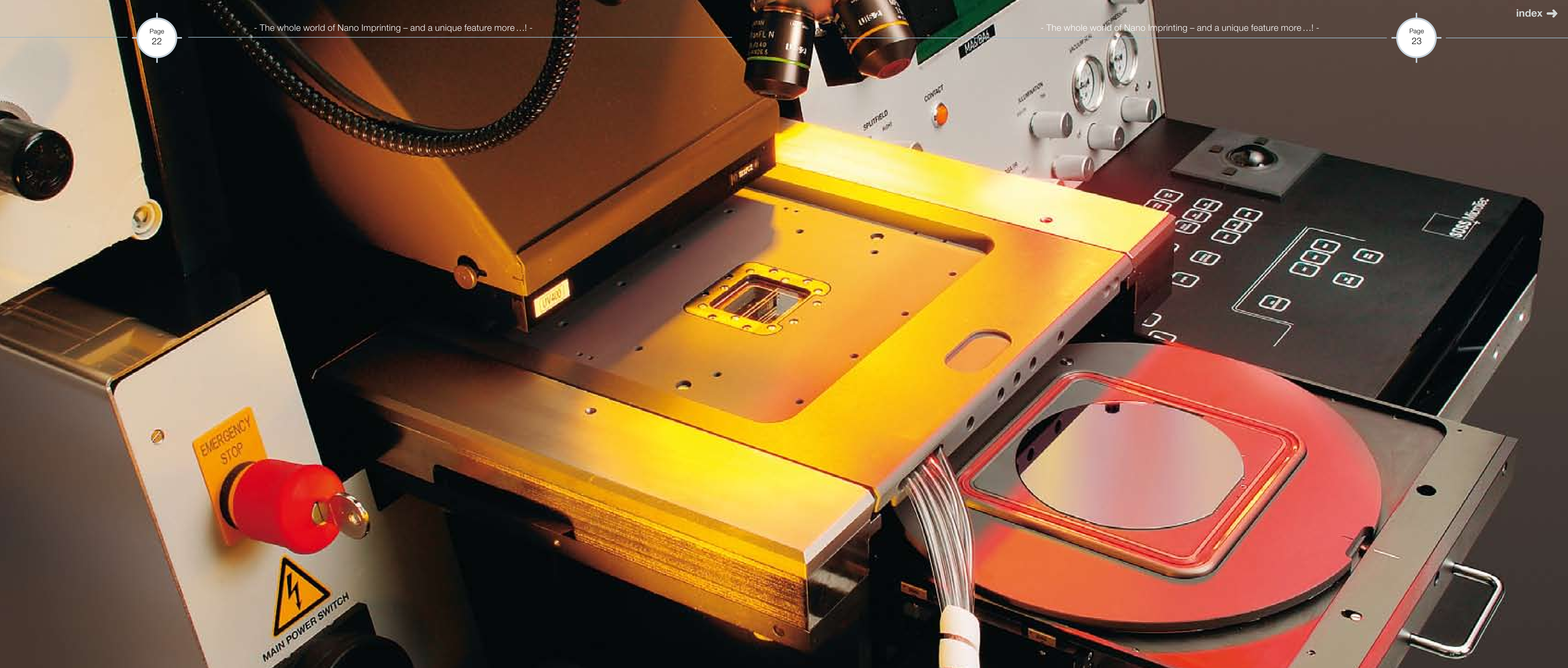


The whole world of Nanoimprinting –

and a unique feature more …!

Dr. Michael Hornung, Application Development Project Manager
Johann Weixlberger, Business Development, SUSS MicroTec

Nanoimprinting as "next generation" lithography was promoted already several years ago, focusing on mainstream semiconductor applications – and failed so far to overcome the most critical hurdles in semiconductor industry: defectivity. Contact in any sense is not a favorite processing technology step in this industry as particle transfer in any direction is a risk, reducing yield, thus profitability.

Nevertheless, looking intensively into this technology a lot of advantages have been discovered and brought towards industrialization, like low cost nano patterning for a wide range of optical structures. Enabling huge steps in more effective light guidance with photonic crystals, light coupling/decoupling for high brightness LEDs, laser diodes and solar cells as well as display backlighting applications. Even the next generation HDDs based on "bit patterned media" technology is one promising field for nanoimprinting lithography (NIL) patterning. In all this applications small defects do not destroy the device, just reduce effectiveness gains.

So NIL was optimized in terms of materials and processes, learning that the master stamp is the key component in this field. UV-NIL as room temperature process and thus most liked technology in this field offers two basic materials for such a stamp – quartz and PDMS. Both offering features but also limitations, a classical compromise is the result for various applications: while quartz as rigid material provides best

pattern fidelity and repeatability it only allows relatively small imprint areas up to 1" as co-planarity between stamp and substrate in the nm-regime is essential – and cannot be granted on larger areas like full substrate size. The alternative PDMS as soft material can overcome this limit and go for full substrate sized stamps, 8" printing is a common methodology today based on this material. The disadvantage herein is the deformation taking place during printing (applying contact force !), thus limiting the minimum feature size to a few hundred nanometer; below that pattern size repeatability and pattern fidelity is no longer granted.

This limits do not matter when it comes to µm or even mm imprint patterns like micro lenses or micro fluidics, for both applications Imprinting has proven its volume manufacturing capability. An ever increasing number of lens systems in mobile phones are relying on this material and technology.

As leading technology provider in terms of equipment Suss Microtec was further looking into improvements to overcome these limits and with Philips` based SCIL-technology the "best-of-two-worlds" method was introduced.

MA8 Gen3 Suitable for all retrofitable options like SMILE (lens printing), NIL SCIL and many other litho features

SCIL – Substrate Conformal Imprint Lithography – was invented by Philips Research, Eindhoven in the Netherlands, NL for inhouse applications and wanted to be available for the entire market; thus Suss Microtec licensed this technology and implemented it into the existing aligner platform and extended its NIL product portfolio successfully, especially for applications that could not be successfully targeted so far.

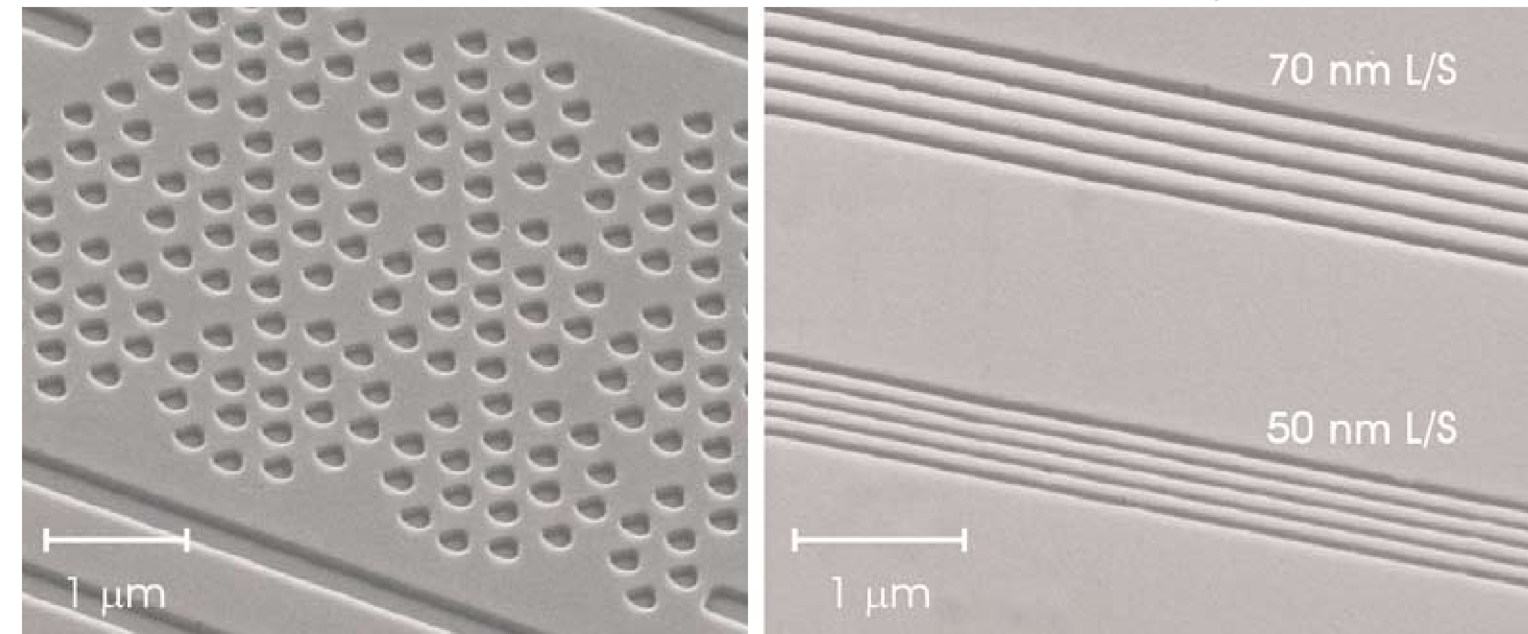
The secret behind SCIL is the combination of a soft PDMS stamp with limited thickness aro 500 µm, attached to a flexible glass backplane (200 µm thickness) – this combination provides lateral stiffness thus no stretching or compression of patterns during imprinting, still allowing large area planarisation due to bendable thin glass backplane. A forceless contact method based on capillary forces completes the optimum imprint method and exciting results open a new world of NIL-based products.

LEDs processed through several epi layers usually tend to have micro spikes on epi surfaces – these spikes usually disable imprinting as hard stamps will destroy the substrate as well as the pattern on the stamp itself.

With SCIL these spikes can penetrate into the soft PDMS, not destroying even neighbor patterns nor the stamp. Patterns in the sub-200 nm range can be applied on full substrate area up to 6" currently.

Hard disk drives on typ. 65 mm discs need to to patterned in the nm-regime as well, even smaller patterns for next generation "bit patterned media" in the 20 µm range – but only a single imprint can grant the uniform concentric dot distribution on this area. Hard stamps have proven their limits for this single imprint application, SCIL is opening the door into a new world of excellence and future TB-HDDs (Terra-Byte).

Suss Microtec with its unique NIL product portfolio serves all this new applications and technologies with equipment and process KnowHow as known in the past in terms of mask-aligners, coaters and wafer bonders – a new arena is entered, we are part of it !



Left: U dot out of 160 nm wide holes positioned in concentric rings as used for photonics crystals

Rigth: 50 and 70 nm lines/spaces pattern

Dr. Michael Hornung,
Application Development Project Manager, managed the application group of the lithography division and took over NIL technology development in 2006.

Johann Weixlberger,
Business Development Manager for NIL, joined SUSS MicroTec in 2007.

Semi-flexible SCIL-stamp

SUSS MicroTec in the News

Here's a summary of our recent press releases.
To read the entire press release, please visit
http://www.suss.com/company/news

August 26, 2008
CB Series Wafer Bonders for Advanced MEMS

"SUSS MicroTec announces the CB Series, semi and fully automated wafer bonders, for Advanced MEMS devices for the automotive and consumer markets. There are a variety of wafer level bonding methods for MEMS fabrication processes like anodic and glass frit, with the most commonly used in Advanced MEMS being eutectic, fusion, and metal diffusion bonding.

September 4, 2008
300 mm ProbeShield System Order

SUSS MicroTec Test Systems has announced that it has received an order for the PA300PS with ProbeShield® Technology, the 300 mm wafer-level probe system for device characterization and reliability test, from a major Asian semiconductor memory manufacturer. The decision follows a six-month, head-to-head comparison against the incumbent and major competition for wafer-level test solutions at the manufacturer's facilities. During this time, several benchmarking activities were undertaken. These consisted mainly of advanced tests of semiconductor devices, such as flicker noise, I-V, C-V and S-parameter measurements, which are used to extract critical parameters in the device design and process control phases. SUSS MicroTec's ProbeShield Technology consistently outperformed the competitive solutions, leading to its ultimate selection.

"The engineers at the manufacturer chose ProbeShield Technology due to the superior measurement results and significant time savings the advanced feature sets provide„
Rob Carter, Vice President of Marketing and Sales for SUSS MicroTec Test Systems

September 9, 2008
New Production Wafer Bonder for CMOS Image Sensor Market

At this year's Semicon Taiwan from September 9 to 11 in Taipei SUSS MicroTec introduces the XBC300 Production Wafer Bonder for the CMOS Image Sensor (CIS) market. Visitors will have the opportunity to learn more about the world's first wafer bonder product family specifically designed for CMOS Image Sensor production.

September 18, 2008
ISO 9001:2000 Certification

SUSS MicroTec announces that SUSS MicroTec Inc., manufacturer and supplier of production and process wafer bonding systems, now holds the globally recognized ISO 9001 certification for having established a high level process and system-oriented quality management (QM) based on ISO 9001 standards. Proceeding the ISO certification of SUSS MicroTec Lithography GmbH in 2007, another division of the SUSS MicroTec group has been certified for international quality standards. This is in line with on-going efforts to increase efficiency and alignment within the SUSS MicroTec group.

October 1, 2008
Next Generation Manual Mask Aligner for Industrial Research and Operator-Assisted Production

SUSS MicroTec launches the third generation of its MA/BA8, a manual mask and bond aligner that offers highest process flexibility including submicron alignment and exposure optics dedicated for thick resist exposure. In addition it allows easy and fast upgrades to emerging technologies such as UV-nano imprinting, microlens imprinting, UV-bonding and enhanced bond alignment. The new MA/BA8 Gen3 from SUSS MicroTec combines an unmatched resolution and light uniformity with a high-precision alignment capability down to 0.25 µm, the highest accuracy for a mask aligner available today.

October 7, 2008
Large Area Nanoimprint Lithography now Available on SUSS Mask Aligners

SUSS MicroTec announced today that the capabilities of its manual mask aligners are now enhanced with a new nanoimprint toolkit, that enables them to pattern large areas with repeatable sub-50 µm printing capability. The new technology called SCIL (Substrate Conformal Imprint Lithography) has been developed by Philips Research, Eindhoven/The Netherlands and transferred to SUSS MicroTec in a technology license agreement.

"This cooperation with Philips Research and MiPlaza demonstrates SUSS Micro Tec's continued commitment to bringing the most innovative technology to the marketplace„
Rolf Wolf, General Manager of SUSS MicroTec's Lithography Division

October 28, 2008
Seminar Series in Asia on Innovative Process Solutions for 3D Integration

SUSS MicroTec and Surface Technology Systems are hosting an advanced technology roadshow in five major cities in Asia from October 29 to November 7. The series of one-day events is building on the success of the US roadshow this spring and will provide a comprehensive overview of the latest developments in the field of 3D Integration and Advanced Packaging

November 11, 2008
Product Launch: iVista™ LC

SUSS MicroTec Test Systems today announced the iVista™ LC High-Resolution Digital Microscope. Its introduction is timed to meet the increasing need in failure-analysis labs for an advanced microscopy tool capable of delivering high-resolution digital images in conjunction with laser-cutting capabilities.

December 4, 2008
ProberBench™ Operating Environment

SUSS MicroTec Test Systems has revealed the ProberBench™ Operating Environment, a full-featured software suite for efficient, intuitive and safe wafer-level probing. In 1995, SUSS revolutionized wafer-level test by introducing the first Windows-based prober control software. Now, more than a decade later, SUSS has developed the latest software revolution for engineering wafer probe systems for the 21st century.

December 22, 2008
Strategic Alliance in Taiwan

SUSS MicroTec Test Systems has entered into a strategic alliance with MPI Corporation and Chain Logic International Corporation of Taiwan. The cooperation includes a relationship among the organizations on a worldwide basis, covering channel distribution of semiconductor test related technologies and products, bi-directional outsourcing as well as development projects that are in alignment with jointly developed and mutually beneficial roadmaps.

"SUSS MicroTec is exactly the type of high-quality organization that will help us improve business practices at home and abroad while offering customers the highest return on their investments.„
Brian Green, Chairman of the MPI Group

January 20, 2009
300 mm Coat/Develop Cluster enhanced for 3D Integration

At Semicon Korea 2009, SUSS MicroTec unveiled the second generation of its ACS300, a modular system for coating, baking and developing of wafers up to 300mm. The ACS300 Gen2 offers unmatched configuration flexibility at market-leading cost-of-ownership). The system architecture and process modules are specifically adapted to the needs of the advanced packaging and 3D integration industry, which requires very thick photo resist layers of up to 100 microns and more. Combining best in class coat and develop uniformity with exceptional edge bead performance makes the ACS300 Gen2 the preferred solution for various special spin coating applications such photosensitive polymers like polyimide, PBO or Cyclotene™ (BCB).

February 2, 2009
Frank Averdung Assumes Position of Chief Executive Officer Ahead of Schedule

Frank Averdung will assume the position of Chief Executive Officer of SUSS MicroTec AG effective starting February 1, 2009. The Company's Supervisory Board appointed Mr. Averdung to the Management Board of SUSS MicroTec AG in November 2008. Mr. Averdung was originally to take over his duties as Chief Executive Officer beginning June 1, 2009. The former Managing Director of Carl Zeiss SMS GmbH will thus take office four months earlier than planned.

"I am ... confident that with the solid foundation of our leading technological product portfolio and timely introduction of cost-reduction measures, we are well positioned to successfully master this challenge"
Frank Averdung, CEO, SÜSS MicroTec AG

February 10, 2009
MST.factory Purchases SUSS MicroTec CB8 for MEMS Process Development and Prototyping in Europe

MST.factory dortmund, a renowned center of competence for micro and nanotechnology based in Germany, has purchased the CB8 High Performance Wafer Bonder from SUSS MicroTec, a leading supplier of innovative process and testing solutions. This purchase continues last year's success when SUSS MicroTec has won more than 80% of the MEMS production wafer bonder orders to become the dominant Advanced MEMS market shareholder in wafer bonding.

February 17, 2009
SUSS MicroTec and iX-factory Join Forces for the Development of Microfluidics and Integrated Optical MEMS Solutions

SUSS MicroTec and iX-factory, a leading expert for single wafer production and technical services, announced today that they are closely cooperating on microfludics and integrated optical applications. iX-factory develops its technologies on equipment platforms that include the newly launched MA/BA8 Gen3 mask and bond aligner and the CB8 wafer bonder from SUSS MicroTec.

Where to Meet SUSS MicroTec in the Next Months

February

- **nanotech 2009** · Tokyo, Japan · Feb 18 - 20

March

- **IMAPS Device Packaging** · Scottsdate, AZ, USA · Mar 10 - 11
- **Smart Systems Integration** · Brussels, Belgium · Mar 10 - 11
- **Semicon China** · Shanghai, China · Mar 17 - 19
- **MIG METRIC** · Pittsburgh, PA, USA · Mar 25 - 26

April

- **ICMTS** · Oxnar, CA, USA · Mar 30 - Apr 2
- **IRPS** · Montreal, Canada · Apr 28 - 30

May

- **EPMT** · Lausanne, Switzerland May 12 - 15
- **MEMS Forum** · Japan, May 17 - 19
- **Semicon Singapore** · Singapore · May 20 - 22
- **Sensor & Test** · Nürnberg, Germany · May 26 - 28

June

- **IITC** · Burlingame, CA, USA · Jun 01
- **ARFTG** · Boston, MA, USA · Jun 01
- **Semicon Russia** · Moscow, Russia · Jun 02 - 04
- **PSECE 2009 Philippines** · Manila, Philippines · Jun 03 - 05
- **SUSS Southwest Test Workshop** · San Diego, CA, USA · Jun 07 - 10
- **EMPC** · Rimini, Italy, Jun 15 - 18
- **MTTS** · Boston, MA, USA · Jun 15 - 19
- **Int'l Image Sensor Workshop** · Bergen, Norway · Jun 25 - 29

Please check our website for any updates: www.suss.com/events

We hope you found this edition of the SUSS Report interesting and informative.
For more information about SUSS and our products, please visit

www.suss.com

or write to **info@suss.com** with your comments and suggestions.

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SÜSS MicroTec

Our Solutions Set Standards