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SUSS report

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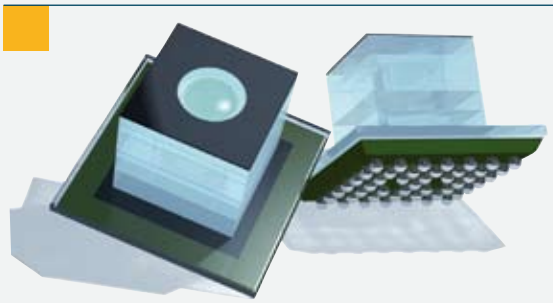
60+

Years of Engineering Spirit

SUSS MicroTec is looking back on sixty years of production of high-quality equipment

SÜSS MicroTec

index



Full View

Frank Averdung
CEO and President of SUSS MicroTec

SUSS MicroTec – Sixty Years of Engineering

SUSS MicroTec is looking back on sixty years. A lot of things have happened in our industry during those early days. Bell Labs invented the transistor, Moore published his now famous law and TI patented the first micro processor. While perusing through the archives on the occasion of our anniversary one can still sense the pioneering spirit that Karl Suss, the founder of SUSS MicroTec, embodied. The industry was still young then. Nobody could foresee how it was going to develop. It quickly became clear: the ones who had joined the club had all the advantages. Those who rejected the new ideas or simply were too slow, would soon find themselves in front of locked doors. Innovation has a short admission period. But even if you took part, that did not guarantee sustainable success. Many of the pioneering semiconductor companies can now only be found in historical reviews.

The break of dawn of a new technology is always exciting and every little success encourages it to go on. The major driving force behind it is competition. The research community gets together to share results only to – after long discussion and thorough evaluation – get back to its laboratories to keep on searching individually. Being part of that small community provides access to innovative know-how. For an industry partner it is important to pick up topics in research and development and actively drive them forward. As in the past companies that choose their research alliances wisely will be ahead of their competitors.

One of today's topics that is considered to be an entrance ticket to the future is 3D integration. Whoever has not started attending to it should start latest by now. The course for a technology introduction has already been set. It is no longer a question of whether or not 3D integration will happen, what is being debated now is when volume production will begin. Experts have long known that 3D integration technology has the potential to allow the semiconductor industry a future far beyond Moore's Law.

There are also new universes to discover in the field of shrink technology. Looking for smaller and smaller structures, suppliers are moving further into the nano world. As soon as the new chip generations work with 22nm structures and smaller, the optical immersion lithography will reach its limits. EUV lithography nano imprinting is seen as a promising alternative – a topic that SUSS MicroTec has approached together with research partner Phillips.

Lucky are those enterprises that not only have enough financial capital for these kinds of undertakings, but also have the right human resources that contribute their creativity and personal experience to new technologies. This really makes the difference. After all, the development of products feeds on the innovative force of individuals. I would therefore like to thank the employees of SUSS MicroTec for their exceptional work over the past sixty years. Without them we would not be one of the worldwide leading equipment suppliers for the semiconductor industry: yesterday, today, and in the future.

Frank Averdung

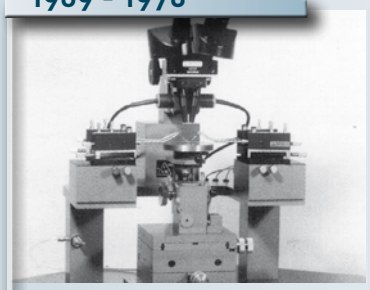
1949 - 1958

When Karl SÜSS founds a sales organization for the optical devices of Leitz Wetzlar (later Leica) in 1949 in a garage in Munich, the German post-war infrastructure still shows the signs of unsteady ruins. It takes the entrepreneur vision, commitment and a lot of courage to set up a business.
Karl SÜSS, however, makes the company an expert in optics. The company soon offers service and maintenance for the optical devices thus gaining reputation within the re-appearing research institutes and industry partners in Southern Germany.

1959 - 1968

Munich-based Siemens approaches SÜSS in 1962 with a manufacturing order for thermo-compression bonding machines for transistors, marking a changing point in the history. The company moves from sales and maintenance to contract manufacturing. The first order is comprised of small measuring tables with stereo microscopes that are temporary staff bonded together. One year later a second order follows. In 1963 SÜSS develops for Siemens a prototype for the first mask aligner, the legendary MJB3. Karl SÜSS and his two sons Ekkehard and Winfried successfully manage the flourishing business which expands so much that the company soon has to move its premises to Garching outside of Munich, which is to this day the headquarters of SUSS MicroTec.

1969 - 1978



As the semiconductor industry grows, various other business opportunities appear. Being an acknowledged expert in photolithography SÜSS now starts looking into the world of test systems. The first prober is released in 1970 providing random testing, measurement and optical tests. SÜSS also engages in manufacturing automatic diamond scribers that are used to divide wafers into individual chips. The first double-sided mask aligner is invented in 1974 allowing for dual-side exposure and confirming the success of SÜSS mask aligners. With a loyal customer base mainly in the field of research and development, SÜSS explores its opportunities in the manufacturing environment. In 1975 the MJB55 is developed, making it the first mask aligner for full production and enables SÜSS to reach out to production customers.

1979 - 1988

This decade is marked for SUSS by worldwide expansion as the semiconductor industry is reaching out to emerging markets in Asia. SÜSS starts its oversea business with a US site in Waterbury, Vermont. The first Asian subsidiary is founded in Thailand in 1983, with more sales offices in Japan, China and Taiwan to follow. With a side step into the very specialized field of xray stepper lithography, SÜSS further concentrates on lithography related processes and gets ready for the production of substrate bonders.

1949
Karl Süss founds the Karl Süss KG in Munich, Germany.

1963
SÜSS develops first mask aligner for the production of transistors.

1970
SÜSS develops its first probe system.

1971
SÜSS opens its first European subsidiary in France. At the same time SÜSS starts with the production of diamond scribers which continues for more than 20 years.

1974
SÜSS releases its first mask aligner for full production processes.

1980
SÜSS starts its overseas business with a new production site in Waterbury, USA.

1983
SÜSS expands into the Asian markets first in Bangkok, Thailand.

1984
SÜSS opens a subsidiary in Wokingham, Great Britain.

1988
SÜSS opens a subsidiary in Kanagawa, Japan.

Historical Review

1989 - 1998

SÜSS meets the growing demand for microsystems by starting to manufacture substrate bonders in 1989. Substrate bonders are used in microsystem technology to join heterogenous materials with patterned surfaces. SUSS adds spin-coaters to its product portfolio by taking over S.E.T in 1993, thus complementing the existing photolithographic product lines.
The development of moduled clusters that combine several wafer processing functions into one unit marks another step in the development of SÜSS that is necessary to meet the requirements of production environments without manual intervention.
Karl Suss passes away in 1994. Soon thereafter, his eldest son Ekkehard Suss unexpectedly dies at an early age setting off a reorganization of the SUSS group.

1999 - 2008

The beginning of this decade is marked by SÜSS MicroTec AG going public. The SÜSS family sells the company that is represented by Dr Winfried Süss on the board.

With the acquisition of Fairchild Technologies and Image Technologies, SÜSS gains access to high-end application markets which further complements the product portfolio of spin coaters and photomasks. Also, SUSS MicroOptics is founded as a supplier of micro optical devices.

SÜSS is renamed SÜSS MicroTec in 2001 and now concentrates on the technology development in the packaging field, offering dedicated solutions for the 3D packaging, MEMS and LED markets.

2009

SUSS MicroTec tackles the challenge of 3D integration. As one of the world's first equipment suppliers the company offers solutions for manufacturing wafer-level cameras. Moreover, it methodically approaches the challenging thin wafer handling process that is one of the barriers for the commercialization of 3D integration technology. SUSS MicroTec is now able to supply its customers with a wide range of functional technologies for temporary bonding and de-bonding processes. Its latest alliances with research institutes worldwide show that SUSS MicroTec stands at the forefront of innovations.

Today SUSS MicroTec has more than 620 employees in six production and eight sales sites.

1989
SÜSS develops the first substrate bonder.

1997
SÜSS launches world's first 300 mm probing system.

1998
SÜSS develops first fully automatic bond and coater cluster for full production in one process module.

1999
SÜSS opens a production site for coaters in Vaihingen, Germany and starts the production of high-end coater clusters. At the same time the SÜSS MicroTec AG goes public.

2001
SUSS MicroTec acquires Image Technologies in Palo Alto, US. The Karl SUSS group is renamed SUSS MicroTec. Subsidiaries in Shanghai, China and Hsin-Chu, Taiwan open.

2002
SUSS MicroOptics in Neuchatel, Switzerland, is founded. Mask aligner and coater go into for 300mm wafer production.

2004
SUSS MicroTec develops its first mask aligner for sub-micron processes.

2005
SUSS MicroTec's first spray coater targeted for the 3D integration and MEMS markets is released.

2006
SUSS' remanufacturing business is launched in Oberschleissheim near Munich offering quality guarantee on used SUSS equipment. At the same time the bond cluster module for SOI (silicon-on-insulator) hits the market.

2007
SÜSS MicroTec sells its device bonder business unit while the Test Systems division comes out with its ProbeShield technology.

2008
SUSS MicroTec releases various equipment for 3D packaging, e.g. a next-generation mask aligner and a wafer bonder dedicated for CMOS image sensor applications. The subsidiary in Korea opens.

Strong Partners for Technology Leadership

3M process enables fast, reliable temporary bonding of ultra-thin wafers

Blake Dronen, Technical Manager, 3M Electronic Markets and Materials Division

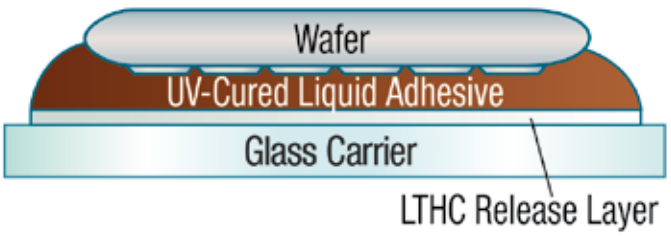
The 3M™ Wafer Support System, a key element of the new SUSS 300mm bonder line, is a temporary bonding process based on high-performance 3M adhesive and release layer technologies. Designed to enable high-volume manufacturing of ultra-thin semiconductor wafers, the 3M system eliminates the use of solvents or additional cleaning steps; offering higher system throughput and reducing chemical waste.

The heart of the system is 3M™ Liquid UV-Curable Adhesive – a family of 100% solids acrylic adhesives designed for temporary bonding of semiconductor wafers to a glass carrier. This provides a rigid, uniform support surface that minimizes stress on the wafer during subsequent processing steps, resulting in less warpage, cracking, edge chipping and higher yields.

PROCESS FLOW

1. Mount

3M™ Liquid UV-Curable Adhesive is spin-coated on to the wafer. The wafer is then vacuum-bonded to the glass carrier, which has been treated with a release layer of 3M™ Light-to-Heat Conversion Coating (LTHC). During spin coating on the wafer, the adhesive flows into the topography of the wafer front side, providing rigid support– even on large bump wafers. The system is designed to accommodate a single dispense and spin cycle on wafers with large 100µm+ topography. Multiple spin and dry cycles are not needed. As a liquid, it also provides more control over the Total Thickness Variation (TTV). The adhesive is then quickly cured with UV light.

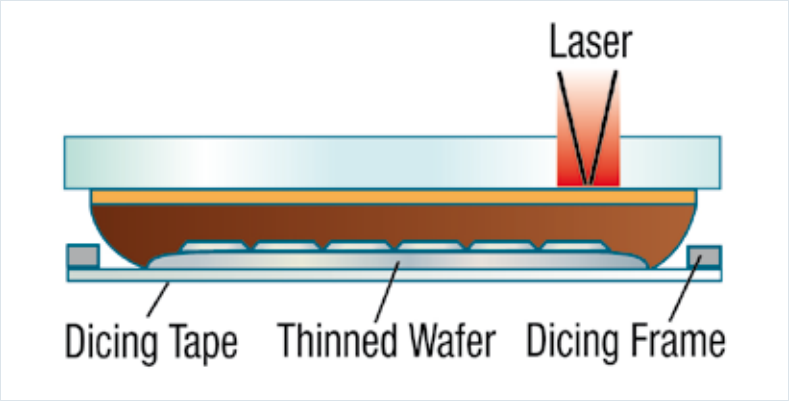


Sidebar to Step 1

Mounting Adhesive

Product Name	Base Resin	Color	Viscosity	Recommended Application
3M™ UV-Curable Adhesive LC-3200	Acrylic	Clear, light yellow	3500 CP @25°C	Low-temperatures; up to 150°C
3M™ UV-Curable Adhesive LC-4200	Acrylic, functional polymer	Clear, orange-brown	2150 CP @25°C	Intermediate temperatures; up to 180°C
3M™ UV-Curable Adhesive LC-5200*	Acrylic, functional polymer	Clear, orange-brown	~2000 CP @25°C	Elevated temperatures; up to 250°C

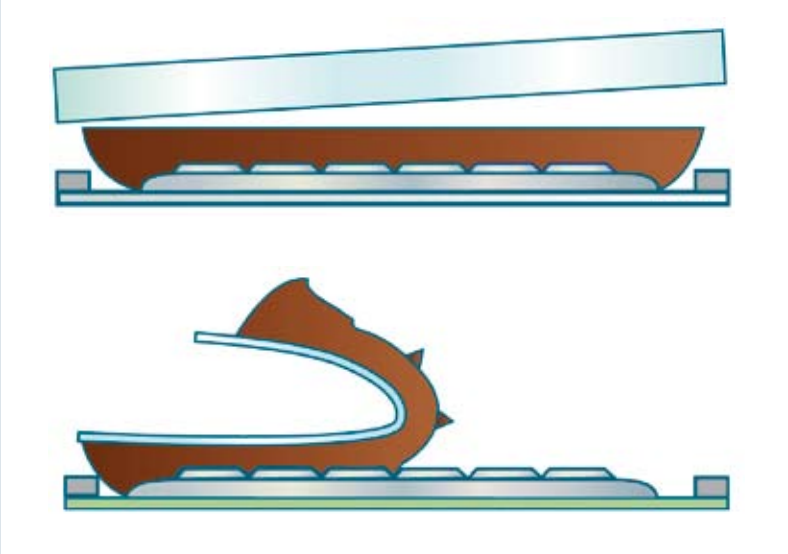
*Commercial release of 3M™ UV-Curable Adhesive LC-5200 scheduled for Q4 2009.



2. Backside Processing
Per customer specifications.

3. Tape Application
After the wafer is processed, standard dicing tape is applied to the back of the wafer. The wafer/glass carrier assembly is then placed in the de-mounting module, where the UV adhesive is de-bonded from the glass carrier using a laser.

4. Laser De-bonding
The laser debonding of the adhesive-glass carrier interface is uniform, so no damage to the wafer occurs when the glass carrier is removed. The 3M™ Light-to-Heat Conversion Coating (LTHC) absorbs the laser energy, generating localized heat in the LTHC layer, which destroys the bond between glass and adhesive. This frees the glass from the adhesive layer with very low separation force. The plate is then cleaned and re-coated with the 3M™ Light-to-Heat Conversion coating, allowing multiple uses.



5. Peel off UV adhesive layer
3M™ Wafer De-Taping Tape 3305 is used to peel the UV adhesive from the wafer. Residue levels on the wafer surface after adhesive removal are minimal, comparable to conventional backgrinding tapes, and typically no post-peel cleaning is required. Removal of the adhesive in this fashion also creates very little stress to the thinned wafer, and is compatible with low k dielectrics. (Sidebar to Step 5)

Designed to enable backgrinding and processing for any thickness down to 20 microns, the 3M Wafer Support System is also ideal for a variety of post-thinning process steps, such as stress relief and backside deposition, etch and metallization processes. And it is a high throughput, cost-effective process for through-silicon via and higher-temperature processes.

Sidebar to Step 5
Adhesive Removal

Product Name	Backing	Adhesive	Color	Standard Roll Length	Tape Thickness	Features
3M™ Wafer De-Taping Tape 3305	Polyester	Rubber	Translucent cream	100 meters (109 yards)	2.7 mils (0.069 mm)	High instant adhesion. Allows for smooth unwind of roll.

THE AUTHOR:

Blake Dronen,
Technical Manager, 3M Electronic Markets and Materials Division

Blake Dronen is a Technical Manager in the Electronics Markets Materials Division (EMMD) laboratory of 3M Company. He currently leads the development and integration of 3M adhesive technologies and equipment solutions for 3M's exciting new Wafer Support System (WSS) technology.

New SUSS MicroTec Bonders for Temporary and Permanent 3D Bonding Solutions

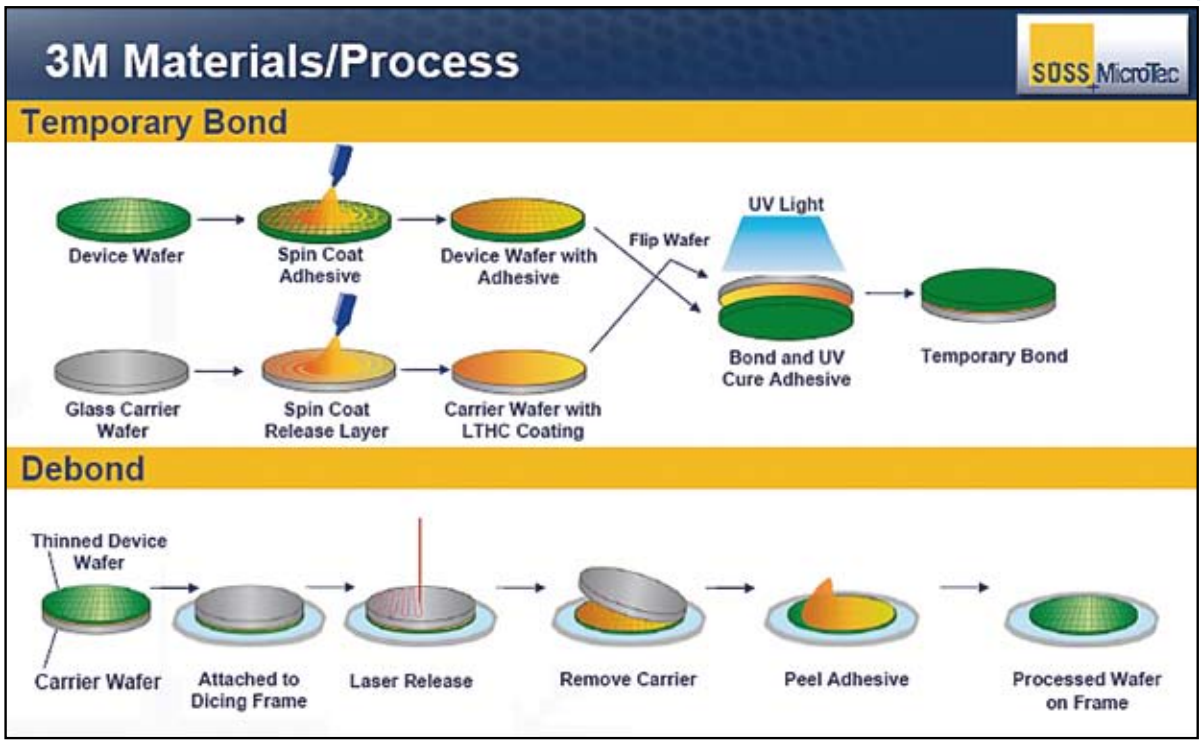
Reprinted with permission from Semiconductor International, Perspectives from the Leading Edge blog by Phil Garrou, June 24, 2009.

Phil Garrou – MCNC

Philip Garrou received his B.S. in chemistry from North Carolina State University and his Ph.D. in chemistry from Indiana University. He is an IEEE and IMAPS Fellow, and has recently served as president of the IEEE Components, Packaging and Manufacturing Technology Society (CPMT, 2003-2005). Garrou currently consults in the area of thin-film microelectronic materials and applications. He was most recently director of technology and director of new business development in Dow Chemical's Advanced Electronic Materials business.

SUSS MicroTec has announced an agreement with 3M to offer 3M's temporary bonding process as part of their new SUSS 300 mm bonder line.

The new SUSS XBC300 cluster tool allows connection of up to 3 different modules, as is shown, from the group consisting of: coater, bond aligner, low force bonding chamber, high force bonding chamber, cooling and unload module, plasma activation chamber, wet chemistry cleaning chamber, formic acid chamber and debond module. The



schematic of the CBC300 high volume cluster tool allows connection of six modules.

"These temporary and permanent bonding tools for 3D Integration are where we have been spending most of our R&D monies for the last 12 – 18 months." commented Wilfried Bair, VP Strategic Business Development at SUSS MicroTec.

TEMPORARY BONDING

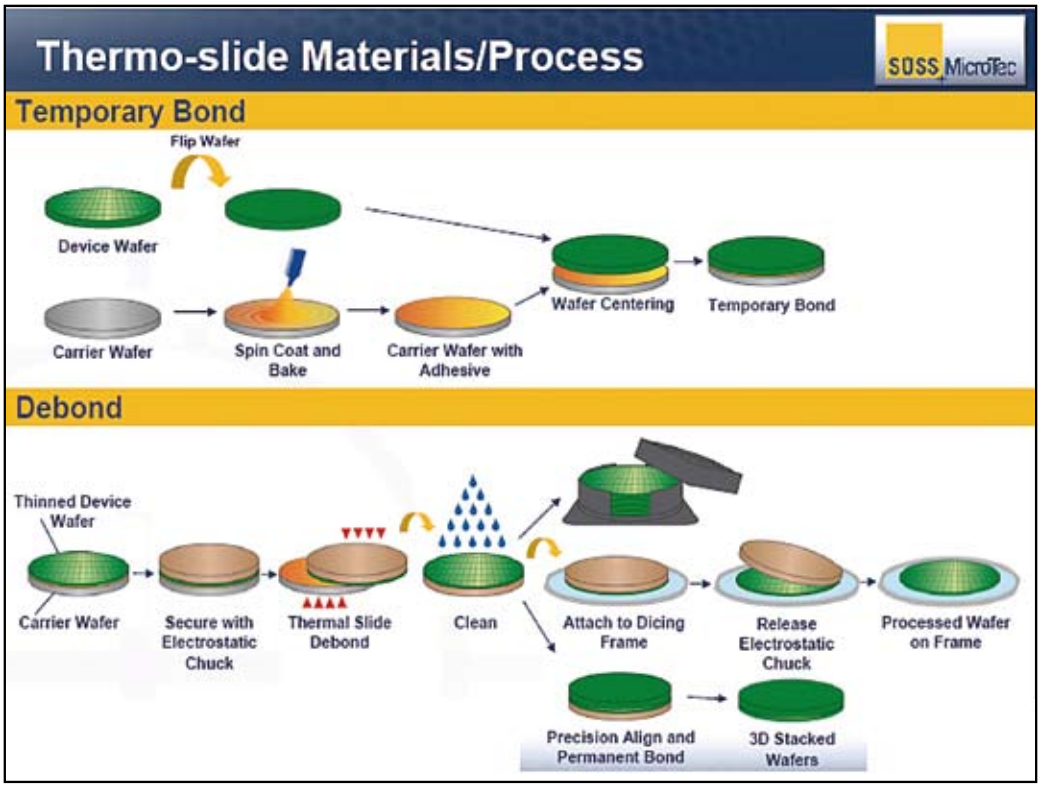
The cluster platform can be configured for any of the following temporary bonding processes. In all of these processes the thinned wafers, are always supported and end up on flex frames or other formats for dicing and subsequent D2W (die to wafer) stacking.

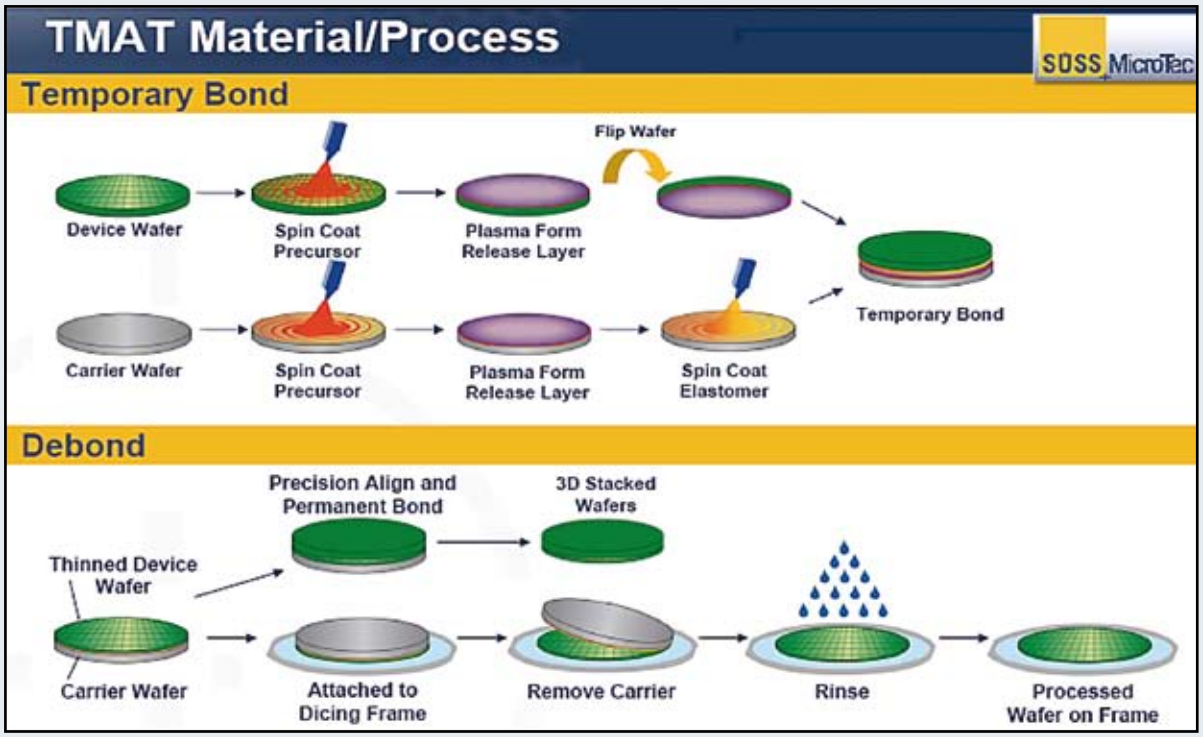
3M PROCESS

The 3M process has recently been reviewed [PFTLE "Temporary Bonding for 3D Thinning and Backside Processing", 05/25/2009] The UV curable adhesive and light-to-heat conversion (LTHC) layer used in the laser debond process will still be sold through 3M this gap looks really big.

THERMO-SLIDE PROCESS

The "thermo-slide process is shown in the figure below. The process has been developed for thermoplastic materials such as the well known Brewer Science HT-10.10. The novel use of an electrostatic chuck to hold the wafer during the thermo-slide process and subsequent attachment to the dicing frame reportedly results in an extremely low stress process for removal of the thinned wafer.





TMAT PROCESS

SUSS has been working with Thin Materials AG based in Eichenau, Germany on a temporary bond/ debond process. The wafers are first coated with a thin (few hundred nm) proprietary release layer and subsequently bonded with silicone elastomer at 180°C. Wafer thinning down to 50 µm and heat resistance above 250°C has been documented. After thinning and attachment to the dicing frame the carrier substrate is lifted off at room temp and the remains of the release layer are rinsed off with a simple hydrocarbon.

Bair indicated that ”All three processes are fully documented and the choice of process will be left up to the customer”. SUSS offered a temporary bonding workshop at Semicon West on July 15th where all of the aforementioned processes were discussed. Contact SUSS for the workshop proceedings.

PERMANENT BONDING PROCESSES

The same equipment platforms can be configured to perform permanent bonding for 3D IC die-to-wafer (pre populated) or wafer to wafer bonding.

The Cu-Cu Bonding process flow consists of a bond aligner, a high temperature bonding chamber, a cooling and unload module and the formic acid vapor module for cleaning the copper surface immediately before bonding. The high volume CBC300 would allow the bonding process to have multiple bonding modules in order to increase throughput. Typical post bond alignment accuracy is within +/-1µm.

The Polymer Bonding process flow consists of a bond aligner a bond chamber and a cool and unload module.

The Fusion Bonding process flow consists of a wafer cleaning module, a plasma activation module (optional) and a bond aligner. The process of record achieves a bond strength 1.8J/m^2 (NH4OH chemical activation, no plasma), 2 hr / 300°C anneal or a bond strength of 1.3 J/m^2 following a 300°C – 2hr anneal.

Bair concluded: “Protecting the capex investment for our customers by offering a flexible equipment platform to cover all new permanent and temporary bong processes was our main development goal for the XBC300 and CBC300 platform. With an easy field upgrade a customer can change configurations to adopt new or different processes.”

200 mm MEMS Pilot Line at Fraunhofer ISIT

Figure 1: Development and production center for microelectronics and microsystems technology.

Dr.-Ing. Wolfgang Reinert and Dipl.-Ing. Claudia Funk, Fraunhofer Institute for Silicon Technology (ISIT)

ISIT has set up a leading-edge pilot line for 200 mm MEMS wafer processing which is operated jointly with an industrial partner. ISIT staff concentrates on new device designs, process technology developments and is also responsible for the process availability. The industrial partner runs the operations and is responsible for logistics control and production liability. The operations are certified by ISO 9001:2000 and audited by industrial customers. All process flows in this pilot line are controlled by PROMIS. PROMIS is an industry standard shop floor system that also facilitates very complex flows. The computer controlled lot tracking allows an individual wafer to be traced through all the process steps it sees, as well as the machine conditions it is subjected to, all measurement results and many more parameters. ISIT runs two clean rooms which are locally separated areas with individual chemistry supplies for power-MOS and MEMS development and production.

A number of dedicated SUSS MicroTec tools were chosen for the MEMS cleanroom as these complied well with the requirements on development and manufacturing flexibility, wafer throughput, service availability and process yield.

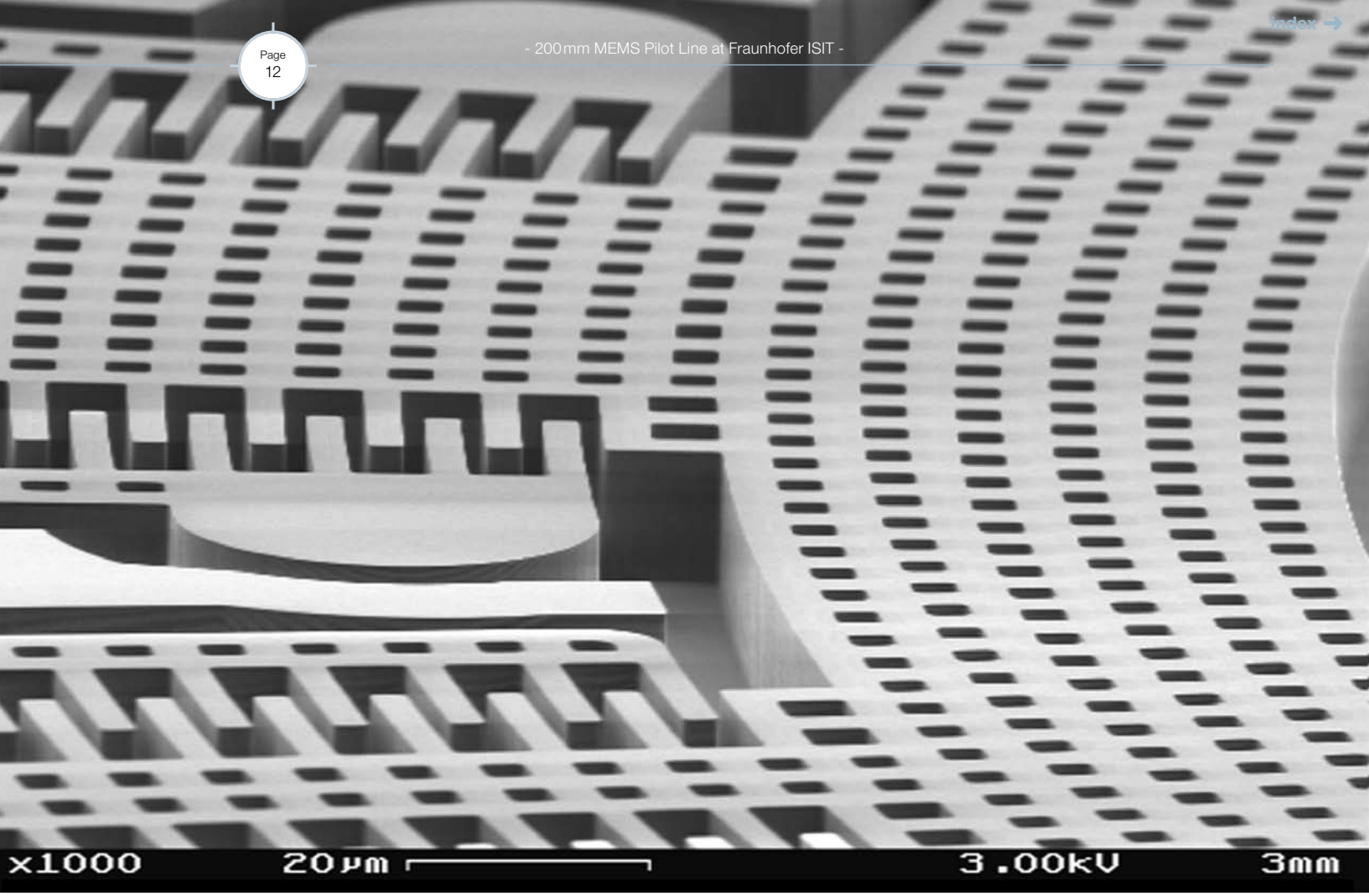


Figure 2
Micromechanic sensors with comb like electrodes enable precise measurements of acceleration and rotation.

The chosen SUSS MicroTec equipment is used for cap wafer manufacturing in multiple steps of the cap wafer flow including wafer bonding and device characterization.

The inertial sensor developments currently ongoing at ISIT are based on 11 µm thick poly-silicon as a functional layer for electrodes and moving structures, called the PSM-X2 technology platform, see figure 2.

PSM-X2 enables sensing electrodes, fine line lateral tracks and vacuum tight lateral vias in layers below the moving structures. The technology platform is automotive qualified.

Vacuum wafer bonding with metallic seal formation is a very effective technology to produce low-cost, hermetic sealed packages for robust precision microsensors and actuators. In addition to protecting the device from outside environmental stresses, the package must also provide an interior environment compatible with the device performance and reliability specifications.

DOUBLE SIDE WAFER LITHOGRAPHY

Cap wafers are unique because they are typically processed on both sides. Double side wafer processing requires double side polished wafers and double side lithography. On the outside, alignment marks for wafer bonding, cap wafer dicing and optional characters for single device tracebility are etched into the top surface. The inside of the cap wafer is structured with seal frames that are plated with a specific metal stack for eutectic bonding. For this purpose, ISIT has learned to master lithography in very deep cavities or thick resist on narrow seal frames with extreme topography to define the elec-

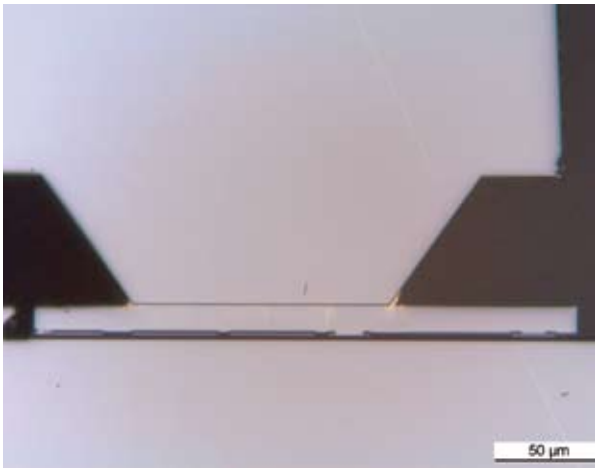


Figure 3:
Cross-section of eutectic AuSi bonding Metallographic cross section of eutectic AuSi seal

troplated solder metallization. Within the cavities, it is possible to provide optional stopper structures, getter layers, Faraday shields, vias or even IR antireflective textures.

ISIT prepares the photoresist for MEMS wafer processing on a SUSS ACS200+ resist cluster and uses a SUSS MA200 Compact exposure tool for single side and double side lithography. Details down to 0,8 µm are achieved with a Canon 2x wide field stepper type FPA-3000iW which also defines marks for the MA200 alignment. This combination allows for very high lateral precision lithography in deep cavities or on wafers with high topography while securing high wafer throughput and keeping cost low. Due to cavity etching either by KOH, TMAH or DRIE sometimes up to several hundred µm deep, the cap wafer presents a challenge to the resist coating process. A SUSS resist cluster ACS 200+ is able to cope with these demands. Spin on and resist spray coating are used on separate stations without tool changes and both have different defined thicknesses. As an example, for electroplating an up to 7 µm thick metal seal frame, the special requirement is to achieve a 10 µm resist thickness on top of a narrow silicon frame, while avoiding excessive resist pile up in the cavity.

Figure 4:
Clean room finger with three SUSS SB8e wafer bonders and BA8 wafer aligner

METAL SEAL BONDING

A number of technological topics are to be taken care of to produce hermetic sealed, micromachined devices on wafer level with controlled cavity pressures ranging from 10^{-4} mbar to 2000 mbar.

Wafer-level processes are particularly interesting for MEMS packaging since they can reduce fabrication costs and open up possibilities for batch processing. Various wafer level sealing technologies may be used, including wafer bonding, cavity sealing by thin-film deposition, and reactive sealing. In addition to maintaining vacuum, encapsulation on wafer level solves the problem of device protection during the wafer dicing operation. The improved robustnes of capped devices allows MEMS devices to be handled in existing standard semiconductor backend processes.

ISIT has worked on a high resolution glass frit seal process in the past and transferred this technology to a high volume MEMS manufacturer. For 8 years the focus of research activities has been on metalic seal bonding. Currently two different eutectic bonding processes are qualified: AuSi and AuSn. Both processes allow the integration of thin film getter to stabilize the damping atmosphere over a demanded device lifetime of 15 years and the seal hermeticity is better $4{\cdot}10^{-14}$ mbar·l/s standard air leak rate. The AuSi eutectic bonding is a technology using eutectic formation at 363°C between a silicon sensor wafer and gold deposited on a separate silicon cap wafer. So only one wafer of the wafer pair needs to carry the gold metallization, which is usually the cap wafer. The bond temperature used is in the range of 400°C. This is compatible with aluminum bond pad metallisations. Due to the liquid melt formed, this technology tolerates wafer topography up to 500 nm, scratches and particles. The technology is compatible with the activation requirements of integrated thin film getter. Compared to glass frit bonding, AuSi eutectic bonding does not outgas during the wafer bonding cycle, and requires only very small bondframe widths. While 5 µm bond frames are already hermetic, ISIT designs bond frame widths typically in the range of 60 – 120 µm to increase the strength of the cap construction. The low stress eutectic AuSi bondline is unique because after the joining process is complete, its mechanical properties virtually will not change any further. This property is the enabling factor for precision sensors that are calibrated after the packaging operation and need the calibration settings to keep stable up to 20 years.

Eutectic AuSn bonding in comparison is performed around 300°C and tolerates wafer topography up to 2 µm, but both wafers need a metallic seal frame. Both seal technologies are tolerant to moisture and pass even extended pressure cooker testing without any problem.

GETTER TECHNOLOGY

The use of Non Evaporable Getter (NEG) material (Zr based alloy) is required to ensure suitable vacuum (total pressure under $1x10^{-3}$ mbar) and long-term stability in MEMS devices. The getter can chemically absorb all active gases, including H2O, CO, CO2, O2, N2 and H2. The main constraints imposed by the device design and process are the compatibility of the getter with the fabrication process, the thickness of the getter film and an activation temperature of 350 °C compatible with the bonding process.

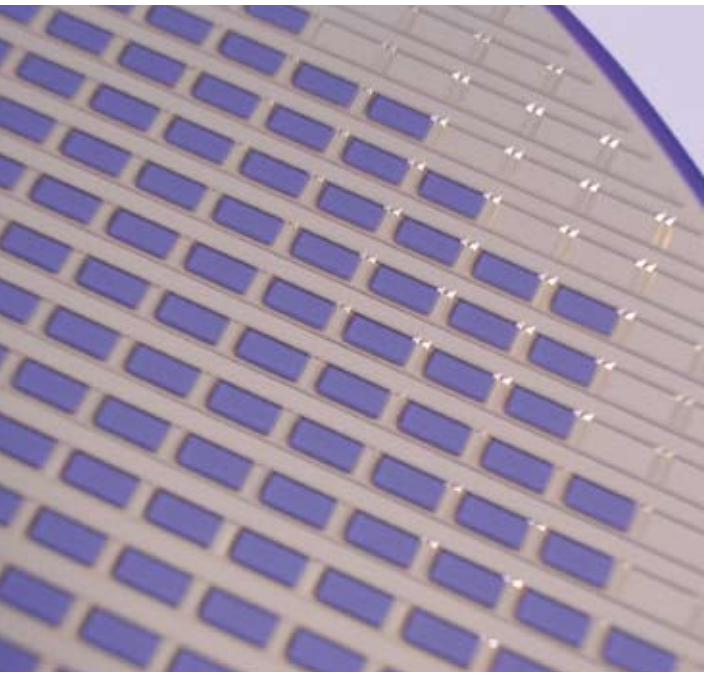


Figure 5: PaGeWafer®, cap wafer with deposited getter layers

The 2 µm thick getter film can be deposited into the cavities without affecting the lateral regions of the wafer where the hermetic sealing is to be performed. The typical pattern lateral dimensions are in the range of the millimeter, while the getter film can be placed in the cavities with any depths, ranging from few microns up to hundreds of microns. Figure 5 shows the precise deposition of the getter material inside the cavities.

As infrastructure for wafer bonding, ISIT operates one BA8 manual wafer aligner and three SB8e wafer bonders which have different features while still offering multiple functionalities. Two wafer bonders are equipped for both eutectic and anodic bonding, from which one bonder can anodically bond a triple wafer stack. All bonders are installed with controlled Argon backfill to define the damping atmosphere inside the sealed cavities in a range between 10^{-4} mbar and 2000 mbar. Without backfilling, a cavity pressure around 10^{-4} mbar is achieved with integrated getter. The highlight is that ISIT developed a process to realize individual cavities at different damping pressure on the very same chip in one wafer bond run. This process is realized with a combination of a gyroscope and acceleration sensor on a single chip. Besides the very precise backfill pressure control, the wafer bonders feature a very low temperature overshoot. High vacuum is achieved after a few minutes pump down, which supports our wafer throughput requirements. Sequential spacer removal (SSR) is a feature normally found only in full automatic SUSS wafer bonders that enables the retraction of spacers with very low friction, while two clamps still hold the wafer pair aligned. This function enables high alignment precision even with thick spacers that are better suited for evacuation and to compensate wafer warpage. The inspection in either IR transmission or X-ray transmission depending on the cap wafer construction verifies the bond result in a short loop.

FULL WAFER PROBING

Modern microresonating sensors demand a very low leak rate that cannot be monitored with the Helium leak test. ISIT developed the Neon Ultra-Fine Leak Test for resonating devices that can measure hermeticity with a leak rate sensitivity in the range of 10^{-16} mbar·l /s. The test is based on Q-factor monitoring before and after a defined exposure in Neon test gas. The in-line critical leak rate testing on wafer level itself is performed as a 100% test screen on PA200 semi-automatic SUSS wafer probers that are equiped with hot chucks. ISIT operates 4 of these probers to check a large number of sensor characteristics with single device traceability and yield engineering capability. The test methodology will become part of a new SEMI standard that is in work right now. The leak test indicates a sealing yield of better than 95% of mechanically good devices.

The test procedure is compatible with integrated getter films. The use of inert gas is mandatory for the leak

Figure 6: SUSS PA200 MEMS wafer probers are used for sensor characterization and leak test by Q-factor monitoring

Figure 7:
Double side lithography for cap wafer processing is performed with a SUSS MA200 Compact

test as all other active air gases will be gettered and do not increase the cavity pressure. The new in-line ultra-fine leak test is uneffected by the typically very small cavity volumes. Other than with all existing fine leak tests, the sensitivity of the test increases with decreasing cavity volume, as the pressure increase during the Neon exposure is larger in a smaller cavity for a given leak rate and exposure time. The test is not limiting the lateral size and pitch of devices on a wafer. Only the ability to access the bond pad locations with a needle prober is required. The Q-factor measurement of every single device is highly selective and not affected by leaking neighboring devices. The Neon tracer gas is selected to achieve a high leak penetration rate but on the other side prevent permeation through the wall materials of hermetic devices. In order to define the necessary test gas exposure parameters, ISIT has developed a vacuum lifetime model that can be tailored to a variety of device characteristics and field use conditions.

OUTLOOK AND CONCLUSIONS

The road map for further developments forsees low stress through silicon vias for bending sensitive sensors that will allow flip chip bonding of sensors directly to the driving ASIC. The formation of a low temperature metallic seal and micro via contacting at the same time, is another capability which ISIT has shown on a feasibility level but will see further investigation in the next future. The ISIT 200 mm pilot line with PROMIS lot tracking is a very attractive service offer for applied research, process development and 0-series manufacturing.

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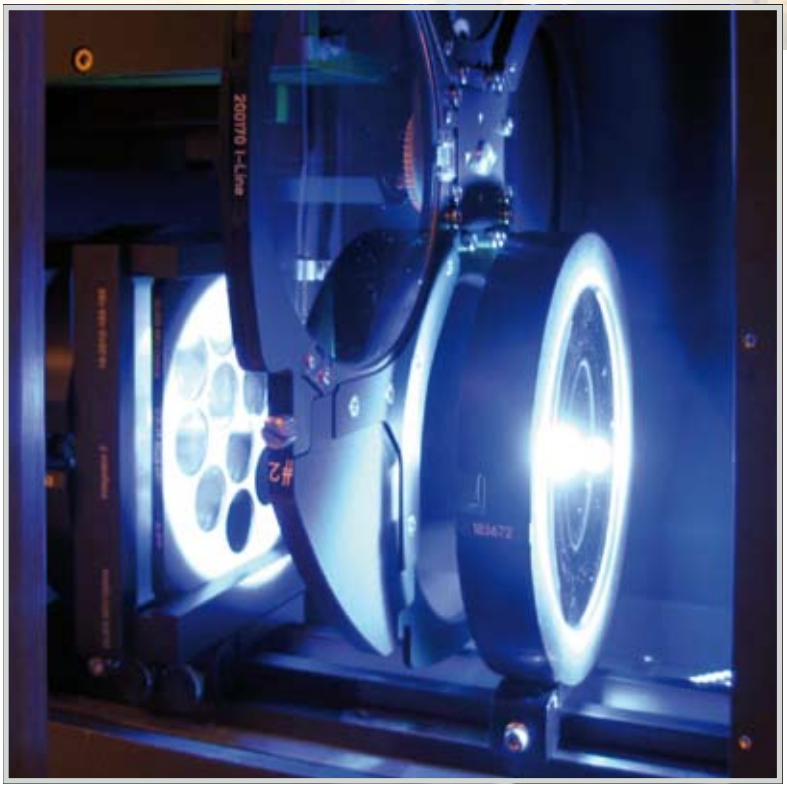
In the Spotlight

MO Exposure Optics: Customized Illumination for Process Window Optimization and Yield Improvement. Exclusively for SUSS MicroTec Mask Aligners

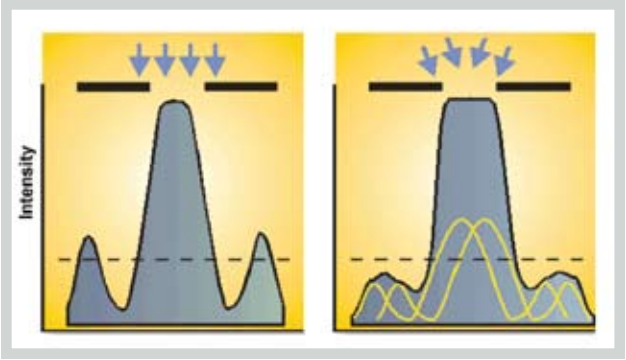
Reinhard Völkel

Since the very beginning of Semiconductor Industry in the early 60s, Karl Süss' Mask Aligners have been the workhorse of success and the backbone of the prospering SUSS group. Founded 1949, the SUSS group has sold more than 4'000 Mask Aligners. As the semiconductor industry as a whole, Mask Aligners have changed much over the years: Evolution from manual 2'' contact printers to the fully automatic LithoPack 300 cluster.

One thing that never changed significantly in all these years was the Mask Aligner optics. Contact- and Proximity Lithography suffer from diffraction effects (side-lobes) and the SUSS concept of a "Diffraction Reduction" illumination (Fig. 1, right) successfully suppressed these side-lobes – better than all our competitors could ever do. SUSS has developed a variety of different illumination settings to better serve specific customers' needs and different tasks. Which one is the best? Sometimes a difficult choice and a change of the optics is cumbersome and expensive. Previous generations of SUSS Mask Aligners were equipped with A-Optics or D-Optics. Today, HR-Optics (high resolution) is the first choice for contact- and proximity lithography with small exposure gaps; LGO-Optics (large gap) is for thick resist processes and 3D Lithography.



MO Exposure Optics in MA200Compact



SUSS MicroTec now introduces the next generation of Mask Aligner Optics, the MO Exposure Optics! This new illumination concept is based

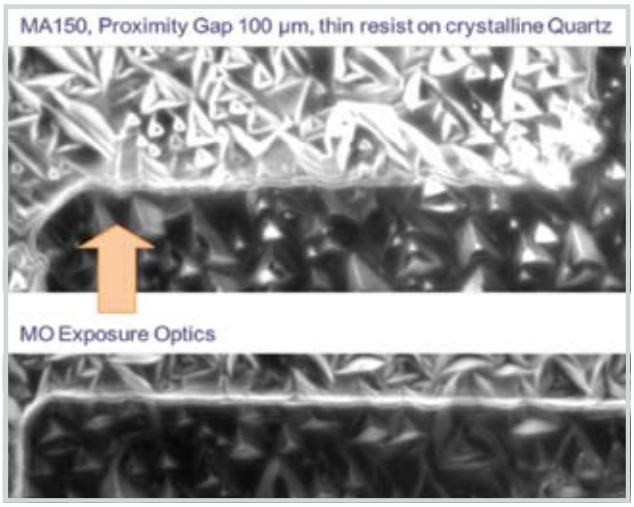
Figure 2:
The MO Exposure Optics Kit consists of a basic library of Illumination Filter Plates (IFP) and allows a simple upgrade of all SUSS Mask Aligner lamphouses.

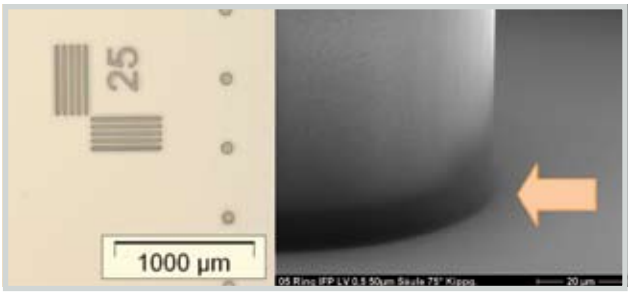
on Micro-Optical Integrators made of high-quality microlens arrays and an exchangeable Illumination Filter Plate (IFP). MO Exposure Optics provides excellent uniformity (around ±2%) with no lamp readjustment over full lifetime, improved telecentricity and customized illumination, the free choice of illumination settings to further optimize the process window and yield in contact and proximity lithography. MO Exposure Optics fits well in all existing SUSS Mask Aligner illumination systems. Changing to MO Exposure Optics is a simple Plug & Play operation. MO Exposure Optics is delivered with HR (high-resolution) and LGO (large gap) illumination settings.

By a simple change of Illumination Filter Plates (IFP) the user can choose his preferred diffraction reduction to improve depth of focus (DOF) and exposure latitude. MO Exposure Optics is providing a precise angular spectrum of the illumination light and also allows Optical Proximity Correction (OPC) in Mask Aligners.

MO Exposure Optics is patented and was developed exclusively for SUSS MicroTec Mask Aligners by SUSS MicroOptics, the leading supplier for high-quality optics solutions in illumination, laser beam shaping, metrology, medical and vision systems.

Figure 4:
MA25, Improvement of CD (Micro Crystal, SiO2 Tuning Forks)





MO Exposure Optics is available exclusively on SUSS MicroTec Mask Aligners. Retrofits allowing the easy and fast upgrade of older generations of SUSS MicroTec Mask Aligners are available.

Figure 5:
MA56, Improvement of Footing & Sidewalls Thick SU8
SU8: 300µm thick, soft contact, resolution 25µm (Courtesy of MRT Microresist Technology Berlin)

Figure 6 :
MA6, Grey-Level Mask and Proximity Printing
Full wafer micro- and nano-structuring
(Examples: 10µm proximity gap, different IFP-Filters)
(Courtesy by Fraunhofer IOF, Jena)

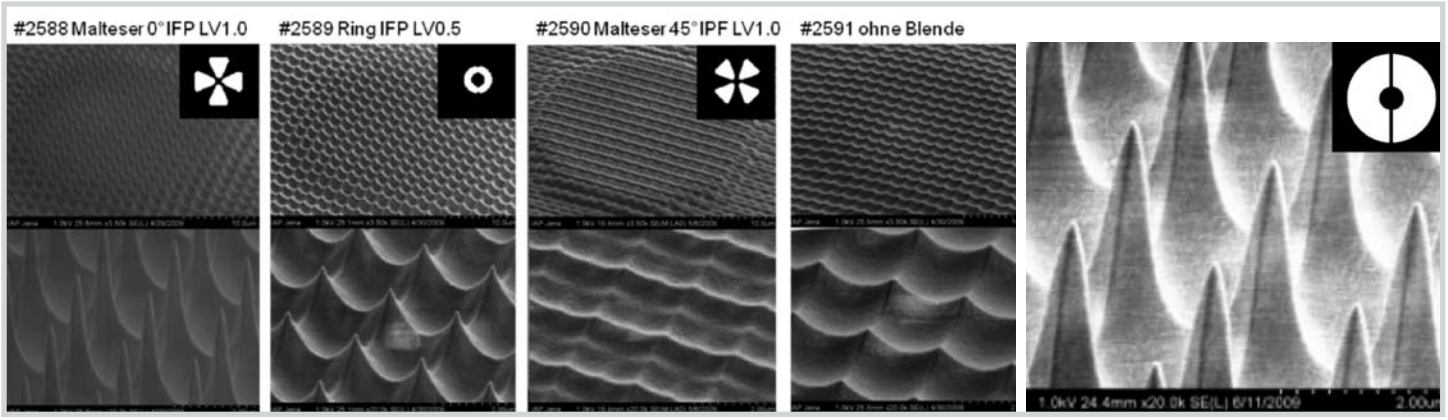
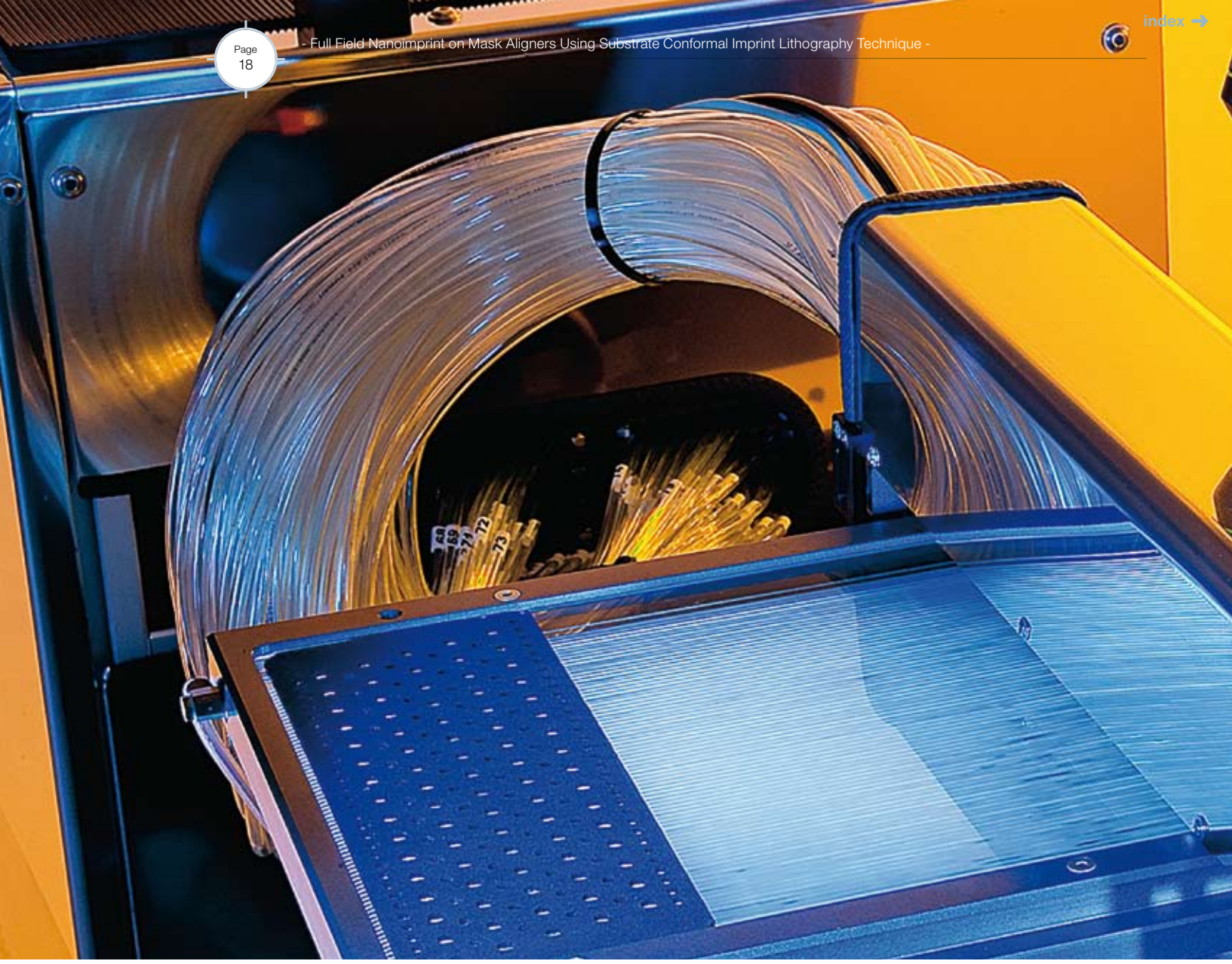


Figure 3: Library of Illumination Filter Plates (IFP) for MO Exposure Optics

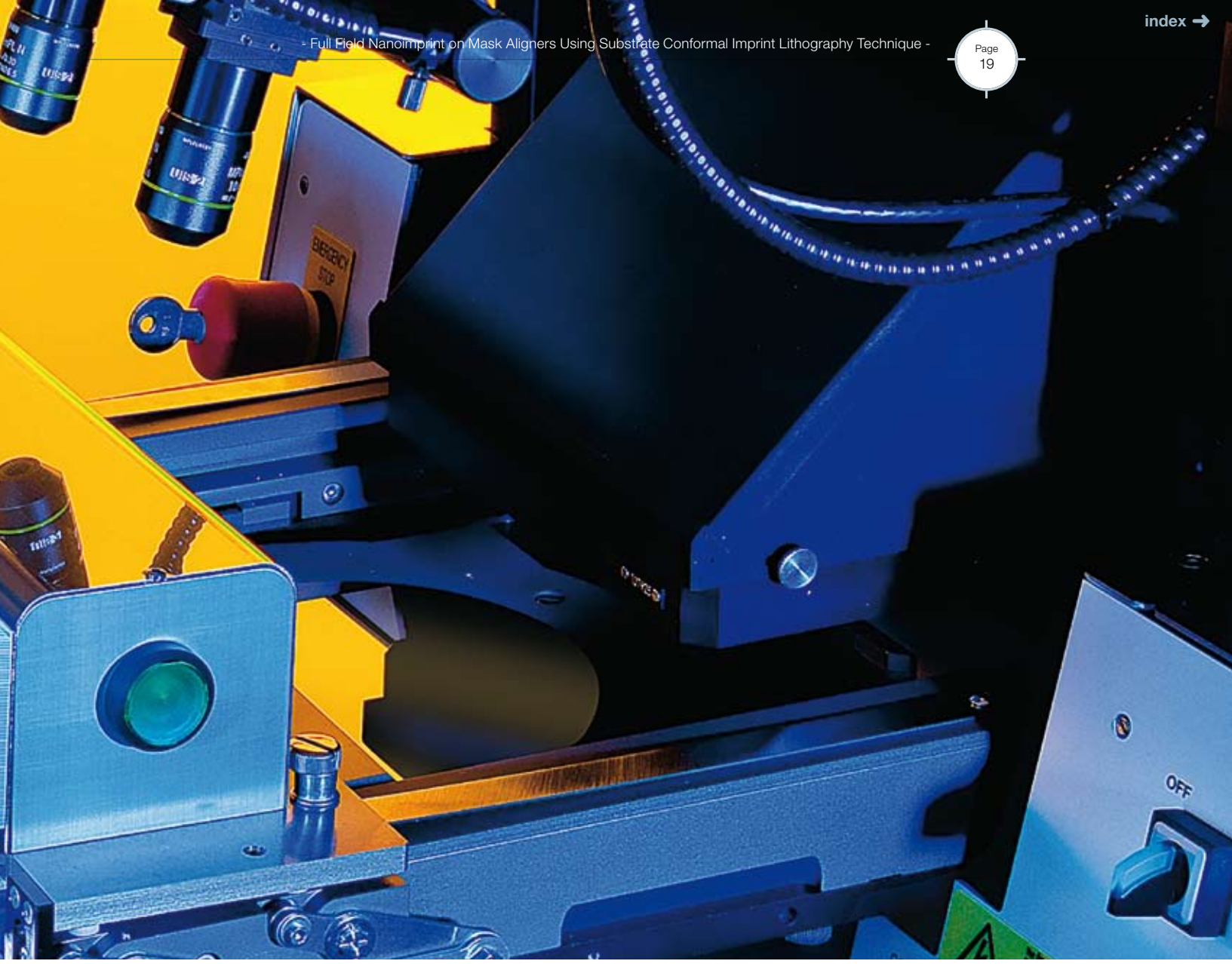


Full Field Nanoimprint on Mask Aligners Using Substrate Conformal Imprint Lithography Technique

Ran Ji, SUSS MicroTec
Marc Verschuuren, Philips Research, Eindhoven, Netherlands

INTRODUCTION

Nowadays, the development of integrated circuit (IC) industry and scientific researches rely more and more on the nanofabrication technologies. The resolution limits of optical lithography are very real even with a number of "optical tricks" at work. E-beam lithography (EBL) provides excellent resolution down to several nanometers. However, the throughput of EBL is too low for mass production due to its scanning exposure principle. Nanoimprint lithography (NIL) has been included on the ITRS lithography roadmap for 32 nm, 22 nm and 16 nm nodes. This parallel patterning technique shows great potentials in fabrication of nanostructures with high resolution at low costs.



Among the established NIL technologies, UV-NIL has attracted considerable attention due to its high resolution, high throughput and low line width roughness (LWR). UV-NIL with rigid quartz stamp provides excellent resolution down to sub-20 nm, however, the imprint area is limited by substrate waviness to less than 1 inch area. In addition, the fabrication of rigid quartz stamps is relatively expensive and the direct contact of the stamp with substrates can easily lead to permanent structure damages. UV-NIL with flexible stamp, e.g. PDMS stamp, allows large area imprinting and can lower the stamp fabrication cost since thousands of copies can be reproduced from one master stamp. On the other hand, the flexibility of the stamp has the disadvantages of lateral stamp distortion and structure deformation caused by backside pressure during the imprint process. Therefore the resolution of UV-NIL with PDMS stamp is normally limited to several hundreds of nanometres.

A novel NIL technique developed by Philips Research and SUSS MicroTec Lithography GmbH, substrate conformal imprint lithography (SCIL), bridges the gap between UV-NIL with rigid stamp for best resolution and soft stamp for large-area patterning. Based on a cost-effective upgrade on SUSS mask aligner, the capability can be enhanced to nanoimprint of sub-10 nm on up to 6 inch area without affecting any established conventional optical lithographic process on the machine.

SCIL STAMP FABRICATION

In order to reduce the cost of ownership) of large-area imprint stamp, the SCIL process uses flexible multilayer working stamps replicated from the original master stamp. SCIL master replication tooling (MRT) and automatic separation tooling, which allow the end-users to produce high quality SCIL stamps with own masters themselves, are developed by Philips Research and available from SUSS MicroTec Lithography GmbH. The PDMS working stamp is replicated from the master and glued onto a thin glass carrier in MRT (Fig.1). On one hand, the rigidness of the glass carrier avoids lateral stamp trapping caused by vacuum fixing on the stamp holder; on the other hand, the flexibility in vertical direction of

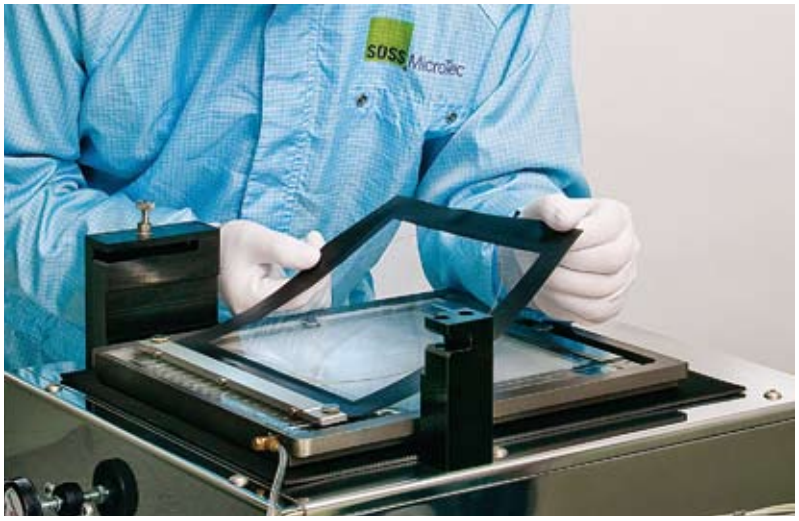


Figure 1:
SCIL uses a flexible PDMS stamp that allows the conformal imprint over large area.

the thin glass and PDMS allows the conformal imprint over large area.

SCIL PRINCIPLE

Although the PDMS stamp can compensate the waviness of the substrate, the local stamp trapping caused by stamp replication can lead to non-conformal imprint or "bubbles" in case of using perpendicular imprint process. To achieve a substrate conformal contact between working stamp and substrate, the SCIL process relies on a sequent approaching process and the capillary forces of the liquid imprint resist surface. The approaching of the flexible stamp starts from one side and spreads to the whole stamp subsequently by releasing the vacuum holding grooves step by step on the stamp holder (Fig. 2 (a) to (c)). This sequent contact mechanism prevents from flexible stamp trapping and therefore ensures that the stamp follows exactly the undulating topography over whole substrate surface. The applying of capillary forces instead of backside pressure minimizes the structure deformation and lateral stamp distortion during the imprint process and actualizes a sub-10 nm resolution. After conformal contact over the entire substrate is carried out, the imprint resist layer is cured by UV-curing or diffusion of the solution into the PDMS stamp, in case of using UV-curable NIL resist or imprint sol-gel, respectively. The automatic separation of the stamp from the substrate is performed by switching on the vacuum in the grooves consequently, which is opposite to the imprint process (Fig. 2 (d) to (f)).

SCIL IMPRINT TOOLING RETROFITABLE ON A SUSS MASK ALIGNER

The SCIL imprint tooling is retrofitable on SUSS MA6 or MA8 Gen3 mask aligners. This upgrade can be installed on-site with very limited efforts. The SCIL process benefits therefore the advantages, such like precise alignment, automatic WEC (Wedge Error Compensation) and uniform exposure, from the mask aligners. The upgrade kit consists of a stamp holder, a frame adaptor for stamp holder, a substrate chuck, pneumatic controller and software. Substrates up to 150 mm in diameter or in special forms can be handled

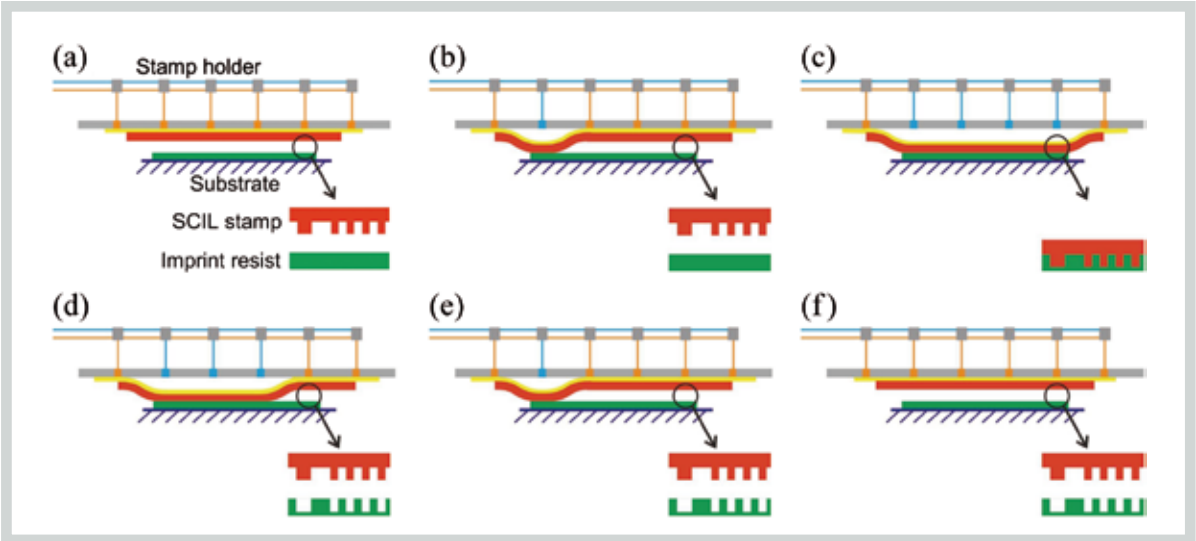


Figure 2:
Schematic illustration of the SCIL imprint and separation sequences.
(a) The SCIL stamp is fixed on the stamp holder by vacuum;
(b) the imprint process starts from one side of the stamp;
(c) the imprint is completed by releasing the stamp holder vacuum grooves one by one;
(d) after curing of the resist, the separation process starts from the other side of the stamp;
(e) and (f) the separation process is completed by switching on the vacuum in the grooves one by one.

Figure 3:
MA6 Mask Aligner with SCIL upgrade tooling

by the tooling. The software allows a quick switch between conventional lithography process and SCIL process. All relevant process parameters, e.g. WEC type, process gap, sequence step time, exposure time, etc, can be predefined in the software and the SCIL process can be carried out full- or semi-automatically.

EXPERIMENTAL RESULTS

In this paper, a 6 inch silicon master Figure 4 (a) (b) from AMO GmbH (Aachen, Germany) with 2D holes array . fabricated by laser interference lithography and etching processes has been used for stamp replication. Full field imprint with the replicated SCIL stamp has been carried out into a 120 nm thick imprint sol-gel layer on 6 inch substrate. After removal of the residual layer (ca. 20 nm) by RIE, the structures have been transferred into silicon substrate for 300 nm. Finally, the imprint sol-gel layer has been stripped by HF dipping. Fig. 5 (a)(b) shows the imprinted wafer after structure transfer and resist stripping and has demonstrated the imprint uniformity and structure fidelity of SCIL process.

Positive pillars and lines have also been imprinted by SCIL process. Fig. 6 (a) shows SEM image of imprinted pillars with a diameter of 64.4 nm and a height of ca. 135 nm. The residual thickness is only 26.4 nm,

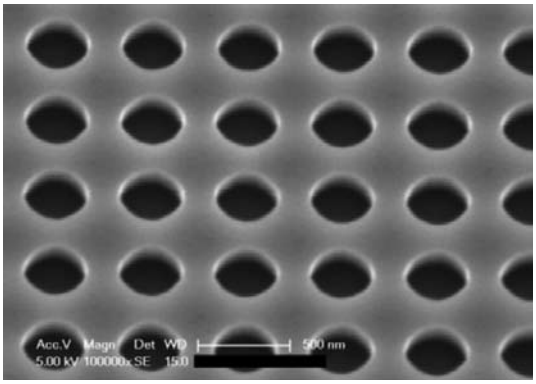


Figure 4:
SEM image of the silicon master with 2D holes array made by laser interference lithography and etching processes; the pitch is 513mm (±5% over 6 inch area); the diameter and the depth of the holes are 340nm and 200m respectively.

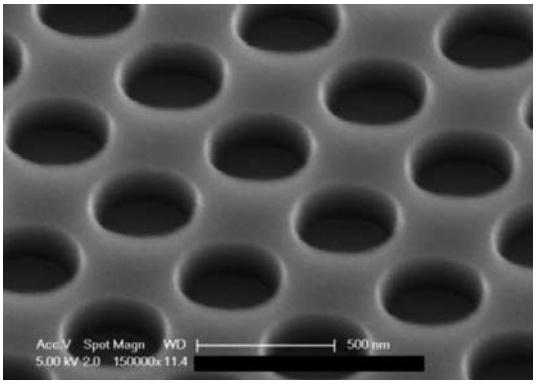


Figure 5:
SEM image of the imprinted wafer after structure transfer and stripping of the imprint sol-gel

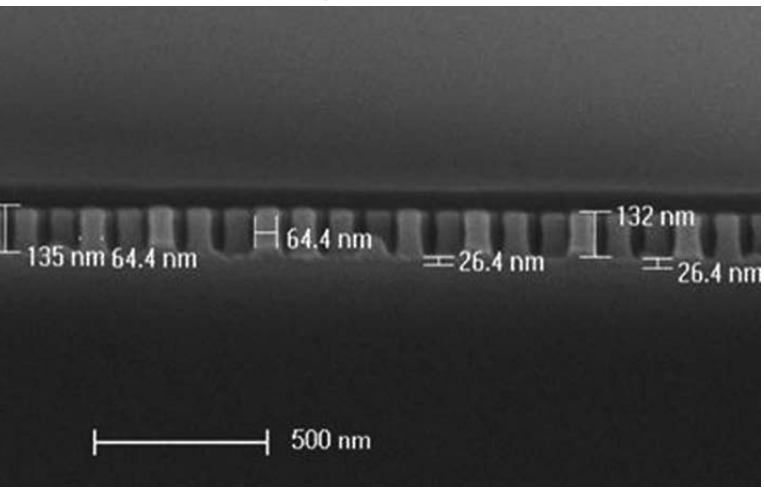


Figure 6a: SEM images of imprinted sol-gel structures: (a) side-view of pillars array with a diameter of 64.4 nm and height of ca. 135 nm, the residual thickness is 26.4 nm;

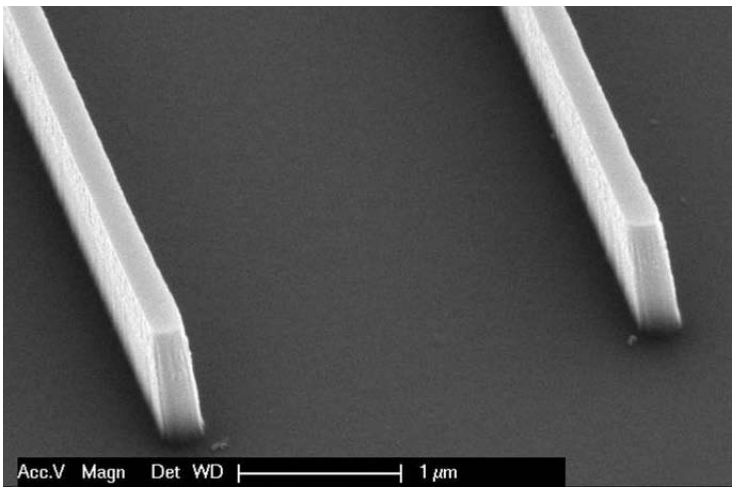


Figure 6b: SEM images of imprinted sol-gel structures: bird-view of high aspect ratio line structures with a line width of 200 nm, the aspect ratio is ca. 1:3 (width: height).

which can be removed by RIE process easily. Imprinted line structures with high aspect ratio shown in Fig. 6 (b) have a line width of 200 nm and the aspect ratio is 1 : 3.

In addition to sol-gel process, we have also demonstrated UV enhanced SCIL process. AMONIL (AMO GmbH, Germany) resist has been used as imprint resist for SCIL process. Fig. 7 shows SEM images of various imprinted structures made by UV-SCIL process. Benefit from the UV-curing the process time can be optimized to less than 2 min per wafer and the throughput increases therefore dramatically in comparison to sol-gel process.

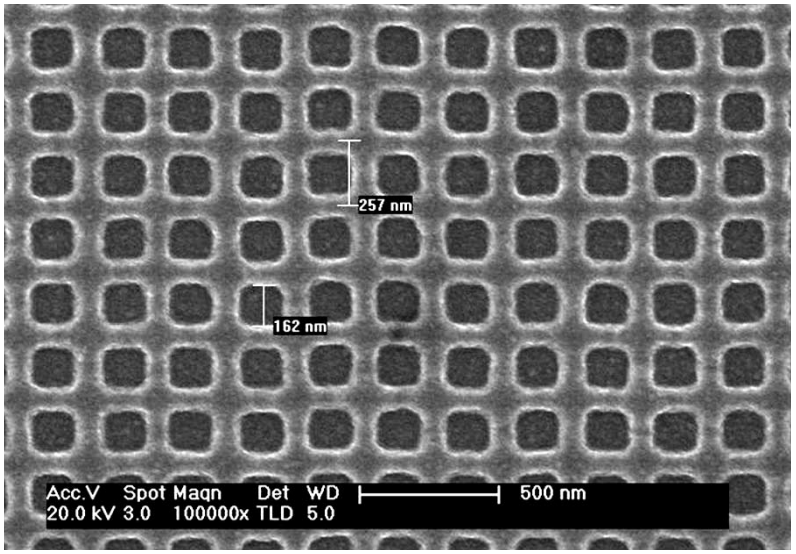


Figure 7a : SEM images of UV-SCIL results: imprinted square shape structures array, the side length is 162 nm and the space between two squares is ca. 100 nm.

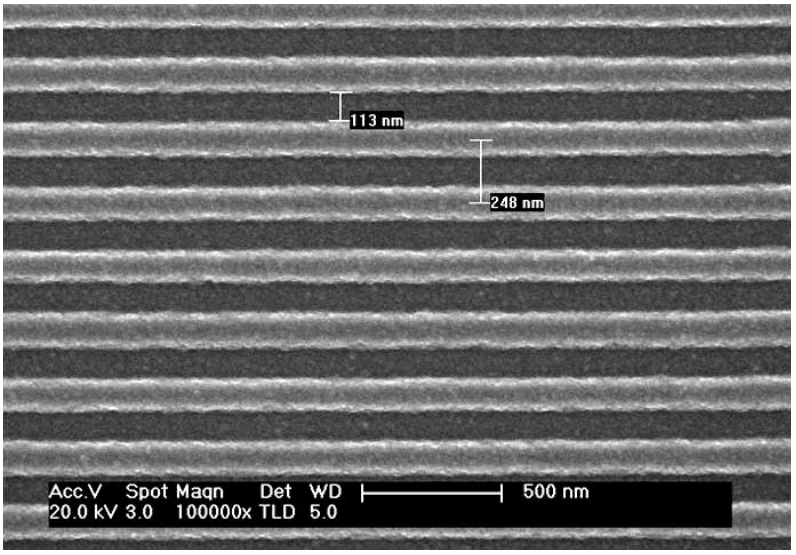


Figure 7b : SEM images of UV-SCIL results: lines and spaces structures with a pitch of 248 nm and a line width of ca. 135 nm

SCIL: PAVING THE WAY TO VOLUME PRODUCTION

The key success factor for industrialization of a NIL technique is the reliability of the process. Particle always plays as “killer” of NIL processes in the real production atmosphere. In case of using rigid quartz stamp, even a single particle on the substrate or the stamp will lead to wedge error, non-contact or permanent structure damage. SCIL technique is insensitive to particles by using soft PDMS stamps. The stamp covers so exactly over the topography of the substrate that particles can be “packaged” by the stamp. Fig. 8 shows a SEM image of SCIL imprint over a particle. The particle is even patterned with photonic crystal structures.

The unique imprint principle of SCIL and the composite stamp guarantee the conformal imprint and the compatibility for production atmosphere. This technique shows therefore great potential in high volume production due to its excellent reliability,

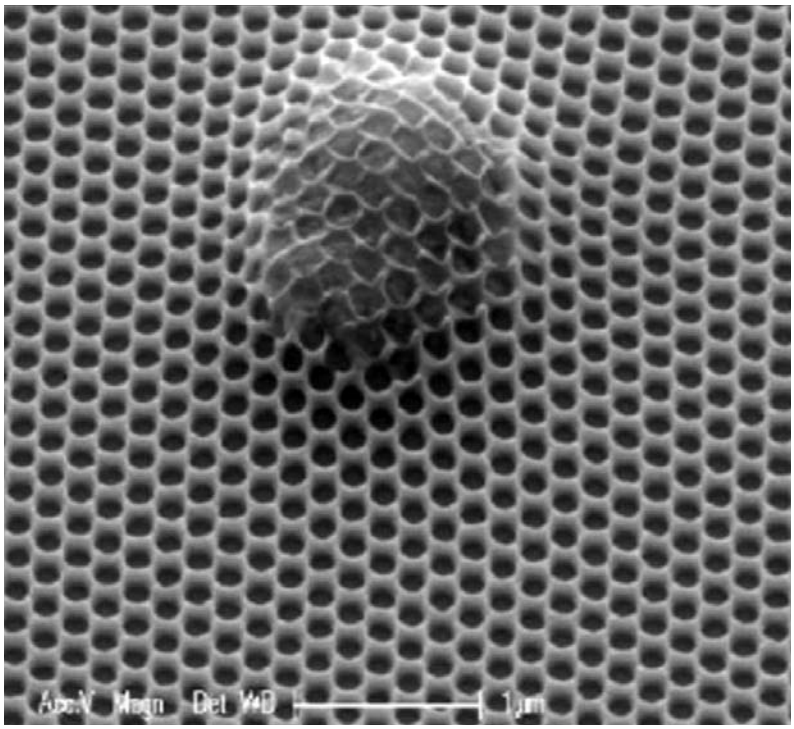


Figure 8:
SCIL imprint over a particle.
Even the particle has been patterned

especially in patterned media storage and HB LED applications.

The global LED market growths dramatically in recent years. However, the applications are dominated by backlighting for cell phones, PDAs, laptops, etc. In order to open the general lighting market doors, the efficiency needs to be improved significantly. Researchers have demonstrated that photonic crystal (PhC) or photonic quasi-crystal (PQC) structures on the LED wafers can enhance the extracting efficiency. NIL techniques have attracted considerable attention to fabricate those structures cost-effectively. However, the current established NIL technologies rely too much on the cleanness of the production atmosphere. The novel SCIL solution will drive the HB LED market towards high volume productions due to its high resolution, high throughput, low cost of ownership and repeatability.

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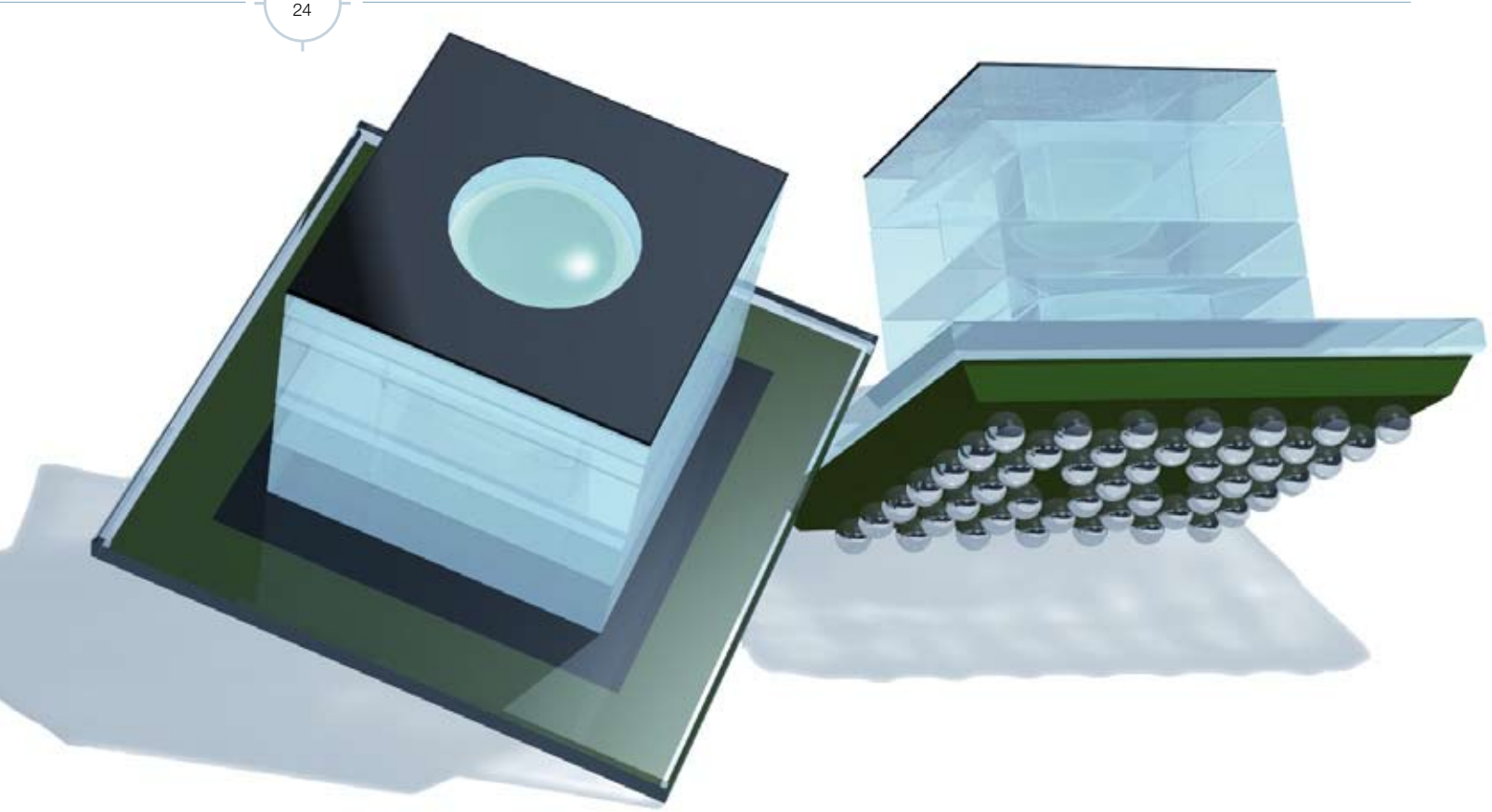

WAFER-LEVEL CAMERAS – NOVEL FABRICATION AND PACKAGING TECHNOLOGIES

Margarete Zoberbier, Business Development Manager, SUSS MicroTec
Andreas Kraft, Business Development Manager, DELO Industrial Adhesives

The increasing demand for more functions and features coming along with cost reduction plays a significant role in today's product design and manufacturing technologies of mobile devices such as PDAs, laptop computer and mobile phones. Besides the main function of the device, imaging is considered a core feature by the user and major mobile phone manufacturers. Therefore the industry puts a lot of effort onto performance improvements and the optimization of the manufacturing method of mobile phone cameras. Wafer-Level Camera (WLC) is supposed to be the technology of choice to address these requirements.

In recent years wafer-level packaging of CMOS image sensors has become a well established technology in the industry. This technology provides a cost efficient packaging method for shrinking device sizes coupled with higher I/O density.

In addition to this wafer-level optics is a novel technology that is designed to meet the demand for smaller form factors of the optical system and cost reduction in the next generation of camera phones. The optical components are fabricated by replicating the optics through a stamp material into a polymer layer, coated

on a glass wafer. Another key challenge is the wafer alignment. Replicated lens wafers are aligned and adhesively bonded at wafer level using a UV curing process in order to achieve excellent alignment results. Finally the bonded opto wafers are subsequently diced to form individual camera modules

wafers is transparent (glass) a live alignment is feasible. Due to the sensor dimensions typically the required post bond alignment accuracy is below 10µm. Followed that thermal curing takes place in the bonding chamber, e.g. SUSS SB8e. The given pressure uniformity of ±1,5% leads to excellent bonding results.

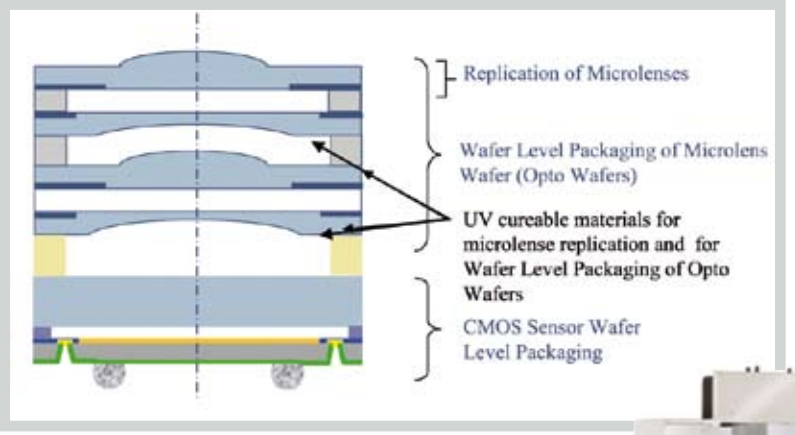

Figure 1.
Schematic of Typical Wafer Level Camera Design

TYPICAL WAFER LEVEL CAMERA DESIGN

Typically a wafer-level camera consists of two main pieces, the image sensor and the optics. Figure 1 shows such a schematic cross section of a classical wafer-level camera.

CMOS SENSOR PACKAGING (GLASS ENCAPSULATION)

In a camera device the CMOS image sensor needs to be covered by a glass layer to protect the active area. This is typically done on wafer-level using bonding techniques. The challenges in this process are high alignment accuracy and excellent temperature and pressure uniformity to achieve best yield. Void-free bond interfaces are also required. The most popular process is adhesive bonding, chosen because of low bonding temperature (below 200°C). Typically the adhesive is dispensed or rolled on frames located at one of the wafers. The next step is alignment of both wafers. As one of the

Figure 3
The SUSS MA8 Gen3 Mask Aligner can be equipped with dedicated tooling to manufacture WLC optics

FABRICATION OF OPTICAL COMPONENTS VIA UV REPLICATION

The replication of optical parts like lenses for WLC is mostly done by molding them from a stamp. Dependent on the method to be used while replicating the lenses, two different stamps are used. Hard stamps, mainly produced from glass, when the process involves squeezing a dispensed polymer droplet over the wafer area or the structures are embossed into a polymer layer spread over the wafer surface in advance as

Figure 2
The third generation MA/BA8 Mask and Bond Aligner is the new benchmark in full-field lithography for MEMS Advanced Packaging, 3D-Integration and compound semiconductor markets. In addition, it supports emerging processes like UV-NIL, bond alignment, UV-bonding as well as wafer level microlens imprinting and assembly.

In return the optics is manufactured using other machine types such as the SUSS MA8 Gen3 Mask Aligner equipped with dedicated tooling.

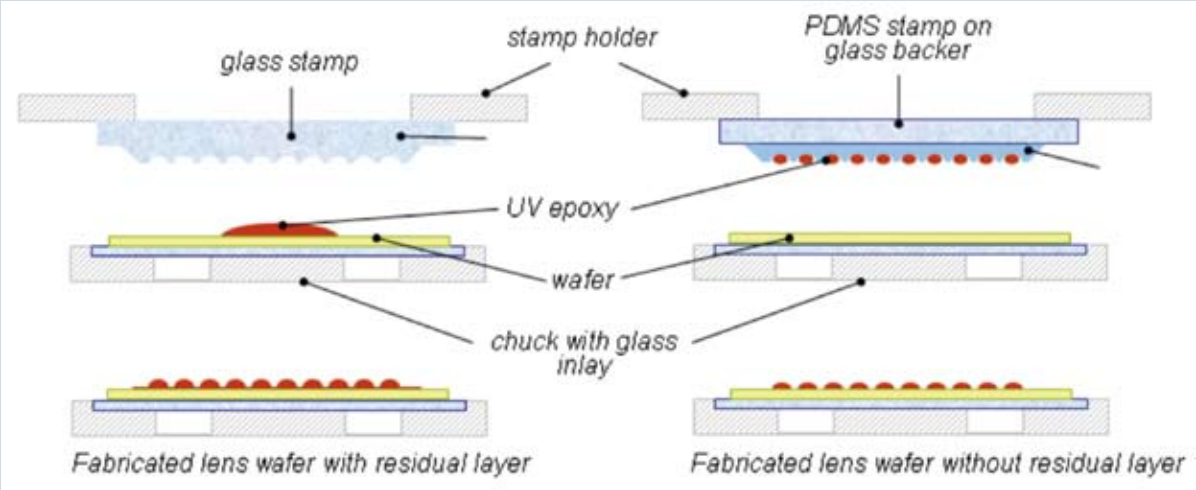

Figure 4:
Comparison between the main imprinting methods. Embossing with residual layer on the left, transfer print without residual layer on the right

it is frequently found in hot embossing. Soft stamps, usually produced from silicone rubbers (i.e. PDMS), when the polymer is dispensed into the single lens molds and the lenses are casted by transfer of these polymer droplets onto the supporting wafer (depicted in figure 4). Both methods have their pros and cons.

The glass stamp provides a very good control about its total thickness variation (important for the uniformity of the molding result and for the alignment accuracy, as described below) and enables the replication of even the smallest structures due to its high stiffness and resulting contour accuracy. On the other hand the hard stamp requires a base layer as a conformal printing over the whole wafer area is impossible between two hard surfaces. Additionally, imprinting into a predispensed layer requires big forces to displace the material. Machines supporting this imprint method have to be very warping resistant and need actuators that can provide these high forces and allow an active control of wedge errors. The silicone rubber stamp shows drawbacks as the hard to control total thickness variation, the shrinkage that can appear during stamp production and the worse resolution due to possible deformations in the stamp during imprinting. However, due to its soft surface that adapts to the wafer surface it can produce lenses without the presence of a residual layer. Therefore wafer warpage due to shrinkage of the lens material is strongly reduced. As a side effect also particle contamination is a less serious problem with soft stamps, leading to reduced clean room costs.

As mentioned above, the total thickness variation is not only a problem for the uniformity of the imprint result, but can also cause problems as soon as the replication process includes alignment between the lens layer and the wafer. While a wedge in the stamp can still be compensated by the wedge error correction system of modern mask aligners, substrate warpage or deformations of even higher polynomial grade cannot be compensated by machines. Therefore contact between different points on the wafer area is established at different times and leads to lateral forces between wafer and stamp which are hard to control.

These lateral forces are mainly caused by shearing of the stamp material due to the non-uniform load or by viscous forces caused by the non-isotropic flow of glue between the stamp and the wafer. Due to these forces shifts between stamp and wafer can occur during the imprint process. To compensate for the shifts, processes with multiple approaching and realigning steps are necessary.

Especially during the last steps of such an imprinting process the contrast of the fiducials, which are typically produced in polymer during the imprinting process themselves, can be very week. Here only the combination of well chosen microscopic techniques and made to purpose fiducial design can provide images offering sufficient reliability for auto-

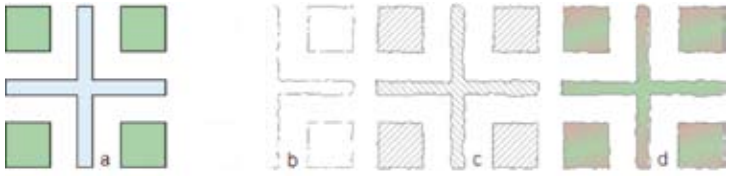

Figure 5:
schematic drawing of polymeric alignment marks and their microscope images. a) mark as designed, b) left half: very weak contrast as obtained with standard reflected light illumination, right half: stronger contrast with transmitted light. Still the pattern is not ideally suited for pattern recognition due to its narrow contrasted structures. c) internal surface patterning of the target to enhance contrast and create expanded structures d) contrast as obtained with DIC microscopy or similar method resulting in better contrasts and expanded structures

mated alignment. Fiducial geometry should take care about reducing deformations of the polymer pattern as well as about the needs of the pattern recognition systems.

To achieve highest reliability, the pattern recognition systems need expanded structures. Those expanded polymer fiducials may be created by dispensing opaque polymers onto the fiducial region or by creating rough surfaces which cause increased scattering, but further development is needed at this point (figure 5).

Also transmitted light microscopy can help to increase structure contrast. Besides that, the use of microscopy optics with small numerical apertures and advanced illumination techniques as dark field or DIC (Differential Interference Contrast) may be useful and are therefore options in SUSS machines.

WAFER-LEVEL PACKAGING OF OPTO-WAFERS

Certainly camera systems consist of several optical elements that need to be assembled quite accurately to provide the best possible optical performance. Until today camera systems have been manufactured by manually assembling lenses into a barrel. This procedure is very costly, time consuming and doesn't seem to be a reasonable approach for the manufacturing of multi level, miniaturized lens stacks that are supposed to be use in modern camera systems for mobile phones. Wafer-level bonding technologies seem to solve this issue. The industry started to use wafer bonding equipment platforms to bond lens wafers with spacer wafers or a second lens wafer with thermal curable adhesives. For this technology state of the art bond aligning and bonding tools can be used. The wafers with applied adhesive on one of the wafers get aligned, get clamped in a transport fixture and get finally bonded in a substrate bonder. However, this process has limits in terms of the achievable alignment accuracy. The reason is that thermal stress in the bond process and the required handlings from the bond align to the bond tool impacts the alignment accuracy and limits process reliability.

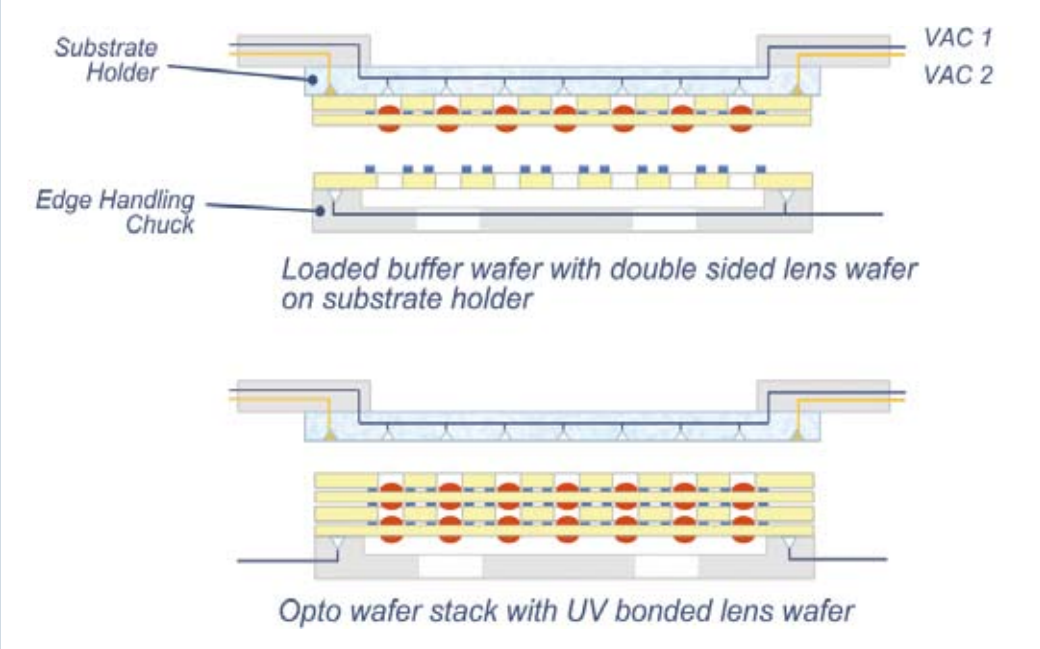

Figure 6:
UV bonding incl. in-situ alignment on the SUSS MA8 Gen3 with the usage of buffer wafers

As lens wafers are transparent for UV light the usage of UV curable adhesives seems to be the solution of choice for a cost effective and highly accurate wafer level assembly with "in-situ" alignment on a mask aligner type of equipment. Leading edge mask aligner technologies allow alignment accuracies well below 0.5µm and offer high intensity UV illumination for effective UV curing processes. The sequence of a UV bond is very similar to common mask aligner photolithography. Two substrates have to be aligned in an accurately controlled alignment gap and UV exposure finalizes the process step. However, for UV bonding the Mask Aligner requires a specific substrate holder that includes a UV transparent chucking plate to hold the top lens wafer. This is shown in figure 6.

The lower lens wafer is handled onto an exposure chuck which is typically designed for wafer edge handling or for the usage of "buffer wafer". Buffer wafers are typical spacer wafers (glass wafers with holes at the position and with the size of the lenses) that are needed and used to ensure a well defined and controlled distance between lens wafers. Both are dedicated to safely handle the wafers with replicated convex lenses.

Besides the alignment and bond equipment, the dispense technology and process play a significant role in the manufacturing of WLC. The dispense volume and pattern of the adhesive need to be controlled to achieve a void free and reliable bond interface. Too much material results in contaminated optical elements while too little material results in leakages of the module itself. The adhesive itself needs to be chosen carefully to match the general requirements to be a fast curing, highly reliable, dispensable and last but not least reflow compatible material. In addition material suppliers like DELO offer material with integrated filler particles to achieve a uniform and automatic residual thickness control by the material itself. With the use of opto wafers together with lenses that are embedded in the polymer, roller dispense processes can be adopted. This offers a much

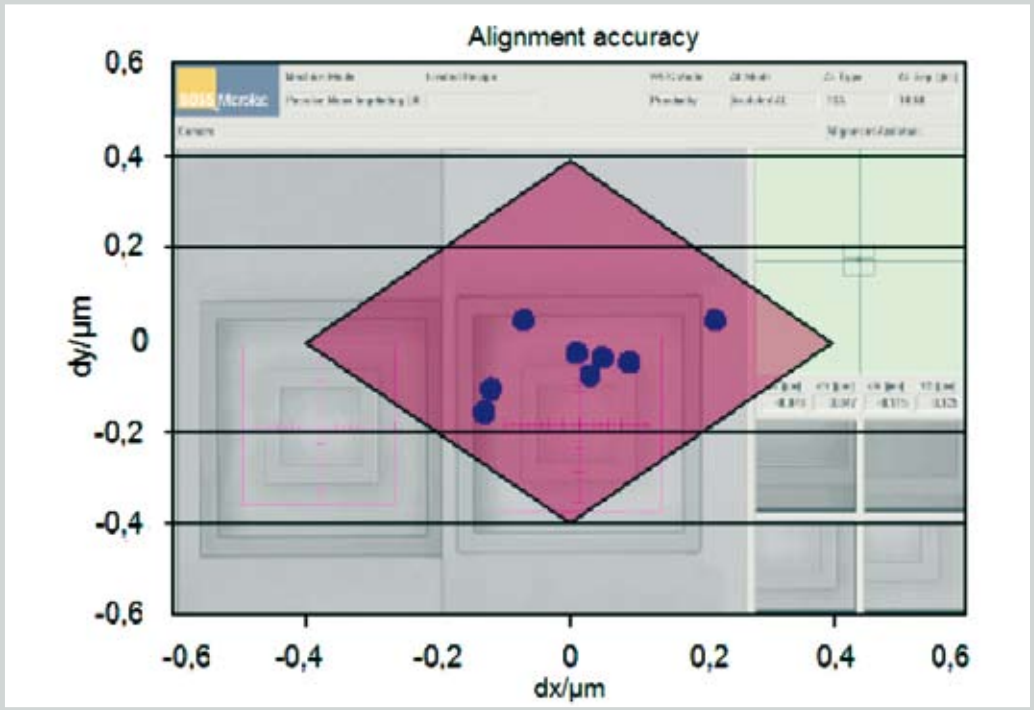

Figure 7:
Alignment results obtained during UV-stacking on a SUSS MA8 Gen3. The points represent results measured with the cognex system in the machine. Vernier measurements resulted in alignment accuracy better than the 0.4 µm resolution of the Vernier (red area)

easier dispense process but limits the design of the lens wafer. High accuracy alignment of opto wafers can be achieved on manual and automatic mask aligners from SUSS MicroTec. As described above, sophisticated toolsets are used to safely handle the lens wafers and to ensure an excellent levelling of both wafers during the gap setting and alignment step. One of the key challenges at the alignment process is the very large distance between alignment fiducials. Depending on the number of wafers to stack, the distance between the alignment targets can get up to several mm. The optical alignment system including the microscope and focus settings need to be highly accurate in design and setup. In addition, leading edge technologies like SUSS "Assisted Alignment", which provides live overlay measurements and direct operator feedback, are required to achieve alignment accuracies <0.5µm. Today, WLC lens stacks with sub-micron post bond accuracy are within reach when adopting UV bonding.

FAST UV-CURABLE MATERIALS FOR WAFER LEVEL CAMERA MANUFACTURING

UV curing adhesives are currently widely used for mass production in the electronics and optics assembly industries. Depending on the chemical basis – acrylic or epoxy- these materials differ in some of the basic parameters. Acrylic adhesives are known to be very fast curing, but are limited at high temperature processes and have high polymerization shrinkage. On the other hand, epoxy based system are known for good thermal stability and low shrinkage. Therefore they are used in high reliability applications, like automotive and optical assembly. The challenge for Wafer-Level Optics (WLO) manufacturing is to develop materials with fast curing mechanism, high optical transmission and high thermal stability (reflowable optics).

The following results show the current status of the material development within DELO:

a. Fast curing with good adhesion

Due to the reflow requirements in the WLC module and the high throughput needed for low cost wafer level manufacturing, DELO has developed new fast UV-curing epoxy-based adhesives. Referring to figure 8 the initial strength of glass samples is reached very fast, at 10 sec after exposure.

b. Adhesion to Stamp Material

For imprint materials, it is very important to have excellent adhesion to glass (wafer), whereby the adhesion to the stamp material should be as low as possible. In our tests, all printed optics wafers could be easily removed from the used stamp material (2 component - silicone).

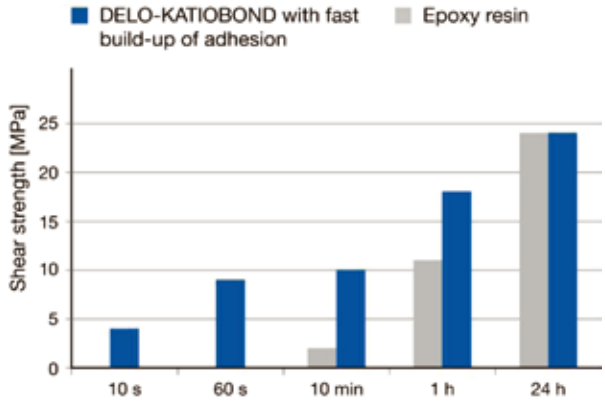

Figure 8.
Time of reaching initial shear strength after UV exposure, compared to standard UV curing epoxy

c. Low Outgasing and Low Shrinkage

Another important parameter in optics applications is the outgasing of the adhesive at high temperatures. Looking at process temperatures up to 260°C, one can see, that the weight loss of the DELO KATIOBOND AD VE 18499 is < 2% @ 260°C.

The shrinkage was measured at 3 positions on a wafer during the imprint process. Thickness shrinkage was <1.5% (Table 1).

d. Reliability Testing

Optical stability
Transmission measurements were done on 100µm thick foils of cured adhesive with no protection.

The foils were analyzed after:
a. 168h Xenon Solar Light exposure
b. 2min @ 270°C (Reflow Simulation)
c. 168 h 85°C/ 85% r.H.
d. 168h 125°

As can be seen on Figure 9, an optical transmission of larger than 80% over the visible range (400nm – 750nm) was achieved for all the conditions tested.

Thermal stability
In order to simulate the mechanical stress in a wafer level optics module, 2 different samples (A, B) were tested:

A: 20mm x 20mm x 5mm glass plates with a 500µm adhesive layer

B: 4mm x 4mm x 4mm glass cubes with a 100µm adhesive layer
Stress on both samples was introduced by a grinding process to simulate the sawing process and to generate possible micro cracks at the edges of the sample.

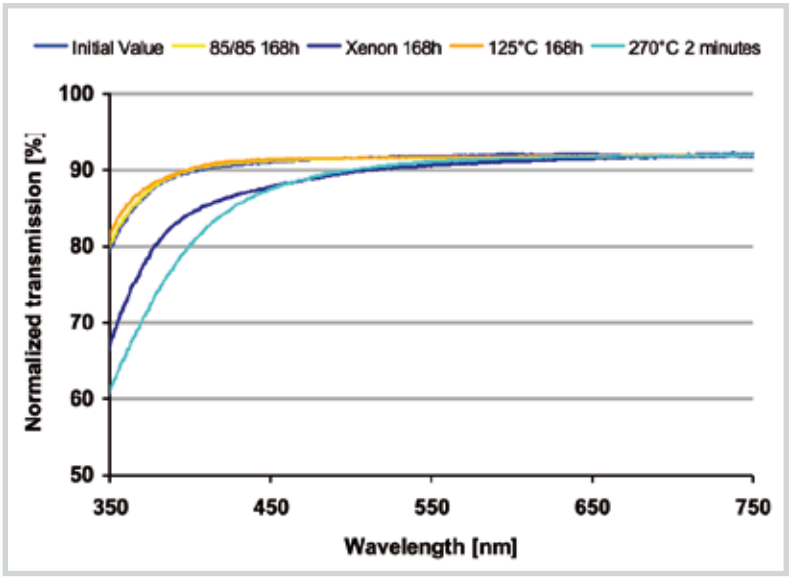

Figure 9:
Transmission of 100µm thick foils of DELO KATIOBOND AD VE 18499

- **Samples A were tested after 500h 85°C/ 85% r.H.**
  The optimized DELO adhesive did not show any delamination, in contrast to some of the standard adhesives.

- **Samples B were run through the following conditions:**

  Temperature shock test: -40°C - -85°C
  The left picture in figure 10 shows delamination of the standard adhesive at the edge of the sample. The right picture in figure 10 shows optimized adhesive, where no delamination occurs.

  Reflow Condition
  A typical reflow profile was simulated in a temperature controlled chamber. None of the samples did show delamination.

Characterization of Micro Lenses (Master, Silicon Stamp and Replicated Lens)

For the measurement of surface deviations the Twyman-Green Interferometer is best suited (Prof. J. Schwider, University Erlangen). The light of a partially coherent source is used to illuminate the interferometer. The deviation of the reflected beam in the test arm (condenser objective/spherical surface) from a plane wave provides the information on the deviations from the sphericity of the micro surface.

Besides of the measurement of surface deviations the radius of curvature of a micro sphere can be determined with the help of this interferometer (= difference between basic position and cat's eye position).

The just described interferometer was used to compare the shape of master, stamp and replicated micro lenses. For the fabrication of the stamp and the replicated lenses the new Mask Aligner MA/BA8 Gen3 from SUSS MicroTec was used. The replicated lenses were fabricated in UV curing adhesives from DELO. Table 1 shows measurement values (radius of curvature, deviation from ideal sphere) over 5 points of a 4

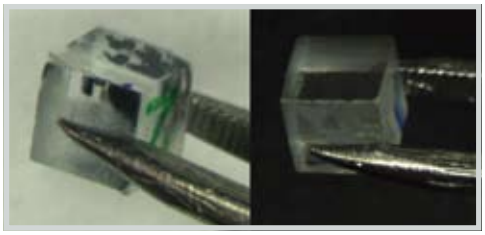

Figure 10.
Images after 300 temperature shock cycles.

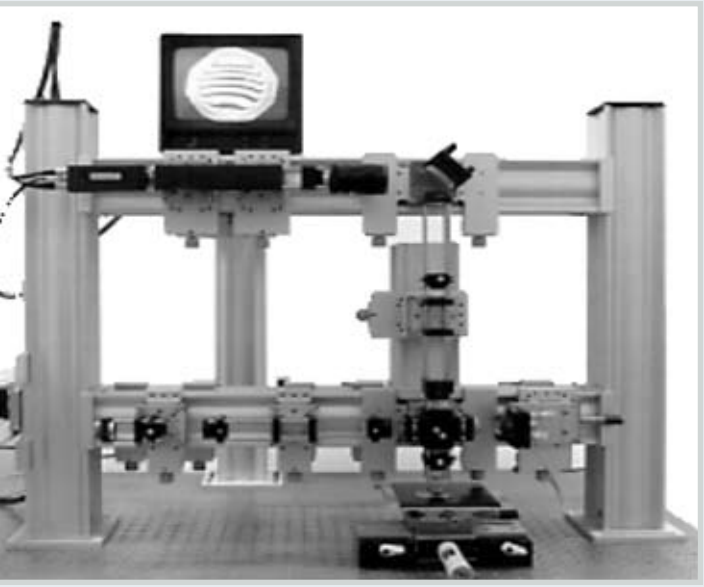

Figure 11:
Twyman-Green Interferometer for measuring surface deviations and radius of curvature.

[µm]	Before UV Cure	After UV Cure	Shrinkage
Left	250	246,5	1,4%
Right	250	246,8	1,3%
Top	250	246,6	1,4%

Table 1.
Thickness change at Curing of DELO KATIOBOND AD VE 18499

inch wafer (centre, right, bottom, left and top) and gives an idea about the very good uniformity which was achieved.

CONCLUSION

In this paper novel fabrication and packaging technologies were introduced. Some required equipment characteristics were introduced, which are beneficial for processes in creating wafer level cameras, like the in-situ alignment and UV-bonding in one tool. UV curable materials for microlens replication and for Wafer Level Packaging of Opto Wafers were presented with their attainable parameters. The developed new materials are showing very good optical and mechanical reliability, as well as excellent reflow behavior. Therefore they were selected for further testing for the imprint processes. Finally characterization of micro lenses was discussed and measurement values of master, stamp and replicated wafer were shown.

A special thanks goes to DELO Industrial Adhesives for providing adhesive and imprint material to realize all tests.

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Margarete Zoberbier, Business Development Manager, SUSS MicroTec

Margarete Zoberbier, started at SUSS MicroTec in 2001 as Application Engineer Bonder, responsible for development and improvement of bonding processes. After being responsible for the Bonder Business Development in Europe, Margarete moved to the Business Development Group of 3D integration in 2008. Margarete co-authored several papers in wafer bonding and related areas. Zoberbier received a Master degree in Precision- and Microengineering field from Georg Simon Ohm University of Applied Sciences in Nuremberg, Germany.

Andreas Kraft, Business Development Manager, DELO Industrial Adhesives

Andreas Kraft got his master's degree in physics at the Universtiy of Ulm, Germany, in 1991. After several positions at Nikon Precision Europe, last as Assistant General Manager as well as Imaging Specialist and Business Developer at Cadence Design Systems, he worked for Suss Microtec as Application Department Manager. Andreas Kraft joined DELO Industrial Adhesives in 2008 as Business Development Manager for the Semiconductor Industry.

Wafer-Level RF Calibration Fundamentals and the New IZI Probe® Technology

Steffen Schott, RF Product Manager, SUSS MicroTec Test Systems

MAKING THE TEST SETUP INVISIBLE

Testing and characterizing all types of high frequency (HF) devices requires a specially designed measurement setup consisting of a vector network analyzer (VNA), a wafer probe system, HF probes, special HF cables, calibration substrates and calibration software.

Systematic error is one of the largest factors reducing measurement accuracy. The sources of this error include cables, connectors, wafer probes, and internal components of the VNA. However, systematic error is highly repeatable if the setup remains constant, and can be defined by the calibration procedure. Once identified, systematic error is excluded from final measurement results, making the test setup "invisible".

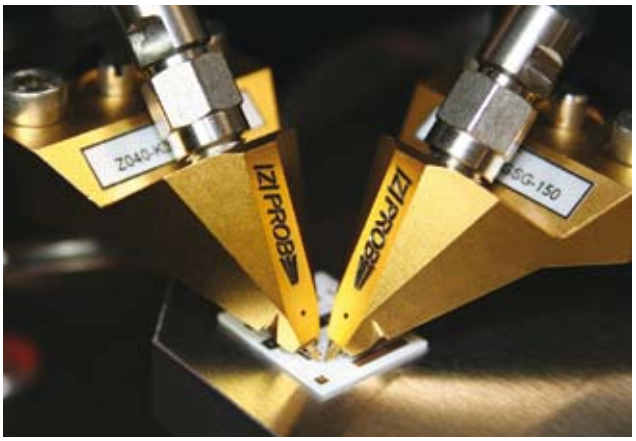
WAFER-LEVEL CALIBRATION STANDARDS

Wafer-level calibration standards are typically fabricated on alumina substrates and grouped into two different types: reflection and transmission standards. Reflection standards are placed in pairs and generally made of gold short-circuits ("Short"), gold open pads ("Open") and gold plus thin-film resistors ("Load" or "Match"). The transmission standards ("Thru" or "Line") usually consist of metal strips in a coplanar configuration. Ideally, Open and Short represent full reflection with 0 and 180 degree phase shift respectively. The Load standard is a 50 Ohm pure resistive element providing a full impedance match. Transmission standards are lossless with 50 Ohm characteristic impedance.

Best results are achieved when using the calibration substrate that

1 MX™ Technology enhances the established IZI Probe® Technology

SOLR Calibration



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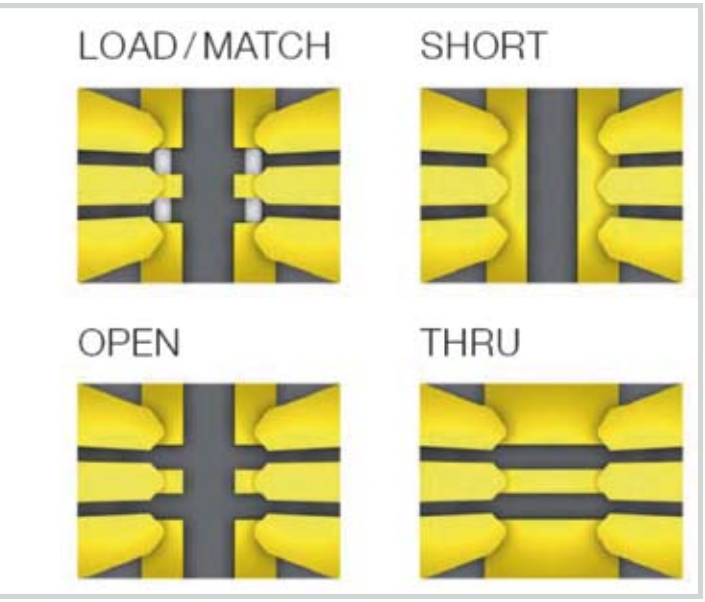


fits to the probes in use, since the standards are designed to ensure the best possible calibration accuracy. Sometimes it is necessary to produce a customized set of calibration standards on the wafer itself, referred to as a test chip. Due to the production cycle of the wafer, these standards are less accurate, and pairs often have different (asymmetrical) values.

Whether on the substrate or on the wafer, calibration standards are never ideal, especially at higher frequencies. Therefore, the standards must be electrically described using a lumped or a distributed elements model. The parameters of the model are referred to as the Cal Kit definition, and must be taken into consideration when setting up the calibration. Normally, the parameters must be entered by hand into the VNA, but a more comfortable and quicker option is to use SussCal® calibration software, which automatically sets the correct values.

There are many calibration methods for wafer-level measurements. Some require ideal or fully-defined standards, whereas others do not. The latter are referred to as advanced self-calibrations. Here are four of the most common calibration methods:

SOLT (Short-Open-Load-Thru) was the first widely-used approach. It is not an advanced self-calibration, and thus requires ideal or fully-defined standards. This is very difficult to achieve for highly-reflective standards (Open, Short) at higher frequencies, thus rendering SOLT impractical for measurements above 20 GHz.

SOLR (Short-Open-Load-Reciprocal) does not require the complete knowledge of the thru standard. In fact, any passive two-port element providing symmetrical (forward/reverse) insertion loss ("Reciprocal") can be used for the calibration instead of Thru, which is useful for setups where use of the Thru is impractical. However, all reflection standards should be fully defined, like SOLT, limiting calibration accuracy to 20 GHz.

The TRL (Thru-Reflect-Line) calibration is not sensitive to the uncertainty of highly-reflective standards. However, the accuracy of the TRL depends on the quality of the transmission standards. Dispersion, skin effects, losses and fabrication tolerances of planar lines as well as requirements for multiple lines and probe repositioning significantly reduce the application and the frequency range of TRL. SUSS MicroTec therefore does not recommend this calibration method for common on-wafer applications.

LRM (Line-Reflect-Match) was developed to overcome the limitations of the TRL calibration. Instead of using a set of different lines, the lumped Match (Load) element is used for calibration. However, good calibration accuracy can be guaranteed only if using purely resistive, highly symmetrical 50 Ohm Loads, which is impossible to fabricate at wafer level. Therefore, the accuracy of LRM significantly decreases as in-pair asymmetry of the Load standard and measurement frequency increase.

The best calibration accuracy without frequency limitation is only achieved with LRM+™ (Line-Reflect-Match extended), an advanced self-calibration. LRM+ defines the measurement system reference impedance for each port individually. Therefore asymmetrical setups can be accurately calibrated with LRM+. This also applies to calibration with test chips, since LRM+ is the only calibration method that does not assume that Load pairs have identical values. Additionally, LRM+ calibrates the system to the DUT, including parasitic influences from contact pads, which means pad de-embedding is no longer required.

The accuracy of LRM+ has been verified using independent standards from NIST. Over a frequency from DC to 110 GHz, LRM+ consistently outperformed all other methods available. LRM+ is only available in SussCal calibration software.

NEW! |Z| PROBE® 1 MX™ TECHNOLOGY!

The patented |**Z**| Probe® Technology, a revolution in RF probe design, makes RF and microwave probing as easy as DC probing. The innovative design ensures that all force applied to the |**Z**| Probe is transferred directly to the contacts. This results in superior handling and contact reliability, minimizing overtravel and damage to the DUT. In addition, the design of the |**Z**| Probe means that SUSS guarantees over 1,000,000 contact cycles – the longest lifetime of any RF probe.

The coplanar line of the |**Z**| Probe is MEMS machined, using the same lithography techniques that SUSS pioneered. It is perfectly symmetrical for ultimate impedance control. The transition from the coaxial cable occurs within the probe body – an air-isolated and controlled environment. This increases the integrity of the signal as well as adding to the impedance control properties of the probe. As a result, contact, stability, repeatability and resistance are all optimized.

1MX™ (pronounced “one-max”) is an improvement on the proven |**Z**| Probe Technology. It is the result of product development done with HF simulations, high tech miniaturisation tools and the latest MEMS technologies.

The improvement, based on a significant miniaturisation of the CPW (coplanar waveguide) structure, leads to higher bandwidth capability and better electrical performance while keeping the unique |**Z**| probes advantages like robustness, contact quality, repeatability and a lifetime of one million touchdowns.

The new 67 GHz provides lower crosstalk and insertion loss as competitive coaxial and thin film RF wafer probes.

“Crosstalk” or “isolation” is the unwanted signal that is transmitted between non-connected probes and “insertion loss” characterizes the loss of signal power resulting from the insertion of a device in a transmission direction.

The improved CPW style with full air isolation makes the 1MX |**Z**| Probe the ideal RF probe for S-parameter measurements at different temperatures from 4K up to 300°C.

1MX is optimized for probes up to 500µm pitch and comes with reduced footprint contact structure compared to the standard |**Z**| probes. The reduced footprint contact structure enables 50µm fine pitch probing with less over travel and therefore less probe force on the pad and less pad damage.

The 1MX |**Z**| Probe is now available for GSG, GS, SG, SGS, GSSG and GSGSG footprints.

SUSS has also extended this technology with the Dual |**Z**| Probe and Multi |**Z**| Probe for probing differential and multiport devices. The precise contact symmetry of the probes ensures accurate results with the least amount of signal distortion and crosstalk.

|**Z**| Probes can be integrated into the |**Z**| Probe Card, the only RF probe card with |**Z**| Probe Technology. It is completely repairable – the probes can be individually removed and replaced. The |**Z**| Probe Card also carries the same long-life guarantee for low cost of ownership.

For mixed RF and DC signal testing, the Multi |**Z**| Probe can be configured to test both signals. Alternatively, SUSS offers the HF ProbeWedge™, which uses the same design principles to eliminate lengthy system changeovers and repositioning of manipulators.

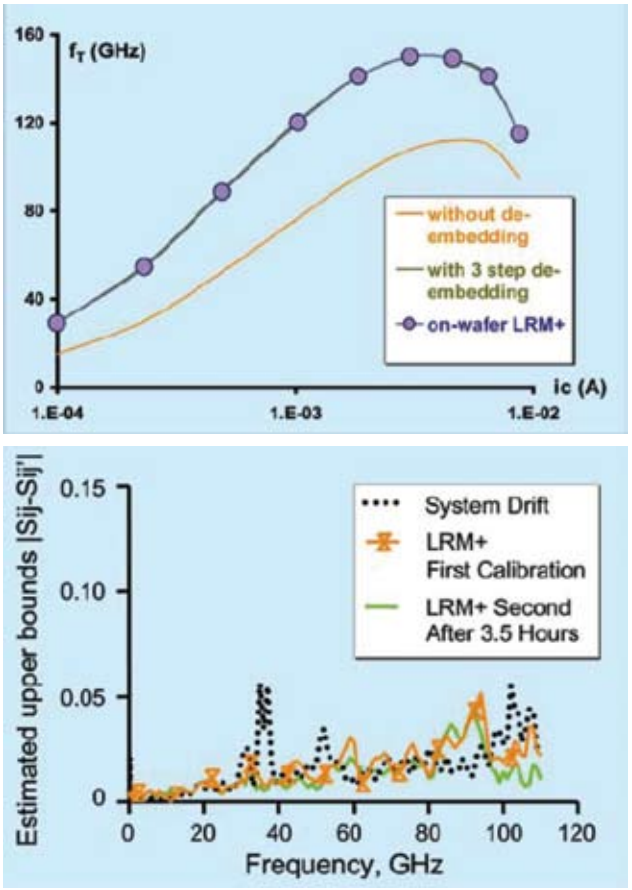
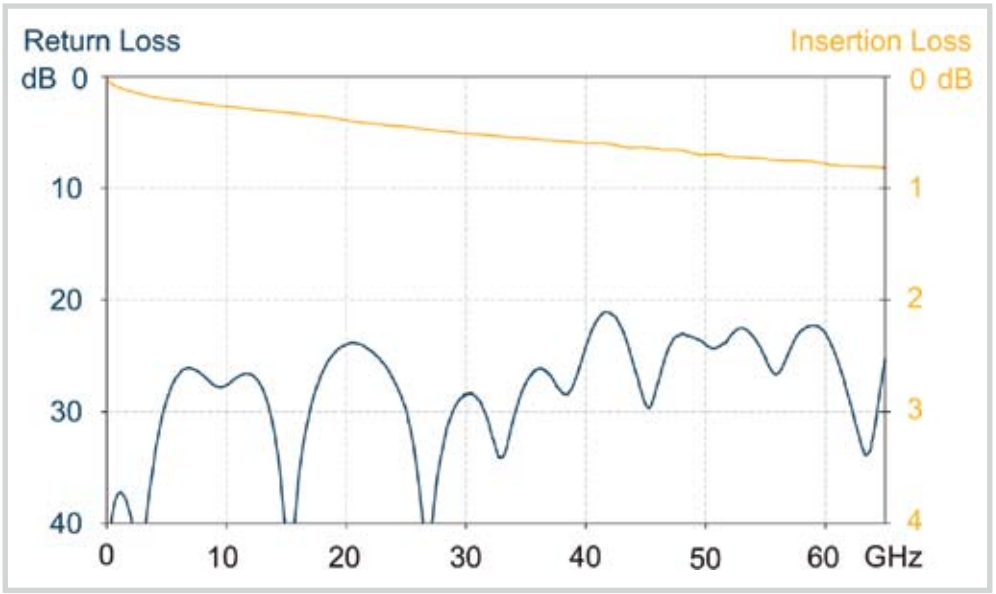


Figure 2: Lower crosstalk and insertion loss with 1MX™ Technology



STEFFEN SCHOTT

is the RF Product Manager for SUSS MicroTec Test Systems, Germany. He holds an engineering degree in sensors and measurements from the Technical University Ilmenau.
After graduation, he spent 6 years developing test systems, sensors and automated production processes before moving into technical sales and marketing. Since 2001 Steffen Schott has been responsible for the strategic development of the SUSS RF probe equipment.

Metal-based wafer level packaging

by Shari Farrens, Ph.D., SUSS MicroTec, Waterbury Center, VT, USA

Metal-based wafer bonding for WLP has several advantages, including enhanced hermeticity and the facilitation of vertical integration. These advantages allow for reduction in die size and cost savings with improved device performance. Until recently, first level packaging for MEMS was done using glass frit or anodic bond process. The glass based bonding methods are used in over 80% of volume MEMS production for high volume products such as pressure sensors, accelerometers and gyroscopes. All of these products, as well as RF resonators, require vacuum packaging. The physical properties of glass and frit sealing materials translate into seal geometries that are in the range of 100s of microns.

Using advanced bonding and bond alignment equipment, in combination with metal bonding methods, significant improvements in COO and device performance can be realized.

INTRODUCTION

The permeability rate of a material is a rate at which gas atoms diffuse through a material. Permeation rates can be compared for materials of equal thickness and under standardized atmospheres. Figure 1 shows this type of analysis for generalized categories of sealing materials; polymers, glass and metals. By definition, materials with less than one day of sealing capacity (1e-14 gm/cm-s-Torr) are considered Non-Hermetic, as indicated by the red line[1].

If a comparison is made between the glass seal and a metal seal, both 10 µm thick, the lifetime of the seal is a few years versus a century or more. The metal seals used for MEMS packaging have seal geometries of 1-2 µm and could conceivably be reduced to less than 1 µm if mechanical integrity (strength) could be ensured.

The combination of improved hermeticity and smaller seal rings enables significant die size reduction. With reduced die size, the number

of die per wafer increases as does the yield, all contributing to cost reductions. Table 1 compares the area savings when the sealing geometry is reduced. The table assumes a constant dicing street size of 75 microns. Using this type of analysis, a 9 mm^2 die that was formerly sealed by a glass-based technology, can be replaced with a 2-3 µm wide metal seal, and several hundred more die can be placed on the same sized wafer.

The two types of metal seals available for wafer level bonding are diffusion-based and eutectic. Both of these fabrication methods have numerous benefits and can be successful replacements for traditional packaging techniques.

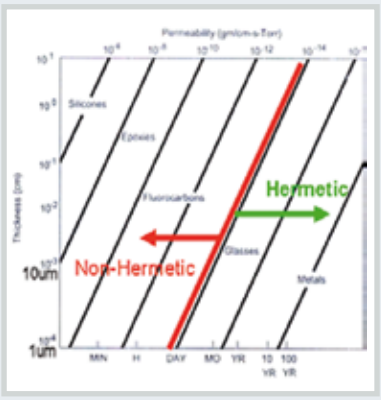


Figure 1.
The Permeability of materials as a function of the thickness of the material. Highlighted arrows compare metal and glass lifetimes.

DIFFUSION BONDING

Diffusion bonding is when two metals are pressed together under applied force and heat, which enables atoms to migrate from lattice site to lattice site, "stitching" the interface together. Diffusion processes require intimate contact between the surfaces, since the atoms move by lattice vibration. Generally speaking, softer metals, such as copper or aluminum, are excellent choices for diffusion bonding due to their ductile properties and rapid diffusion rates. Gold is another excellent candidate and can be used at lower temperatures than the other options.

Die size (mm x mm)	3	5	7	10
Effective die area w/50 µm seals	10.1	26.8	51.5	103.5
Effective die area w/25 µm seals	9.8	26.3	50.8	102.5
Effective die area w/10 µm seals	9.6	26.0	50.3	101.9
Max added die/wafer (100 µm > 50 µm)	187	44	17	6
Max added die/wafer (50 µm > 25 µm)	101	23	9	3
Max added die/wafer (25 µm > 10 µm)	63	14	5	2

Table 1.
Comparison of effective die size and number of additional die added when seal geometry area is reduced.

Diffusion rates vary dramatically depending upon the reaction path. Surface diffusion is diffusion along the terraces of a surface. Since there are no atomically flat surfaces on MEMS wafers, the atoms will move from surface site to surface site to reduce the terracing and free energy. This is the most rapid diffusion process, since the atomic motion occurs relatively unimpeded.

Grain boundary diffusion is the next most rapid reaction pathway. Since most deposited layers are polycrystalline, there are numerous boundaries between the grains in which 1:1 atomic lattice matching is incomplete. This leaves empty space in which the atoms can migrate freely.

Diffusion through the bulk of the crystal is the slowest of the three mechanisms. Exchange of atoms or vacancies within the lattice enables the mixing to occur. The onset of bulk diffusion is typically 1/3 to 1/2 of the melting point of the material and increases exponentially with temperature in a Arrhenius relation[2]. However, oxidation and impurities in the metal films also play a significant role in diffusion reactions and generally reduce the diffusion rates significantly. Thus manufacturing techniques need to include clean deposition practices, and bonding using surface oxide removal and re-oxidation prevention are recommended.

Table 2 gives the recommended processing ranges for the three leading metaldiffusion bonding techniques. Aluminum bonding is generally not pure aluminum but rather the metallization alloy used in the fab, which includes up to 4% Cu or other binary additions. Both aluminum and copper bonding require temperatures above 400˚C to achieve a good hermetically sealed interface. Aluminum also requires a large applied force, which is apparently needed to crack the surface oxide that spontaneously forms on any aluminum surface. The surface oxide of aluminum is not soluble in the matrix (<2e-8 wt%) and tracer studies have proven that aluminum does not penetrate the oxide[3,4]. Rather, oxygen from the surface diffuses through the Al_2O_3 layer to provide the source of additional oxygen until the surface is fully passivated. However, the surface oxide can be cracked, and bonding can be completed by using a high applied force.

Gold diffusion is the lowest temperature process of the three and is successfully managed at temperatures

Table 2.
Typical processing parameters for metal diffusion bonding.

Metal	Temperature	Applied Force Range†	Time	Atmosphere
Al	400-450˚C	>70 KN	20-45 min	Vac or H_2/N_2
Au	350-450˚C	>40 KN	20-45 min	Vac or H_2/N_2
Cu	380-450˚C	>30 KN	20-60 min	Vac or H_2/N_2

†Applied force depends on wafer diameter and pattern density. Table values are representative of 200 mm wafers.

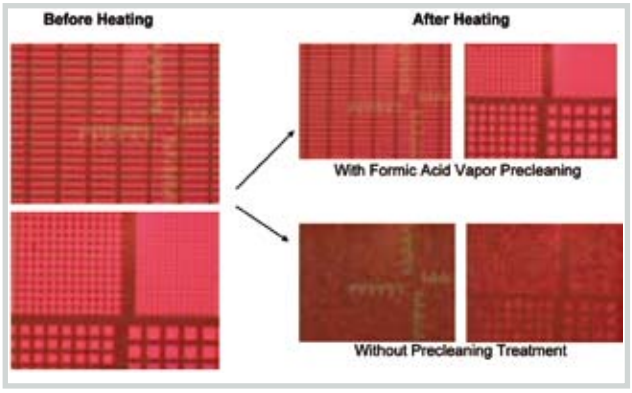


Figure 2.
Images on the right are the wafer as received. The wafer was then heated in a bonding chamber to 450˚C for 30 minutes. Right upper images were cleaned with formic acid cleaning prior to heating and the right lower wafer was not cleaned.

as low as 380°C. Unlike copper and aluminum, gold does not readily form an oxide and under normal processing conditions; it is not necessary to use surface cleaning prior to bonding.

Copper, on the other hand, readily forms a surface oxide. The oxide can be successfully removed and the surface passivated by the use of formic acid vapor cleaning. Vapor cleaning with formic acid is used in 3D vertical integration to ensure high conductivity of interconnects[5]. The vapor cleaning is demonstrated in Figure 2. A patterned copper wafer was exposed to elevated temperatures with and without the formic acid cleaning. The cleaned wafers were able to withstand post cleaning exposures to high temperature in the bonder and subsequently showed improved electrical performance.

EUTECTIC BONDING

The other major category of metal-based bonding used in MEMS packaging is the eutectic bond. A eutectic alloy is sometimes called a "solder;" however this is not necessary the correct metallurgical term.

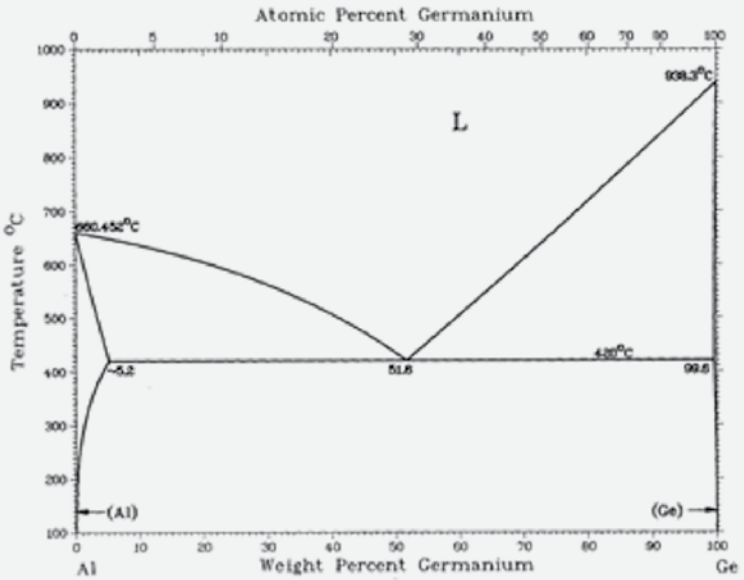


Figure 3. Aluminum–germanium phase diagram showing simple eutectic reaction at 56.1wt% Ge and at 420°C.

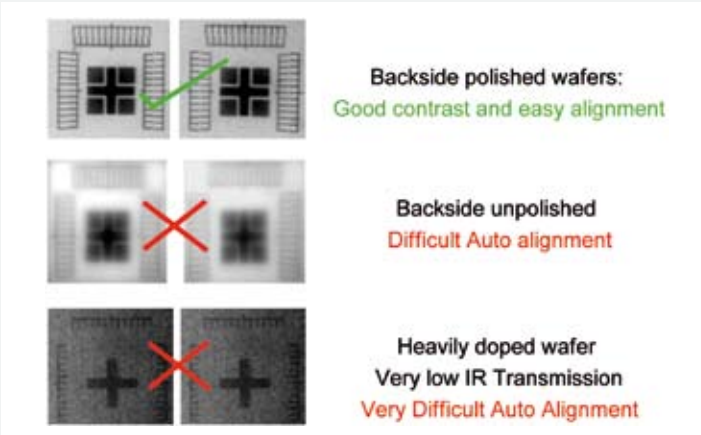


Figure 4. Image degradation from sample effects.

A eutectic alloy is a two-component alloy that undergoes a direct solid to liquid phase temperature at a specific composition and temperature.

The composition and temperature define the reaction and are unique to only a few materials systems. Table 3 shows the alloys most often used for wafer level bonding. The choices are alloys of gold, aluminum or copper, since these materials are already used in semiconductor fabrication labs and in most cases have established processing and deposition methods. The most common choice is the gold- tin system with interest in other alloys fairly evenly distributed.

Choosing the correct eutectic alloy for an application is most often determined by the processing temperature and compatibility of the materials with the existing manufacturing flow. In addition to alloy selection, it is equally important to determine the method of eutectic alloy formation.

Eutectic alloys have several advantages over the diffusion processes, including lower processing temperatures and reflow. The reflow process enables the interface to self-planarize

Table 3.
Eutectic alloy commonly used in MEMS wafer level packaging.

Eutectic Alloy	Eutectic Composition	Eutectic Temperature
Al-Ge	49/51 wt%	419˚C
Au-Ge	28/72 wt%	361˚C
Au-In	0.6/99.4 wt%	156˚C
Al-Si	97.1/2.9 wt%	363˚C
Au-Sn	80/20 wt%	280˚C
Cu-Sn	5/95 wt%	231˚C

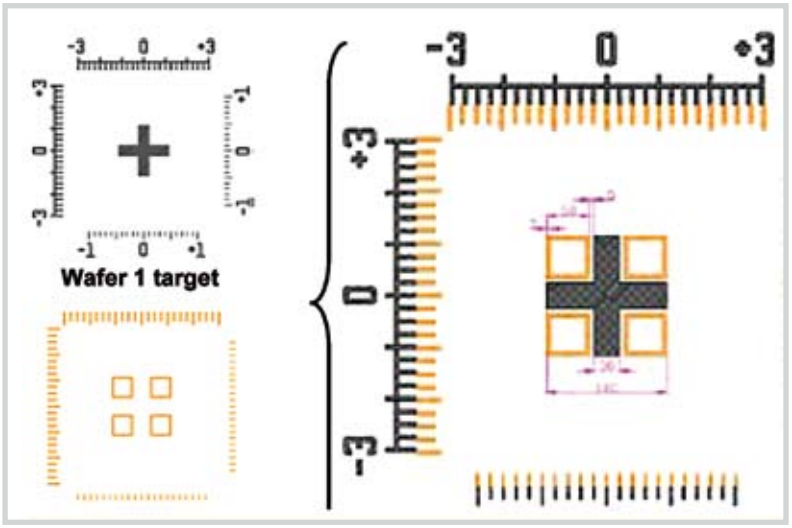


Figure 5. Suggested male and female targets for IR or ISA alignment. Note dual scale verniers provide either 0.25µm or 0.1µm resolution.

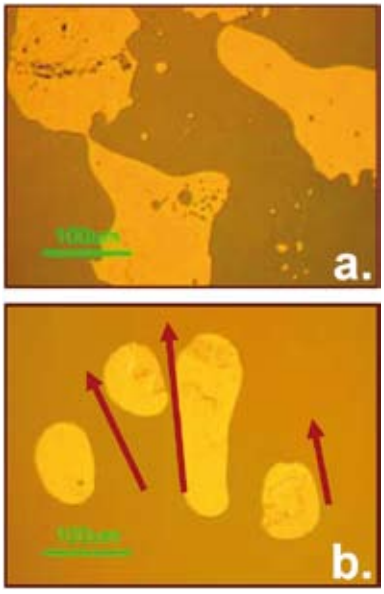


Figure 6.
a) Bubbles formed in the eutectic alloy due to overheating;
b) smearing of the eutectic alloy in the direction of non-parallel force application.

and minimize the effects of surface topography or less-than-ideal CMP (chemical mechanical polishing) steps. However, the reflow must be controlled through proper thermal and force application in the bonder.

Figure 3 is the Al-Ge phase diagram[6]. This is a simple eutectic phase diagram with no intermetallic phase formation. The aluminum has a melting point of 660˚C, and germanium melts at 938˚C. The eutectic reaction is at 51.6 wt% Ge and has a solid to liquid transition (eutectic point) at 420˚C. In most eutectic bonding applications, the rule of thumb is to remain at 7-15˚C above the eutectic temperature. Going to higher temperatures will increase the fluidity of the alloy and can lead to excess flow into unwanted regions in the die. However, if the temperature is not uniform, the viscosity of the melt will vary. Some areas on the wafer may be solid and others liquid, and the wafers will crack under the applied force as bending moments develop in regions with varying compliance.

The next decision that must be made for a eutectic bond is whether or not the bond will be done by melting the alloy or by a combination of diffusing pure materials together in the solid state to reach the eutectic composition and then melting the alloy. If the alloy, for example 51.6 wt% Ge, can be deposited as an alloy layer on both sides of the interface, then the wafers are simply aligned, brought into contact and pressed together. After contact is established, the wafers are heated to the eutectic temperature, melted and re-solidified. Alloys can be deposited by sputtering of alloy targets or electroplated in some but not necessarily all cases. The advantage of the direct melting of alloy layers is speed because the diffusion step can be avoided.

Alternatively, the aluminum can be deposited on one wafer and the germanium on the other substrate. Then the wafers are pressed together and heated (below 420˚C) until the interface mixes. Note that limited solid solubility means that the diffusion is only a few percent, and grain boundary reactions will play a major role in the success or failure of the bonds when completed with this strategy. After mixing the material, the wafers are reflowed and cooled.

After eutectic bonds are cooled, there is a possibility that microvoids form in the eutectic microstructure. These voids may be due to the Kirkendall effect, which occurs when one element diffuses more quickly than the other and the lattice sites left behind are empty[7]. Or, rather, they are filled with vacancies. If a substantial vacancy concentration exists, then the vacancies can cluster and lead to microvoiding. In most cases this can be overcome by adjusting the cooling rates and the amount of hyper eutectic heating.

ALIGNMENT

Alignment accuracy is affected by the quality of the alignment keys, the method of imaging used during wafer-to-wafer alignment and the thermal response of the wafers during heating and bonding. There are three primary alignment methods used for metal bonding. These are BSA (backside alignment), ISA (inter-substrate face-to-face alignment), and IR (infrared) alignment. In general, metal bonding provides a huge benefit over other types of bonds whenever the fiducials can be defined with the metal layers. The sharp contrast between the metal and semiconducting layers provides excellent human or automated image resolution.

Backside polished wafers are recommended for BSA alignment and usually required for IR alignment. IR alignment has the additional advantage that for samples that are IR transparent (resistivity levels >0.01 Ohm-cm) and have no metal surrounding the alignment keys, the IR imaging method can be used for post-bond overlay accuracy assessment and inline metrology during full automated production[8]. Figure 4

Table 4. Au to Au alignment accuracy, post bond.

	ALIGNMENT SHIFT X-AXIS AND Y-AXIS IN THREE LOCATIONS							
	X1	Y1	X2	Y2	X3	Y3	X misalign (µm)	Y misalign (µm)
	-0.03	0.02	-0.08	0.07	-0.10	0.10	1.25	-1.85
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.80	-0.90
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.50	-1.75
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.95	-1.05
	-0.03	0.02	-0.08	0.07	-0.10	0.10	1.70	-2.15
	-0.03	0.02	-0.08	0.07	-0.10	0.10	1.85	-2.40
	-0.03	0.03	-0.08	0.08	-0.10	0.10	1.60	2.25
	-0.02	0.03	-0.07	0.07	-0.10	0.10	-1.20	0.30
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.55	-1.75
Average	-0.03	0.02	-0.08	0.07	-0.10	0.10	1.25	-1.85

shows the degradation that occurs in IR imaging when the wafers are too highly doped or do not have a polished backside on at least one of the wafers.

Alignment key recommendations exist for all the types of imaging conditions. In addition, it is very useful to consider the use of verniers in the alignment key as a method of quantifying lot to lot variations. Figure 5 shows an alignment key with graduated lines used to assess the post bond alignment shifts. Fast, calibrated assessments of final overlay accuracy allow for rapid feedback and process development improvements.

One of the key benefits of post-bond alignment checks is that the alignment can be checked for each wafer pair. Thus when production tools are running unattended, the cluster tool can make use of the rapid speed of the alignment module relative to the rate at which the bonder can complete a full metal bond thermal treatment. The master recipe or path is defined such that when the bonds are completed in the bond module, the wafers can return to the aligner, and a post-overlay image is taken. If the accuracy is within the tolerances set by the recipe, then the bond chamber is loaded with the next aligned pair. If the accuracy is not within specification the operator is notified to remedy the situation. The frequency of the checks can be selected to match the product necessities.

Both metal diffusion and metal eutectic bonds are capable of achieving <5 µm post-bond alignment accuracy. The metal diffusion bonds are affected by thermal expansion difference between top and bottom wafers if the upper and lower heat sources are not consistent with one another. In eutectic bonding, the major contributor to post-bond alignment accuracy is the shifting that may occur if the applied force or other mechanical systems in the bonder do not prevent the two wafers from sliding on the liquid interface. Currently, metal diffusion bonding with Cu has be proven as a 1-2 µm process with ability to achieve <1 µm alignment accuracy in well-defined 3D integration applications. MEMS bonding with eutectic bonds is usually a 2-3 µm process.

EQUIPMENT

The sensitivity of the metal bonds to uniform temperature and force applications has led to improvements in wafer-level bonding equipment. Improvements in materials and design have led to bonders such as the SUSS MicroTec CB8 (or CB200 and CB300 in 200 mm and 300 mm cluster tools) and have led to temperature uniformity levels with <1% difference within wafer or between upper and lower heaters. The force uniformity in advanced bonders is now 5% and results from the fact that in these

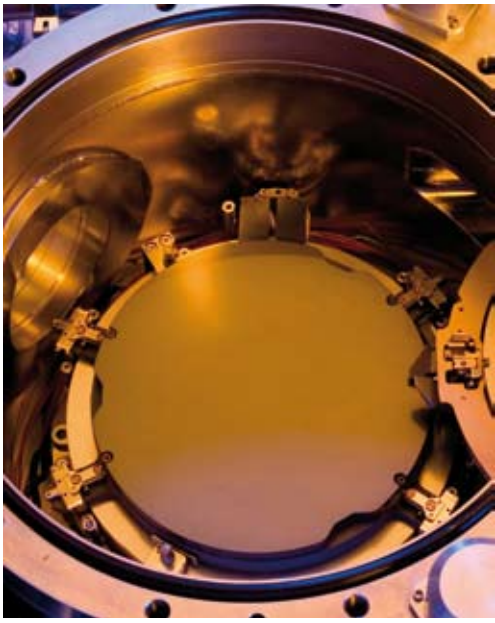


Figure 7. SUSS MicroTec CB8 wafer bonder with WEC (wedge error compensation) to ensure parallelism between pressure plates for all bonds.

Sample #	POST BOND ALIGNMENT DATA				
	LX	LY	RX	RY	Acc Post
1	-3.0	0.0	-1.5	0.0	2.3
2	-0.5	-2.0	0.0	2.0	2.0
3	-3.5	-0.5	1.5	0.0	1.1
4	0.0	0.5	0.0	0.5	0.5
5	-1.0	-1.0	-0.5	-1.0	1.3
6	-0.5	0.0	0.0	0.0	0.3
7	0.0	-2.0	0.5	0.0	2.0
8	-0.5	-2.0	-0.5	2.0	2.1
9	0.0	0.0	-0.5	-2.0	2.0
10	0.0	-1.5	-0.5	0.0	1.5
Max	0.0	0.5	1.5	2.0	2.3
Min	-3.5	-2.0	-1.5	-2.0	0.3
Avg	-0.9	-0.9	-0.3	0.2	1.5
St Dev	1.3	1.0	0.8	1.2	0.7

Table 5.
Cu to Cu diffusion bonding, post bond alignment results.

bonders the upper and lower pressure plates establish parallelism by a WEC (wedge error compensation) operation before bonding begins. During the WEC operation the lower bond head assembly is floated on a bed on N2 air and allowed to rotate on a spherical bearing. This eliminates any non-parallelism between upper and lower plates and ensures the applied force is perpendicular to the bond interface at all locations.

A study was performed in which a glass wafer and a silicon wafer were bonded using eutectic alloy balls[9]. The balls were placed between the two substrates and put into the bonder. Several parameters were explored including the effect of overheating and non-planar force application.

When the temperature is too high above the eutectic, the alloy has a very low viscosity and flows readily with even the lightest application of force. This can lead to the formation of bubbles at the interface and areas with unwanted metal. Figure 6a is an optical micrograph looking through the upper glass substrate. The unconfined flow is clearly visible and there are numerous bubbles. In Figure 6b, the flow direction is very obvious, and this is a tip off that the bond heads were not parallel to one another as the contact was made.

RESULTS

Gold-to-gold bonding is the lower temperature diffusion bonding method of the three options discussed above. Table 4 is the post bond alignment accuracy of several wafers aligned with face-to-face ISA alignment on the SUSS MicroTec BA200 Gen2 aligner. The wafers were subsequently bonded on the SUSS MicroTec CB8 shown in Figure 7, and measured independently on a freestanding IR microscope. The average overlay accuracy of all wafers measured in three locations each, was +0.89 µm in x and -1.03 µm in y overlay accuracy.

A similar analysis was done with a copper-to-copper bond on 200 mm wafers. These wafers did not have backside polished surfaces, and the IR alignment was compromised as a result. In addition, the additional temperature, approximately 100˚C, would have increased the radial expansion of the wafer by over 50 µm and would have exacerbated any upper and lower heater deviation. Nevertheless the data in Table 5 shows that the post-bond alignment accuracy for copper wafers bonded at 450˚C was an average of 1.5 µm microns, well within needed requirements and specifications.

Figure 8 shows an example of 150 mm successful aluminum diffusion bonding. These wafers were also bonded in the SUSS MicroTec CB8 chamber using 80KN of force at ~400˚C. Both the blanket layers of aluminum as well as the patterned

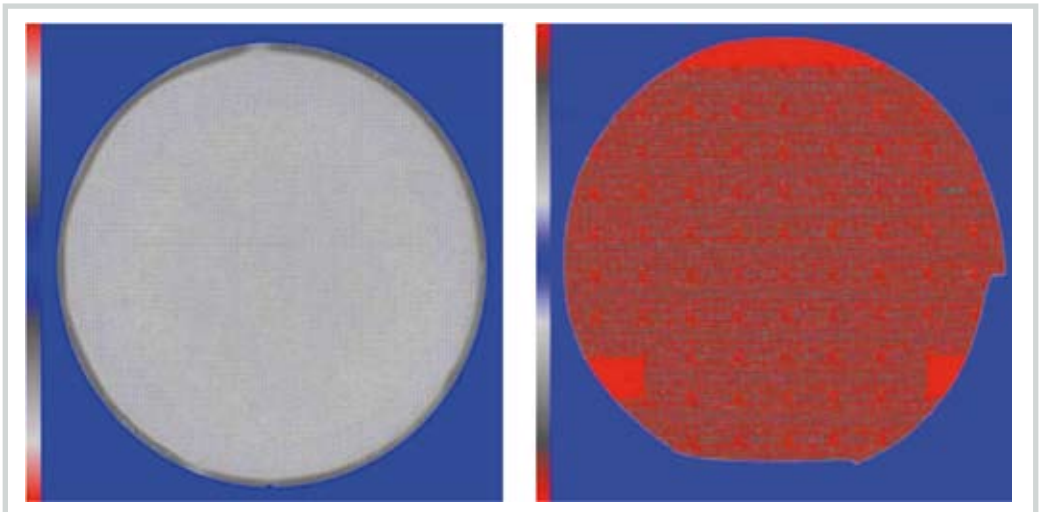


Figure 8.
Left is a blanket layer of aluminum on a 200mm wafer successfully bonding with Al diffusion techniques. On the right is a 150mm device wafer also bonded with aligned Al to Al diffusion methods.

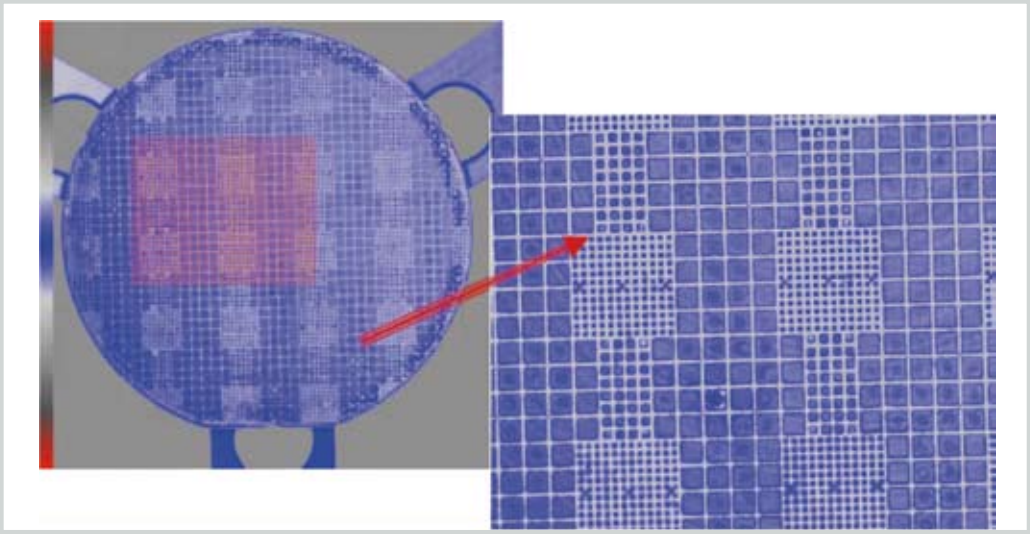


Figure 9.
Au-Sn eutectic bond between silicon and sapphire. Gray areas are the seal rings in this Sonoscan acoustic image.

device wafer structures were successfully bonded in a void free fashion.

The eutectic bonds are used in a variety of applications. The lower temperature processes make these bonds appealing to optical markets such as LEDs. The LED device is grown by epitaxial methods on lattice-matched substrates, such as InP, GaAs or sapphire. The growth substrates are generally removed to access the backside of the device and improve output efficiency and brightness. Bonding is used to attach the LED structure to a lower-cost substrate such as silicon, and the growth substrate is removed by mechanical methods (grind an etch) or by laser lift off[10].In all these process flows, the thermal mismatch between the growth substrate and the silicon is extremely severe. This stress often cracks the epitaxial layers and ruins the device.

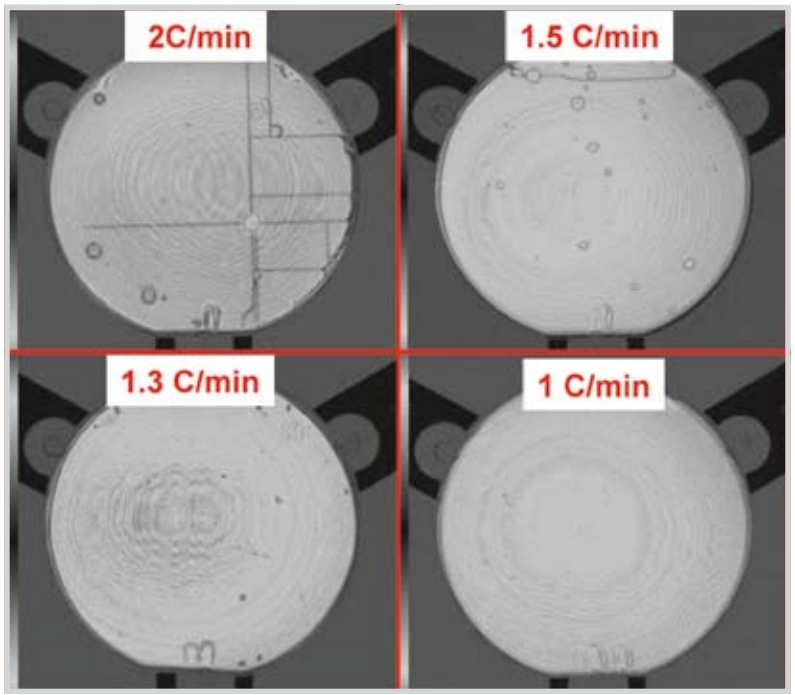
Figure 9 shows the results obtained using an AuSn eutectic alloy to bond silicon to sapphire at 290˚C for 20 minutes. The bonds are void free and the wafers did not crack. The ability to reduce the processing temperatures minimized the time needed to heat and cool the bonder and the sample. The decreased sensitivity to thermal gradients (less CTE mismatch) also enabled faster cooling rates and improved the throughput and COO for this metallurgical choice.

This is in direct contrast to the results shown in Figure 10 for a gold diffusion bond at 380˚C in which the cool-down rates must be extremely slow in order to control the additional stress from the temperature difference between the two metallurgies and expansion differences between the substrate materials. In Figure 10, one can truly see the difference that temperature and heating rate plays in thermal expansion induced stress. The CTE (coefficient of thermal expansion) for Si is 3.2 ppm, compared to 5.32 ppm for GaAs and 8.4 ppm for sapphire. Thus the benefit of the lower temperature process for the AuSn eutectic compared to the Au-Au diffusion process allows the Si to sapphire to be successfully bonded even with the extreme (3.2 vs. 8.4ppm) CTE mismatch.

CONCLUSIONS

Several technologies based on metal bonding methods are available as replacements for glass frit or anodic bonding techniques. The metal bonds are categorized according to the type of metallurgical reactions that are used. These are the diffusion-based processes and the eutectic reactions. The former does not involve reflow and generally requires a higher processing temperature and potentially longer cycle times. The eutectic process enables reflow similar to the glass frit processes and is more forgiving to surface roughness. The choices for eutectic alloys is varied and processing temperatures range from slightly above 150˚C to over 400˚C. Thus it is possible to find a metallurgy that is compatible with materials

Figure 10.
Gold diffusion bonding of Si to GaAs at 300°C for 1 hour. Cooling rate must be extremely slow to prevent the subsurface cracking shown in these acoustic images of the bulk GaAs substrate[11,12].



requirements as well as post bond processing needs like solder packaging. The key motivation for device manufacturers to transition to metal based wafer level bonding is the increased hermeticity which improves device functionality but more importantly enables the continued scaling of the device to smaller sizes. In addition to device scaling the geometry of the sealing rings surrounding the device can be diminished further increasing the number of die per wafer. In closing it is worth noting that while the market growth of products such as accelerometers, gyros and RF MEMS is growing at more than 25% per year through 2011, the ASP (average selling price) is expected to drop by 8-13%[13]. Thus the analysis in Table 1 is very poignant. This table compared, through simple analysis, the number of additional die that can be placed on a wafer by switching from a large seal area typical of glass frit to a smaller metal seal. For example, a 3 mm x 3 mm die size switching from a 100 µm seal to a 10 µm seal enables an additional 363 more die. This does not include any assumptions of die scaling or increases in yield which most companies are beginning to report. Metal bonding is a valuable asset to MEMS wafer level packing. The economic and technological advantages are clear, and these methods will continue to increase in use as markets become more consumer oriented and integration with other components increases.

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Wafer Surface Parameters and Their Significance in Wafer Bonding

Sumant Sood, Senior Applications Engineer for Wafer Bonders at SUSS MicroTec

INTRODUCTION

Wafer bonding is a collection of techniques used to unite two substrates with or without an intermediate layer. Most wafer bonding processes require the two mating substrates to meet incoming flatness and smoothness specifications. At a microscopic scale, no surface appears perfectly smooth. All materials exhibit surface irregularities and bumps. Surface flatness specification is a global/macroscopic concept typically measured over the whole wafer. Smoothness on the other hand is a local microscopic parameter of wafer surface quality. During the bonding process, at least one material surface must deform to fit the other substrate and fulfill the contact conditions necessary for intersubstrate bond formation. This deformation may be accomplished by plastic elastic deformation, or by wetting a surface with a liquid material. This application note will discuss the typical wafer surface parameters of interest and how they affect bonding for the different bond technologies.

Some of the important wafer surface parameters provided for bare Si wafers include roughness (usually RMS roughness or mean roughness), TTV, TIR, Bow, and warp.

Surface micro-roughness measurements are performed on an area of a wafer that is typically 1 µm x 1 µm or 5 µm x 5 µm using atomic force microscopy (AFM). The AFM probe detects minute variations in the electromagnetic forces between itself and the wafer, which is directly proportional to the separation dis-

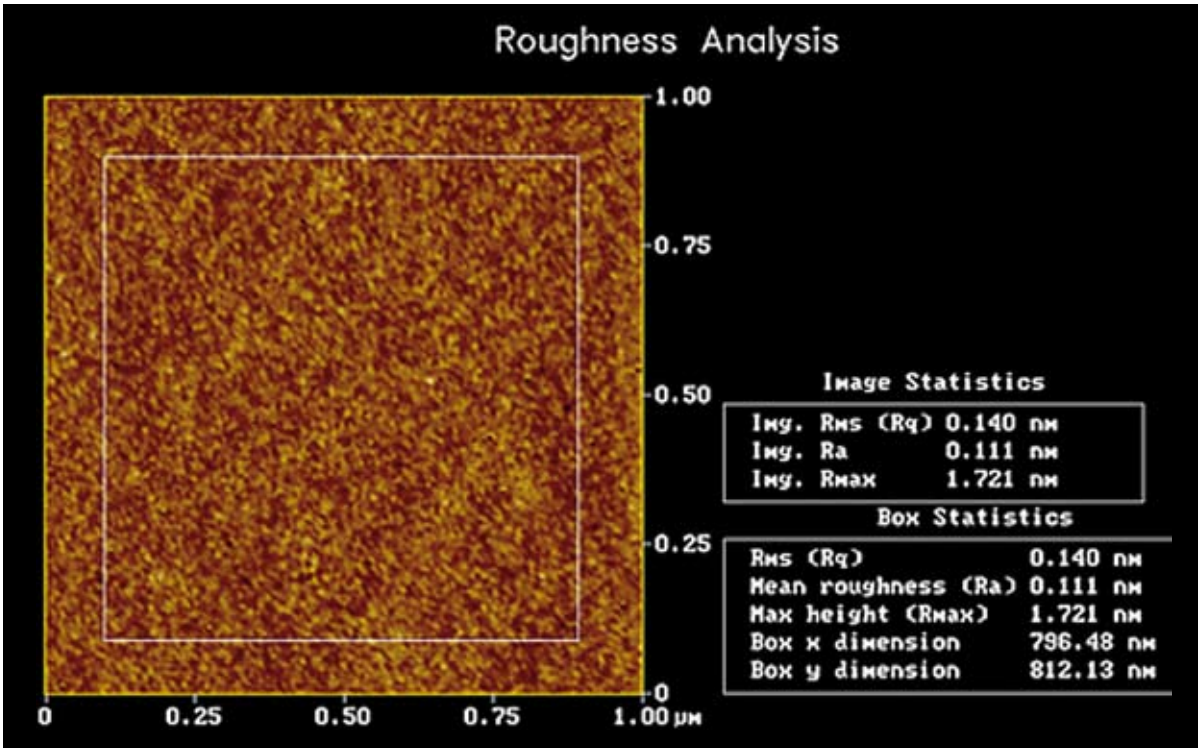

Figure 1:
AFM Micro roughness measurement of a 1 µm by 1um area on a prime grade silicon wafer showing RMS roughness (Rq) of 0.14 µm and mean roughness) 11nm. (Image: Silicon Quest Intl)

Surface parameter	Description	Suggested Values for direct bonding	Typical Values available for Silicon wafers (200 mm dia)[1]	Typical Values available for wafer bond quality Glass (200 mm dia)[2]
Micro Roughness (R_a or R_q)	Roughness of a 1 x 1 µm to 5 x 5 µm area measured using Atomic Force Microscopy	$R_a \leq 1$ nm	$R_a < 0.1$ nm $R_q < 0.2$ nm	$R_a \leq 1$nm
TTV	The difference between the max and min values of thickness during a scan pattern or series of point measurements.	≤ 3 µm	< 1 µm	< 2 µm
Bow	Deviation of the center point of the median surface of a free, unclamped wafer from the median surface reference plane	≤ 30 µm	< 2 µm	± 2.5 µm
Warp	Difference between max and min distances of the median surface of a free, unclamped wafer from a reference plane (takes both concave and convex deviations in account)	≤ 30 µm	< 20 µm	< 70 µm

1 Prime Si wafers, 2 AF 32 Glass

Table I:
Suggested values of common wafer surface parameters for spontaneous wafer bonding and typical available values for 200mm Si and glass substrates

tance between the probe tip and varying surface heights of the wafer. Wafer surface micro-roughness values are critical for direct bonding in which near atomic registration of the surfaces is necessary. For metal bonding the quality of the CMP process is monitored by AFM analysis to ensure that the surfaces can be brought into contact under applied force for the diffusion process. When substrates are not able to meet the exacting specifications of surface flatness for either diffusion or silicon direct bonding the information may lead to the selection of an alternative bonding technology such as a eutectic, polymer or glass frit bond. Typical values of wafer surface parameters required for spontaneous direct bonding (silicon direct/fusion) are shown in Table 1.

Bow and warp measurements are based on the median surface of the wafer relative to a reference plane. Flatness measurements are based on the front (top) surface of the wafer relative to a reference plane. The wafer bow can be a positive or negative number. Positive indicates that the center point of the median surface is above the three point reference plane (convex shape). Negative indicates that the center point of the median surface is below the three point reference plane (concave shape). Bow/warp anomalies in the mating wafers can be mediated by applying sufficient force during bonding to establish contact but are not eliminated. The tolerance of the process to final bow and warp often depends on the device application and post bond processing needs.

Prime silicon wafers coming from a “wafer manufacturer” meet the specification for all wafer bonding types. That said, wafers from a “silicon vendor” and not a manufacturer might be called “Prime wafers” but chances are they have some faults ranging from pits to sub-surface defects. These wafers might be suitable for most MEMS wafer bonding processes (eutectic, adhesive or frit bonds) but are not suitable for SOI bonding. It is therefore critical to understand the exact wafer specs needed for a particular bonding process.

In addition to thermal budget, materials and other requirements, wafer surface parameters play a critical role when selecting an appropriate wafer bonding profess for a particular application. Silicon wafers in a MEMS or semiconductor fab go through multiple processes (oxidation, etching, thin films deposition) prior to the wafer bonding step. Depending on the previous processing steps, the wafer may have surface parameters that would put it outside the range of specs required for some wafer bonding processes. For example, a processed wafer with large bow/warp might not be suitable for Au-Au thermo compression bond but would be suitable for a AuSn eutectic bond process.

THERMAL VS. CVD OXIDES

Micro roughness values for thermally grown thin oxide films is close to that of prime silicon wafers. However, thermal growth of oxide on silicon wafers is a long and high temperature process typically at 1000°C but not lower than 700°C. MEMS and semiconductor manufacturers use CVD processes (LPCVD or PECVD) to form oxides that grow much thicker in relatively short times and at lower temperatures. CVD growth is performed at temperatures less than 450°C. Two major concerns about the use of LPCVD TEOS for

Wafer Description	Mean roughness (nm)	rms roughness (nm)
Bare Si wafer	0.097	0.143
5000 Å SiO_2 /Si	0.202	0.273
4 μm PECVD SiO_2 /SOI (as-prepared)	7.929	9.757
4 μm PECVD SiO_2 /SOI (annealed at 350 °C for 16 h)	6.877	8.501
4 μm PECVD SiO_2 /SOI (annealed at 350 °C for 16 h +3 min CPM)	0.312	0.394

Table II: Direct comparison of Mean and RMS roughness of Si wafers with different surface preparations

direct bonding are the bubble formation at the bonding interface after an annealing above 300°C and the existing surface microroughness. The uneven surface profile of an as-deposited PECVD oxide film limits the amount of surface area that can be in intimate contact with its pairing wafer, which in turn will degrade the quality of the bonding. A pre-bonding heat treatment, so-called densification anneal, is generally used as a solution to the bubble formation problem, resulting in driving-out of the surface water vapor or hydrocarbon species. A final CMP in then used to achieve acceptable surface roughness for direct wafer bonding. CVD processes are also used to deposit silicon nitride and polysilicon over metal layers on substrates for MEMS and mainstream CMOS processes. These process flows use planarization CMP treatments to achieve surface quality suitable for wafer bonding and are a cornerstone of the hybrid bonding technologies used in 3D integration.

WAFER SURFACE REQUIREMENTS FOR METAL AND EUTECTIC BONDS

After direct bonding, diffusion bonding has the second most stringent surface roughness and flatness requirements. It is known that for diffusion bonding, the contact area and bonding energy must be as large as possible. It is therefore important for the two mating metal surfaces to be very smooth and flat to allow for solid state diffusion. The surface roughness of the substrate in addition to its surface cleanliness defines the temperature and the force required for good bonding. It has been demonstrated that the surface roughness affects the bonding quality when the bonding temperature is low. The typical reported micro-roughness values of sputtered Cu (300nm) on Ta (100nm) range from 1.5 to 2nm. Low temperature bonding processes (<300°C) for Cu-Cu bonding have been demonstrated by controlling copper surface roughness (using optimized CMP processes) and removing surface oxidation.

For eutectic wafer bonding, the surface micro-roughness is not as important as the flatness requirements for the wafer. For MEMS packaging, the eutectic metal seal ring width and height can be selected based on the surface waviness and bow/warpage of the mating substrates. Typically, for eutectic bonds the surface metal stacks thickness should be 1.5 times the surface flatness. Eutectic bonds can conform to wafer topography and provide hermetic seals. Figure 4 illustrates the different seed layer and eutectic metal thickness for common eutectic bond types. These stacks are based on wt% of the interlayer for target composition and the ratio of parent metal to interlayer that will produce that composition. Depending on the surface roughness and flatness of the substrates to be bonded, the stack thicknesses of the eutectics can be increased or decreased while keeping the target eutectic composition more or less constant.

ADHESIVE BONDS

Adhesive bonds are the most forgiving when it comes to wafer surface roughness and flatness requirements due to the ability of the soft adhesive material to deform and conform to the surfaces being bonded. When an intermediate adhesive material is used to join two solid-state surfaces it is naturally the adhesive material that deforms to fit the surfaces to be bonded and not the rigid substrates. During the bonding process, the adhesive in a liquid or semi-liquid phase wets the surfaces to be bonded and flows into the valleys of the surface profile. The thicker the adhesive film, the less stringent the surface requirements. To put in perspective,

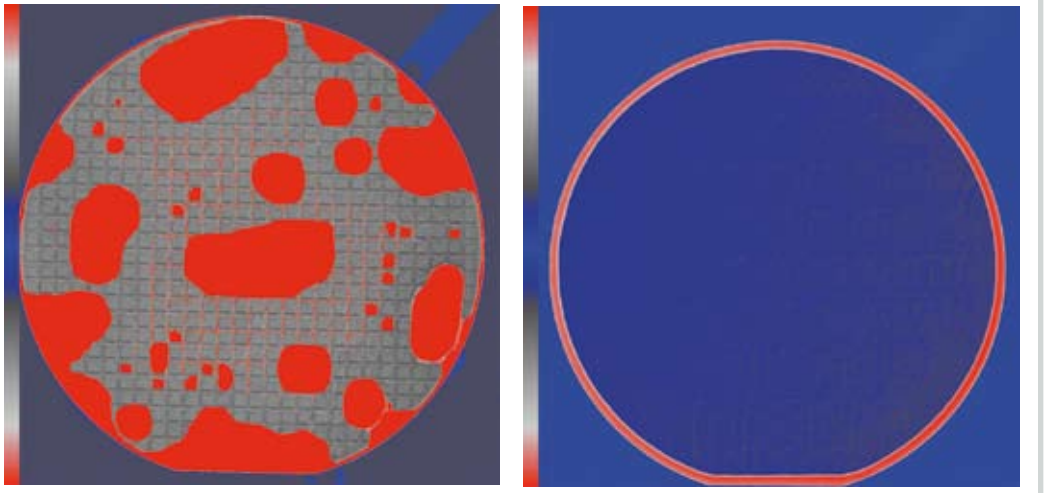

Figure 2: Comparison of (a) Bonded pair using as-deposited undensified TEOS and (b) Bonded pair using densified and CMP'd TEOS. Both pairs were direct bonded in the CL200 followed by 400C, 1 hour anneal in N2 ambient

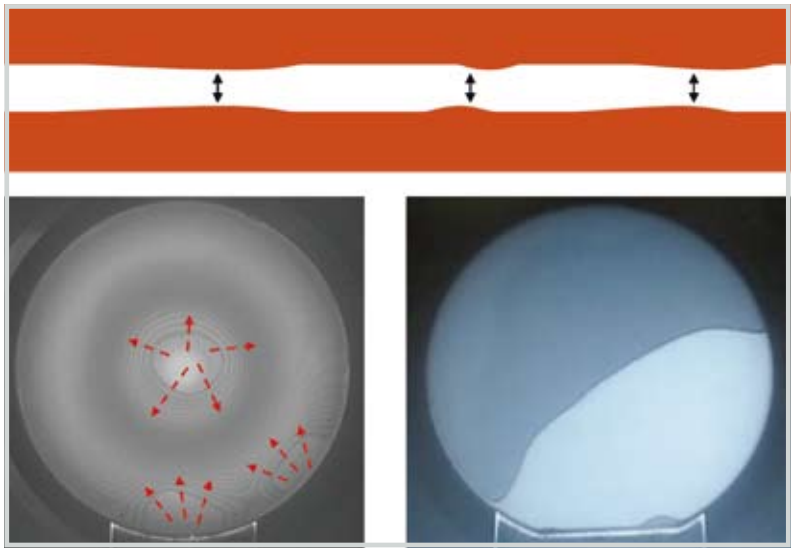

Figure 3:
(a) Sketch showing and exaggerated view of two non-uniform surfaces for direct bonding (b) Multiple wave-front propagation and collision voids during direct bonding of a nitride on Si to an oxide on Si due to CVD deposited silicon nitride surface non-uniformity(c) Single wave-front propagation in a Si-oxide direct bonded pair.

Figure 4: Typical seed layer and eutectic/metal stack thicknesses for (a) AuIn, (b) AuSn and (c) AuSi eutectic bond seal rings for MEMS wafer bonding

on a wafer surface with TTV close to 2 µm, SOG films which are typically very thin (<500nm) will be harder to bond compared to a BCB film which is typically spun on much thicker (thickness >1 µm). Polymers that have low viscosity, slow hardening speeds and low shrinkage during hardening generally achieve better filling of the trenches of a surface profile.

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Website of Silicon Quest Intl.
www.siliconquest.com

SUMANT SOOD
is the Senior Applications Engineer for Wafer Bonders at SUSS MicroTec. His recent experience includes development of plasma enhanced wafer bonding processes for SOI and strained silicon on Insulator (sSOI) applications. Sumant has authored and co-authored more than 15 papers in wafer bonding, SOI, strained silicon and related areas. He received his B.Tech in Electrical Engineering from Punjab Technical University, India and MS in Microelectronics from University of Central Florida.

Clif's Notes

Is the Tail Wagging the Dog?

Clifford J. Hamel, SUSS MicroTec

INTRODUCTION

Did you pay a large sum of money for your measurement tool? If so then it is possible that you are placing a lot of faith in the numbers it generates simply because of the cost. After all any tool that costs hundreds of thousands of dollars must be good! This general acceptance of measurement tool data will frequently have detrimental effects on the control and operation of a manufacturing process. That is to say, if the measurement tool is not accurate or then changes in your product quality caused by the measurement tool will be interpreted as changes due to your process. The result is that the measurement tool will be causing you to make changes in the production process when they are not needed!

We will present the basics of assessing the capability of a measurement tool as it might be encountered in a semiconductor manufacturing facility.

Did you pay a large sum of money for your measurement tool? If so then it is possible that you are placing a lot of faith in the numbers it generates simply because of the cost. After all any tool that costs hundreds of thousands of dollars must be good! This general acceptance of measurement tool data will frequently have detrimental effects on the control and operation of a manufacturing process. That is to say, if the measurement tool is not accurate then changes in your product quality caused by the measurement tool will be interpreted as changes due to your process. The result is that the measurement tool will be causing you to make changes in the production process when they are not needed!

We will present the basics of assessing the capability of a measurement tool as it might be encountered in a semiconductor manufacturing facility.

SOURCES OF VARIATION AND SOME COMMON TERMS

In most semiconductor manufacturing lines there are four main sources of variation which will affect overall product quality,

1 Measurement tool variation.
2 Process variation comprised of
  a) Within substrate,
  b) Substrate to substrate, and
  c) Batch to batch variation.

The accepted level of contribution of the measurement tool to the variation in the process, i.e. the process specification, is typically less than ten percent. As the effect of measurement tool variation increases it will soon approach the point of 'wagging the dog' and your process will be out of control! The term used to describe the contribution of measurement tool variation is called the precision to tolerance ratio (P/T). It is defined as the ratio of the measurement tool precision to the specification. Precision is the degree of agreement of repeated measurements of the same parameter, such as temperature, expressed in terms of the standard deviation.

	Groups											
	A				B				C			
Test Sample	1st	2nd	3rd	Range	1st	2nd	3rd	Range	1st	2nd	3rd	Range
1	0.3465	0.3656	0.4060	0.0596	0.3671	0.3122	0.3365	0.0549	0.2981	0.3167	0.3498	0.0517
2	-0.2764	-0.2228	-0.2389	0.0535	-0.1939	-0.2203	-0.2149	0.0264	-0.2203	-0.2210	-0.2379	0.0176
3	-0.6141	-0.5909	-0.6246	0.0337	-0.6245	-0.6532	-0.7221	0.0976	-0.6901	-0.6037	-0.5886	0.1015
4	0.7523	0.7428	0.8031	0.0602	0.7166	0.7588	0.6655	0.0933	0.7717	0.7284	0.7693	0.0432
5	0.3269	0.3800	0.3448	0.0531	0.3161	0.4094	0.4317	0.1156	0.4831	0.4936	0.4907	0.0105
6	-0.7443	-0.7601	-0.7936	0.0492	-0.7834	-0.7758	-0.7165	0.0669	-0.7358	-0.8030	-0.7693	0.0673
7	-0.7681	-0.7139	-0.7780	0.0641	-0.7524	-0.7367	-0.7475	0.0157	-0.7738	-0.7518	-0.7499	0.0239
8	-1.3169	-1.3952	-1.2319	0.1632	-1.3253	-1.2850	-1.3182	0.0403	-1.2803	-1.0747	-1.2526	0.2056
9												

Figure 1: Measurement Results

Before proceeding we will define here a short description of those statistical terms near and dear to your heart:

Accuracy:
the relationship of the average of a group of measurements to the real or standard value.

Repeatability:
a measure of variation often expressed as the standard deviation of results obtained by the same operator using the same instrument in successive measurements.

Reproducibility:
the variation in measurement averages when several tests are made under the same conditions by several people, sites, or measurement units.

Stability:
the variation of measurement averages over a period of time.

Capability:
combined variation of tool due to accuracy, repeatability, reproducibility and stability.

Total measurement error, precision, is sum of the repeatability and reproducibility errors using the law of addition of standard deviations.

HOW DO I DO THAT?

Well there are some significant, but straight forward statistical procedures*1 involved in determining the gage capability of a measurement tool. But with some simple ground rules and a little help from an Excel spreadsheet*2, see Figure 4, it can be made very easy and non-statistical. We will concentrate on understanding the concepts of using the gage capability procedure and avoid the statistics.

Consider that you have a measurement tool which is pretty much automated, i.e. you basically define a measurement program or sequence which is then used by an operator to make measurements. Therefore it is unlikely that there will be significant operator to operator measurement dependency, but there will surely be variation day to day due to ambient or other conditions. So what do we do next? It is very simple:

IDENTIFY THE MEASUREMENT TOOL.

A. Locate and identify up to ten samples to be measured, ensure the samples represent a good spread of possible measurement values. Note that the parts to be measured are not required to be identical, in fact, the more variation the better. A minimum of five samples is recommended.

B. Define the measurement program(s) for the samples to be measured.

*1 Based on article by Harvey C. Charbonneau, Gordon L. Webster, Industrial Quality Control, 1978 Prentice-Hall, Inc., ISBN 0-13-464255-4, Appendix 1, Evaluating Gage Capabilities.

*2 The spreadsheet is available upon request from the author.

DSM 8: SUSS MicroTec's Front-to-Backend Alignment Tool

Test for Control

Upper Control Limit = D4 x Rdbar = 2.574 0.0654 = 0.1682 um

If any individual range exceeds this limit the measurement is suspicious. Review, repeat or correct to ensure a valid test.

Figure 2
Test for Control

Capability Analysis

Repeatability/Equipment Var = K1 x Rdbar =	0.591	0.0621	=	0.0367 Repeatability	(1 sigma value)
Reproducibility/Operator Var = K2 x Xdiff =	0.446	0.0261	=	0.0116 Reproducibility	(1 sigma value)

Total Gage R & R = sqrt [Repeatability^2 + Reproducibility^2] = 0.0385 (1 sigma value)

Gage Acceptability =	Total Gage R&R / Specification Tolerance	=	0.198201 / 2	=	9.9%	Great!

The Gage is acceptable if the percentage value is less than 25%, but should be less than 10%.

Figure 3
Summary of Measurement Tool Capability P/T Ratio

C. Measure each sample once, then measure them again but in a different order and repeat again for a total of three measurements. You may repeat only two measurements per sample which may have some impact on the results of the gage capability. We recommend three repeat tests per group.

D. Wait one day then repeat the random measurements again. Wait a third time and then repeat the measurements for a total of three data groups. The delay is to allow for possible changes in ambient conditions or other parameters such as calibrations of the tool, etc.

E. Fill in the Excel data sheet; ensure you input the three-sigma specification of the product that this tool will be used to control. Your final P/T ratio of the tool will be found at the bottom of the sheet and it should be less than 10% of the specification.

AN EXAMPLE

Let us assume you have an automated measurement tool which you need to evaluate such as the SUSS DSM8 front to back alignment system. This system will measure how well the patterns on the front of a substrate are aligned to patterns on the back of the substrate, i.e. overlay measurement. In normal operation you simply need to create a measurement program for your samples, place the substrate on the tool and press start.

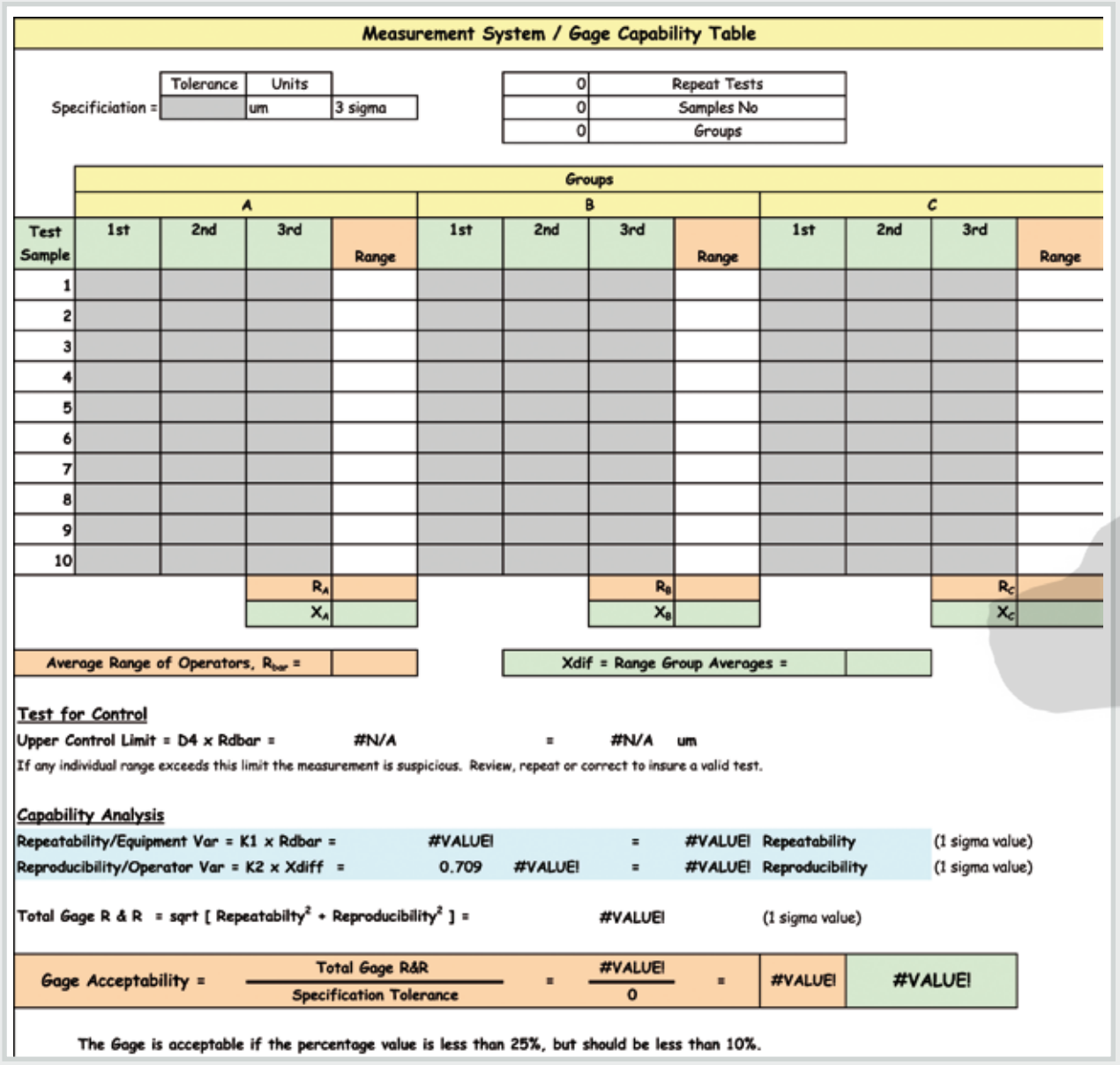
We have selected eight substrates with a wide range of overlay values for the test. Measure the substrates over a period of three days per D and E in the previous section; do not attempt to review the results until all measurements are completed, Figure 4. We recommend that you record the measured values to one decimal place more than the instruments output, i.e. if the least value output is 0.001µm then record to 0.0001µm.

Your first step in the analysis is to make sure that your measured values are reliable. Simply look at the Excel sheet section of Figure 4, highlighted above in Figure 2. The test for control value, 0.1682, indicates that any range value exceeding this term is suspect and should be reviewed.

Note the value circled in Figure 1 exceeds the limit suggested in the test for control section. Look carefully at the second set of readings taken in Group C of the test and you will see that the measured value is not in the same range as the other readings. Note that the variation of the measurements for this sample is clearly not at the same level of all the other sample values. Clearly something is unusual about this sample and you should consider reviewing it in more detail to understand why results from this sample are so high. Perhaps this particular sample should be removed from the analysis until you can identify why the results are so clearly different. In so doing the final gage capability value will change from 0.198µm to 0.173µm and the overall P/T ratio of the tool will change only slightly. Use the data or not, it's your choice since the spreadsheet will make the proper changes to the test procedures based on your input. The analysis results presented in Figure 3 clearly indicate the measurement tool is acceptable assuming a product specification of 1.0 µm. However, if future production parts require meeting a tighter specification, then an understanding of the measurement tool variation would have to be taken into consideration.

That's it; you're done with the easy part. Now you have to decide if you want to continue using your measurement tool! In the case of the SUSS DSM8 tool the capability is "Great" and we may continue to rely on the tool to monitor our process.

Figure 4
Measurement Capability Worksheet



Measurement System / Gage Capability Table

	Tolerance	Units	
Specificiation =		um	3 sigma

0	Repeat Tests
0	Samples No
0	Groups

	Groups											
	A				B				C			
Test Sample	1st	2nd	3rd	Range	1st	2nd	3rd	Range	1st	2nd	3rd	Range
1												
2												
3												
4												
5												
6												
7												
8												
9												
10												
			R_A				R_B				R_C	
			X_A				X_B				X_C	

Average Range of Operators, R_{bar} =

Xdif = Range Group Averages =

Test for Control

Upper Control Limit = D4 x Rdbar = #N/A = #N/A um

If any individual range exceeds this limit the measurement is suspicious. Review, repeat or correct to insure a valid test.

Capability Analysis

Repeatability/Equipment Var = K1 x Rdbar =	#VALUE!		=	#VALUE!	Repeatability	(1 sigma value)
Reproducibility/Operator Var = K2 x Xdiff =	0.709	#VALUE!	=	#VALUE!	Reproducibility	(1 sigma value)

Total Gage R & R = sqrt [Repeatability^2 + Reproducibility^2] = #VALUE! (1 sigma value)

Gage Acceptability = Total Gage R&R / Specification Tolerance = #VALUE! / 0 = #VALUE! #VALUE!

The Gage is acceptable if the percentage value is less than 25%, but should be less than 10%.

CLIF HAMEL
is the principle applications engineer at SUSS MicroTec, Inc. for lithography processes involving full field mask aligners and automated cluster coating equipment. Over the last 12 years at SUSS he has co-authored several papers in the field of thick resist processes and process optimization. He has over 26 years of BEOL process and mask fabrication experience at IBM where he was the principle engineer and inventor for lift off process development. He received his BS in chemical engineering at Trinity College of Vermont.

SUSS MicroTec in the News

**Here's a summary of our recent press releases.
To read the entire press release, please visit
http://www.suss.com/company/news**

April 14, 2009

SUSS MicroTec Test Systems Chosen for Advanced Testing Laboratory at Ualbany NanoCollege

SUSS MicroTec Test Systems today announced receipt of purchase orders for test equipment that will enable the development of next-generation integrated circuits (ICs), including CMOS transistor scaling to the 16-nm node and beyond and the investigation of the reliability characteristics of high-k dielectrics. The partnership with SEMATECH, a global consortium of chipmakers, Core Wafer Systems and the College of Nanoscale Science and Engineering (CNSE) of the University at Albany includes advanced 300-mm wafer-level characterization systems with ProbeShield Technology and a cryogenic probe capability system to be installed at CNSE's world-class Albany NanoTech Complex.

"The SUSS Cryogenic Probe System provides a core competence within CNSE's Albany NanoTech that will help researchers recognize how newly developed processes can improve the desired fundamental properties of advanced substrates.„
Richard Brilla, Vice President for Strategy, Alliances and Consortia at CNSE

April 22, 2009

SUSS MicroTec Receives Multiple Orders from Nemotek Technologie for Wafer-Level Camera Production to use in Portable Applications

Nemotek Technologie, a manufacturer of customized wafer-level cameras for portable applications, has selected multiple lithography systems from SUSS MicroTec. The deal includes a 200mm production mask aligner, coat, bake and develop systems. The systems have been selected for their image sensor wafer-level packaging (WLP) and wafer-level optics (WLO) services and were successfully installed at Nemotek's facility in Rabat Technopolis Park, Morocco.

"We truly believe that wafer-level camera solutions are the technologies of the near future„
Jacky Perdrigeat, CEO of Nemotek Technologie

April 28, 2009

SUSS MicroTec Test Systems Named Exclusive Supplier of 300 mm Characterization and Reliability Test Solutions

SUSS MicroTec Test Systems has announced that it has once again won a head-to-head evaluation with its unique PA300PS with ProbeShield® Technology, the 300 mm wafer-level probe system for device characterization and reliability test. The evaluation took place at a major integrated device manufacturer (IDM) located in the United States. As the winner of the evaluation, SUSS MicroTec has been named the exclusive supplier of on-wafer characterization systems for three years and is committed to work diligently in maintaining this position for many years beyond. As expected, the manufacturer has already placed the first system order.

"The engineers at the manufacturer chose ProbeShield Technology due to the superior positioning accuracy especially on small pads and significant time savings„
Rick Dock, Vice President of North American Sales at SUSS MicroTec

June 4, 2009

SUSS MicroTec Introduces New Illumination System for Mask Aligners

SUSS MicroTec launches with the MO Exposure Optics a new illumination system designed for all generations of manual and automatic SUSS mask aligners. The new optical system is based on unique microlens arrays of high optical quality to provide higher intensity, improved exposure light uniformity and customized illumination shaping. This allows users of SUSS MicroTec mask aligners to optimize the process window and enhance yield in contact and proximity lithography. MO Exposure Optics (patent pending) has been exclusively developed by SUSS MicroOptics, a world leading supplier for high-quality optic solutions in illumination, laser beam shaping, metrology, medical and vision systems.

"By offering the possibility to upgrade the installed base with the new MO Exposure Optics illumination system we help our customers to protect their investment in the well-proven mask aligner technology„
Frank P. Averdung, President and CEO of SUSS MicroTec AG

June 10, 2009

SUSS MicroTec Introduces New |Z| Probe® Technology for Wafer-Level RF Testing

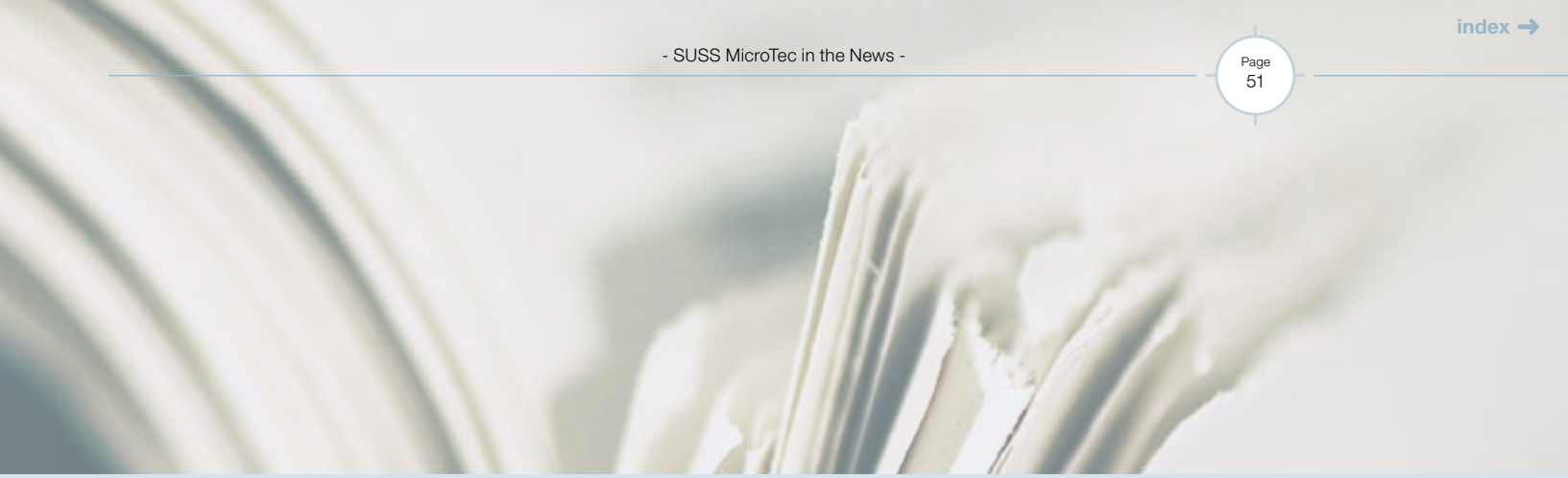
SUSS MicroTec Test Systems has introduced 1MX™ Technology for its line of on-wafer RF probes, the |**Z**| Probe®. The new technology significantly improves the high-frequency performance of the |**Z**| Probe by minimizing unwanted signal loss, reflection, and crosstalk and by extending the frequency range. Design enhancements provide test engineers with the new level of measurement accuracy when characterizing nanoscaled RF and microwave devices.

*"The |**Z**| Probe family, with its unsurpassed lifetime and excellent contact quality, reliability and repeatability providing lowest cost of ownership, is now expanded with the new 1MX Technology"„*
Dr. Stojan Kanev, Director of Marketing and Product Management at SUSS MicroTec

June 22, 2009

3M and SUSS Announce Agreement on Temporary Wafer Bonding Technology to Enable 3-D Semiconductors

3M, a leading supplier of advanced materials to the semiconductor industry, and SUSS MicroTec today announced an agreement to expand access to 3M Wafer Support System (WSS) equipment for temporary wafer bonding of ultrathin wafers required for 3-D packaging. As part of this non-exclusive agreement, SUSS MicroTec becomes an authorized equipment supplier for the 3M WSS and will manufacture and sell XBC300 and CBC300 wafer bonders



configured to use 3M's WSS materials including 3M Liquid UV-Curable Adhesive and Light-To-Heat Conversion coating. Under the agreement, both companies will work closely to address customer demands for high-performance process solutions that support high-volume manufacturing with a competitive cost of ownership.

"SUSS MicroTec is a recognized leader in wafer bonding and applications for 3-D and MEMS markets„ Mike Bowman, marketing development manager for 3M Electronics Markets Materials Division

July 1, 2009

SUSS MicroTec Strengthens Presence in Asia with New Sales Structure

SUSS MicroTec today announced a new structure for sales in Asia based in Singapore. With the consolidation of the sales office in Bangkok (Thailand) having administered sales and service for lithography and wafer bonder equipment in Asia and the former Singapore office of SUSS MicroTec Test Systems to a joint sales office for the three product lines in Singapore and with the appointment of ZMC Technologies as general sales representative for Malaysia, Singapore and Philippines SUSS MicroTec reinforces its strong presence in Asia already maintaining sales offices in Seoul (Korea), Shanghai (China), Yokohama (Japan) and Hsinchu (Taiwan). SUSS MicroTec now also operates two fully equipped application centres in Yokohama and Singapore and provides realtime after-sales support for both process and test solutions to its Asian customers.

"Within the global semiconductor and MEMS markets customers demand new advanced processes requiring the one-source solutions offered by SUSS MicroTec. Streamlining our organization is therefore a logic step for us" Frank Averdung, CEO and President, SUSS MicroTec

July 8, 2009

SUSS MicroTec and Thin Materials Cooperate on Temporary Bonding Solution for 3D Packaging

SUSS MicroTec and Thin Materials, a semiconductor process development company, announced today that they are cooperating on a temporary bonding solution to be used for challenging thin wafer handling technologies required for emerging 3D Integration and Packaging technologies. With this cooperation SUSS MicroTec extends its solution portfolio for temporary bonding and thin wafer handling.

"Thin Materials' technology for temporary bonding perfectly complements our process offering portfolio for 3D Integration and Packaging„ Frank Averdung, CEO and President, SUSS MicroTec

July 14, 2009

IMEC and SUSS MicroTec to Collaborate on Wafer Bonding for 3D Integration Applications

SUSS MicroTec and the Belgian nanoelectronics research center IMEC have entered a joint development program. Together, they will develop permanent bonding, temporary bonding and debonding processes for 3D system integration, including through-silicon-via (TSV) manufacturing. IMEC will use SUSS MicroTec's XBC300 production wafer bonder platform to develop 200 and 300mm permanent metallic interconnect bonding, as well as temporary bonding and debonding solutions for its 3D-stacked Interconnect and 3D Wafer Level Packaging technology.

"Working with IMEC, a premier research facility, on 300mm 3D development for temporary and permanent bonding applications is an exciting opportunity for SUSS MicroTec„ Wilfried Bair, General Manager, SUSS MicroTec's Bonder Division

August 25, 2009

SUSS MicroTec Expands 3D Integration Activities in Japan

SUSS MicroTec has shipped a LithoPack300 lithography cluster to Japan. The system has been successfully installed at the customer site where it will be used for 3D integration technology development. The cluster solution with coat, bake, expose and develop modules for wafers up to 300mm constitutes a cost-efficient approach for the challenging Through-Silicon-Via (TSV) manufacturing and backside redistribution layer (RDL) in 3D integration production. With this integrated lithography solution and further solutions for permanent and temporary wafer bonding SUSS MicroTec offers a complete process and technology portfolio for 3D integration. SUSS MicroTec has recently announced its participation in a range of research projects on 3D integration processes driving technology advances from the equipment supplier side.

"With the involvement of SUSS MicroTec in international research cooperations we are proud to become further involved in 3D integration process development„ Raymond Lau, Business Manager for SUSS MicroTec in Japan

September 1, 2009

SUSS MicroTec Launches World's First 300mm Test Solution for 3D Integration

SUSS MicroTec announces the release of the probe station PA300PS 3D geared for 300mm electrical probing of 3D stacked structures on wafer level and targeted at the market for 3D integration. The flexible probe station allows for various engineering and monitoring tests after wafer production as well as before further stacking steps or final packaging. With the launch of the new tool SUSS MicroTec supplements its product suite of wafer bonders and lithography equipment for 3D integration.

"The roadmap of SUSS MicroTec's Test division clearly meets the industry's demands for a test solution for 3D integration„ — Wilfried Bair, VP Business Development SUSS MicroTec

Where to Meet SUSS MicroTec in the Next Months

September 2009

Seminar: Accurate Device Characterization and Modeling Solutions · Germany, Switzerland, France, Belgium	15. - 22. Sep.
IEEE (3DIC) · San Francisco, USA	28. - 30. Sep.
MNE · Gent, Belgium	28. Sep. - 1. Oct.
European Microwave Week · Rome, Italy	28. Sep. - 2. Oct.
SEMICON Taiwan · Taipeh, Taiwan	30. Sep. - 2. Oct.

October 2009

ESREF · Arcachon, France	5. - 9. Oct.
RF Measurement Technology Conference · Gävle, Sweden	6. - 7. Oct.
RF & Hyper · Paris, France	6. - 8. Oct.
SSDM 2009 · Miyagi, Japan	7. - 9. Oct.
NEXT Conference · Shanghai, China	12. - 14. Oct.
Webcast: New Opportunities for Nano Imprint TechnologiesWebinar	20. Oct.
IWLPC · Santa Clara, CA/USA	27. - 30. Oct.

November 2009

ISTFA · San Jose, CA/USA	15. - 19. Nov.

Please check our website for any updates: www.suss.com/events

We hope you found this edition of the SUSS Report interesting and informative.
For more information about SUSS and our products, please visit

www.suss.com

or write to **info@suss.com** with your comments and suggestions.

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SÜSS MicroTec

Our Solutions Set Standards