ISSUE 01/2012

THE CUSTOMER MAGAZINE OF SUSS MICROTEC

EXPANSION OF TECHNOLOGY COMPETENCE

TAMARACK Scientific Co., Inc. is now a SÜSS MicroTec AG Company

Lithography *PLUS*...

Partners for Technology Leadership

Laser Ablation – Emerging Patterning Technology for ADP

Advanced Mask Aligner Lithography (AMALITH)

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+EDITORIAL

The requirement for more functionality and higher performance of electronic devices drives the increasing performance needs for semiconductor components and higher complexity at the same time. SUSS MicroTec understands that this trend requires the adoption of innovative technologies in the semiconductor backend. Over the last years initiatives were undertaken to focus SUSS MicroTec onto this task and prepare the company for the future.

Frank Averdung, President & CEO of SÜSS MicroTec AG explains the strategic background of the recent acquisition of Tamarack Scientific Co., Inc. (Tamarack).

Why did you decide to acquire Tamarack Scientific?

With including Tamarack into the SUSS MicroTec Group we significantly expand our core expertise in backend lithography and bring ourselves in a position where we can respond to all exposure requirements from the market.
Tamarack develops, manufactures and distributes innovative UV projection lithography systems as well as laser micro-structuring tools for markets like Advanced Packaging, 3D Integration, MEMS and LED. The systems address the requirements of high volume industrial manufacturing as well as research and development.

Two main reasons were driving the decision for Tamarack Scientific:
SUSS MicroTec strengthens the company's lithography segment by adding a complementary patterning technology to our existing exposure capability. The comprehensive set of products and technologies of proximity printing and UV projection enables SUSS MicroTec to perfectly match various application requirements. It also allows the company to offer a broad product range at different price and performance points as required by the industry.

In addition SUSS MicroTec gains access to Laser processing and structuring expertise. Laser based patterning technology has the potential to complement existing solutions in applications, such as Fan-out WLP. While being an enabling technology it promises cost saving at the same time.
The merger of both companies combines Tamarack's innovative technology offerings with SUSS MicroTec's global footprint and excellent market access.

What are the next steps?

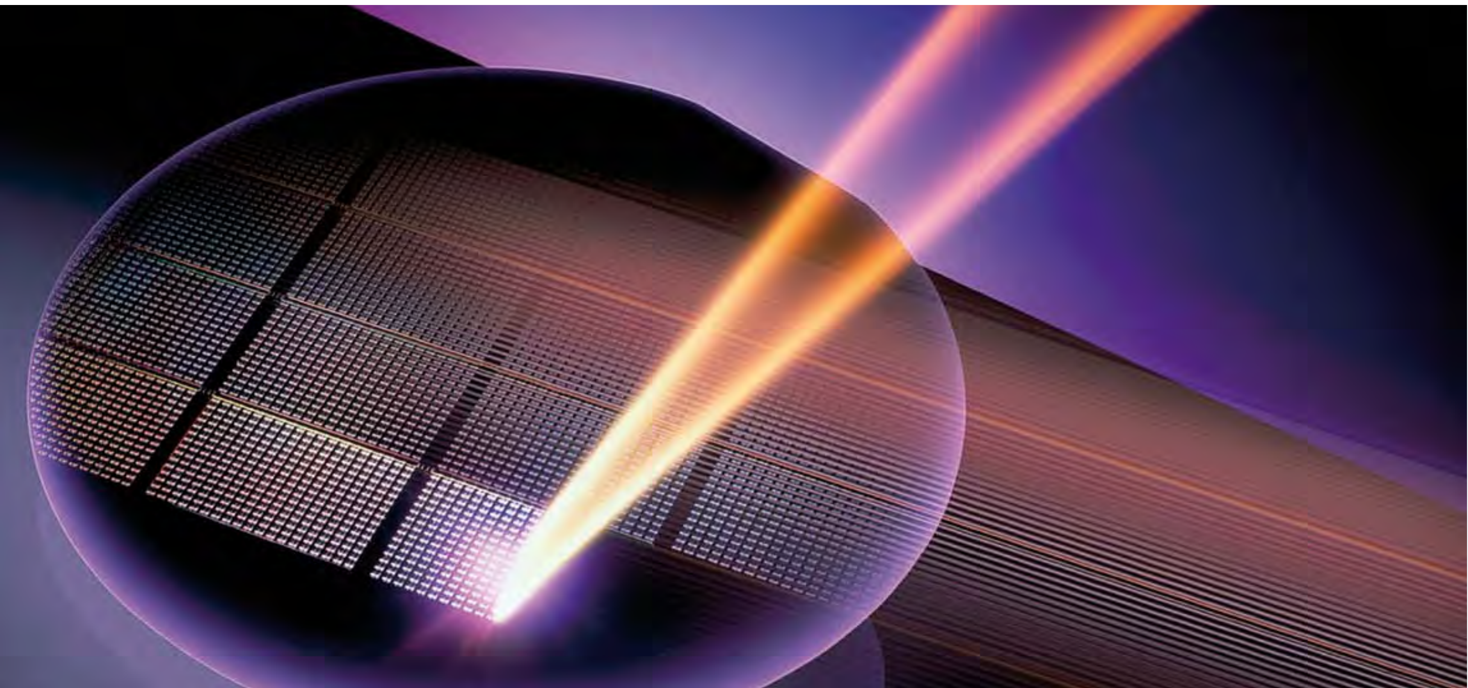
We have already enlarged the SUSS MicroTec sales and service structures by including Tamarack's systems into our products and solutions offering.
The goal is to immediately make available the Tamarack "technology kit" to our target markets through our existing distribution channels.
Subsequently we are going to align roadmaps and adapt R&D activities to meet future requirements of the industry. The alignment and further development of the comprehensive set of exposure technologies allows us to offer the "best technology fit" to our customers. With our joint exposure and lithography expertise we are going to address markets and applications, which in the past were difficult to address for either SUSS MicroTec or Tamarack.

What are the plans with the factory in Corona?

Our facility in Corona has become the competence center for projection lithography and laser processing. In fact we are heavily investing into this site to strengthen our engineering and manufacturing capabilities.
Thanks to this acquisition SUSS MicroTec strengthens its position as the leading backend lithography equipment and solution provider by offering the most comprehensive set of products and technologies to the market.

Read more about other interesting lithography projects in this issue.

Frank Averdung
President & CEO
SÜSS MicroTec AG



LASER ABLATION – EMERGING PATTERNING TECHNOLOGY FOR ADVANCED PACKAGING

Ralph Zoberbier, SUSS MicroTec Lithography GmbH, Schleissheimer Str. 90, 85748 Garching, Germany
Matt Souter, TAMARACK Scientific Co., Inc., 220 Klug Circle, Corona, California 92880-5409, USA

INTRODUCTION

Wafer Level Packages have emerged as the fastest growing semiconductor packaging technology. Rather than a single solution, wafer level packaging technologies are a set of different solutions including flip-chip wafer bumping, electroplated gold, solder bumps and recent copper pillar technologies. These chips can be packaged in many different ways, through fan-in WLCSP, fan-out WLP, 3D WLP, interposer and 3D IC interconnections using TSV's.

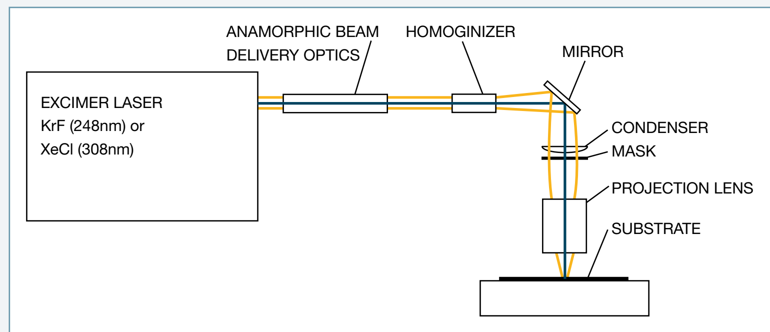


Figure 1. Tyical optical set-up of an excimer laser system

One of the most critical process steps of each technology is the patterning of features or interconnects in a most efficient but reliable manner. Nowadays, proximity exposure technologies (mask aligner) or projection lithography (step and repeat or scanning) are the typical choices to create redistribution lines, pads, TSV patterns and others. However, the latest developments and advances in Excimer laser ablation and complementary technologies, offer the promise of further reductions in manufacturing costs as well as enhancements in chip performance.

This article provides a general overview of the Excimer laser ablation technology delivered by the equipment set from Tamarack Scientific Inc., recently acquired by SUSS MicroTec in March 2012.

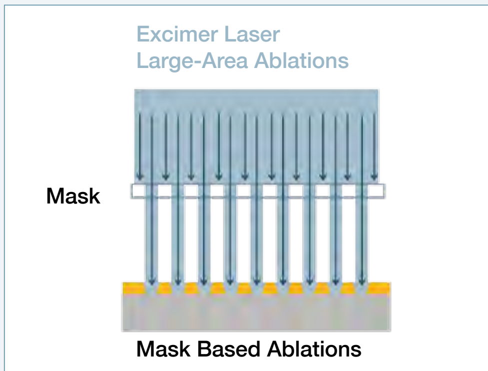


Figure 2. Mask based ablatoin optimizes throughput and pattern placement

WHAT IS LASER ABLATION?

Excimer Laser ablation is a dry patterning process, utilizing a 248nm or 308nm excimer laser source. The laser light is shaped and homogenized through a series of optics, where it is projected through a mask. The mask itself defines the pattern to be ablated, which is projected through a reduction lens onto the substrate or wafer, removing the material as desired. This technology is quite similar to a typical UV Stepper, however, instead of exposing a photo imagable material, the substrate is etched directly without the need for a photosensitive material nor any of the post develop and etch processes that accompany a photolithography process. Ablation is a physical and photo chemical removal process, breaking the materials molecular structures and directly etching the circuit patterns to desired depths on the substrate. Only those areas not protected by the mask are ablated, unaffecting the areas surrounding. This 'non-thermal' laser ablation process produces a very accurate replication of the mask image. Combined with a large field projection lens and high power laser, the system can ablate areas up to 50 x 50mm at one time, resulting in high throughput in comparison to other patterning technologies such as DPSS ablation or LDI (Laser Direct Imaging), where single laser beam is rastered, greatly limiting throughput capability.
Laser ablation offers the ability to directly etch materials, offering a means to significantly reduce manufacturing costs in comparison to a photolithography process. By using Excimer laser ablation, many process steps and costly materials can be eliminated from the manufacturing flow, including resist coating, baking, developing, resist stripping and etching.

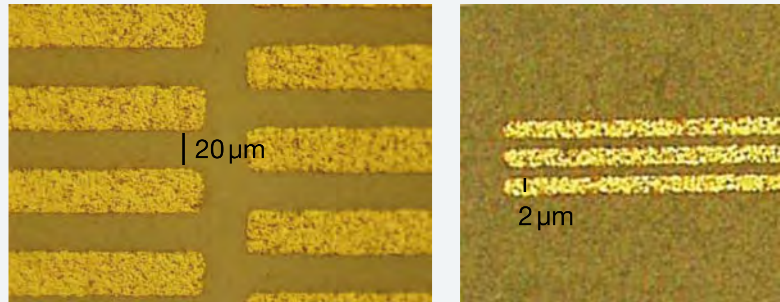


Figure 3. 50nm ablated Au pattern on PET

Furthermore, laser ablation enables the use of less expensive non-photosensitive materials, which often promote better thermal characteristics. Excimer ablation is suitable for ablating a wide variety of polymeric materials, thin metals (<600nm), epoxies, nitrides and other organic materials. For example, the technology can be applied to pattern conductive films over polymer layers, while not damaging the underlying polymers.

LASER ABLATION EQUIPMENT

Tamarack Scientific, recently acquired by SUSS MicroTec, has been designing, engineering and manufacturing laser ablation equipment since 1987 and recently introduced its 6th generation laser ablation stepper (ELP300), targeted at the advanced packaging market. While laser ablation is already in use in many other electronic applications, including the medical and display markets, the WLP industry has also begun to embrace this technology as a means to not only lower manufacturing costs, but also achieve requirements for next generation chip packages. The equipment platform is designed to address WLP applications, with standard platforms to

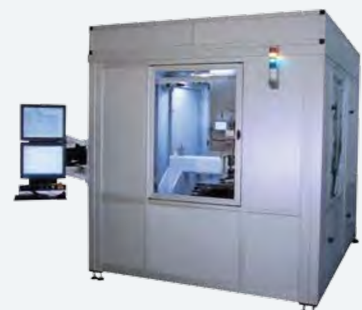


Figure 4. ELP300 Laser ablation stepper

automatically handle wafers up to 300 mm and substrates up to 800 x 800 mm. Using a step and repeat approach, similar to a UV stepper, the system can also compensate for substrate run-out.

The system allows the patterning of traces to 2 µm and vias down to 1µm, with alignment accuracies <+/-1 µm. System throughput is dependent on material type and desired ablation depth.

In addition, the same Excimer laser based system can also be utilized for other WLP applications including laser debonding for 3D TSV's, RDL/UBM seed layer removal and for resist exposure. This makes it the perfect versatile tool for laser processing in packaging applications.

LASER ABLATION IN WLP APPLICATIONS

Laser ablation, by design, offers a significant potential for manufacturing cost reduction and is currently being investigated by the packaging industry for various applications including patterning of RDL trenches and vias in FOWLP and WLCSP, blind via drilling for 3D TSV and via drilling for PoP applications in EMC for FOWLP.

In 2010, at the IEEE (ESTC conference) hosted in Berlin, AMKOR announced the development of a Fan-Out WLP Technology based on laser ablation patterning, addressing lower cost patterning solutions. The technology used ABF (Ajinomoto build-up film) and laser ablation to generate the RDL interconnect pattern. ABF, which was developed for multi-layer substrate fabrication, allows direct laser drilling of micro vias and traces, where these are filled with Cu using electro-less or electroplating methods. The process flow is shown on the right. In a similar fashion to more standard fan out processes, chips are first attached face down to a laminating tape and compression molded into wafer form. At this point ABF or other EMC materialsare

Figure 5. Typical Fan Out WLP

laminated on the reconstructed wafer and vias are laser drilled. Thin film processing is used for interconnect and UBM before the solder balls are attached. The parts are then singulated.

In this process, laser ablation is used to directly etch the RDL traces and pads to a specific depth in the dielectric material, followed up by the RDL vias down to the Cu or Au pads in two steps.

In the first step, the trace/pad pattern is aligned to global or local alignment targets. Following alignment, the system ablates the trenches and pads to the desired depth within the material. Folllowing this step, the laser is used to continue ablation of the vias down to the Cu or Al pads, stopping precisely on this metal layer without damaging the pad.

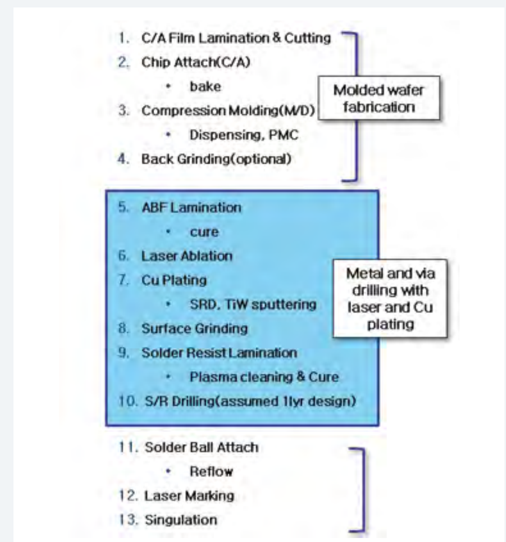


Figure 6. Process Flow
(Source: Yole, I-Micronews; http://www.i-micronews.com/lectureArticle.asp?id=6058)

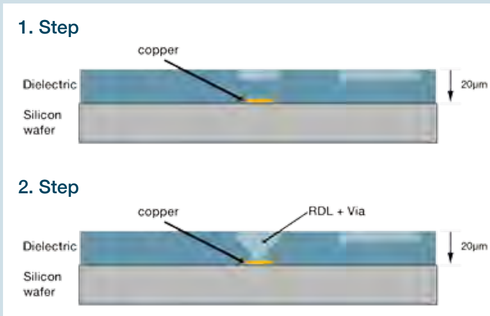


Figure 7a. Excimer ablated dielectric – cross-section

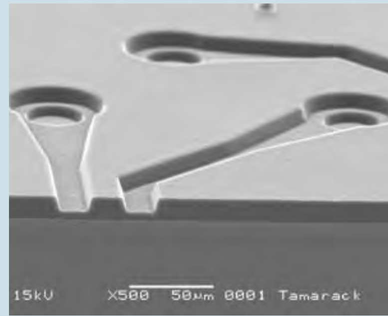


Figure 7b. SEM picture of ablated pattern

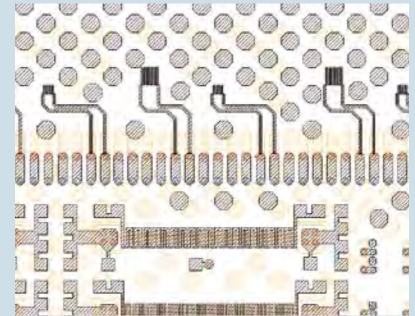


Figure 7c. Two layer RDL and Vias
Courtesy: Fraunhofer IZM ASSID

SUMMARY

The requirement for more functionality and higher performance of electronic devices continues, while also under the continued pressure lower manufacturing costs. This trend will continue, requiring the adoption of innovative technologies in backend semiconductor packaging. Excimer laser ablation is the promising technology that will make and is already making its way into packaging applications to address these future requirements.

With the acquisition of Tamarack Scientific, SUSS MicroTec compliments its patterning technology with projection lithography and laser ablation competence. Laser ablation technology and toolsets are now available by SUSS MicroTec, which have been serving the semiconductor industry for over 60 years, with early adopters within the industry already using this technology in production.

SUSS MicroTec will continue to focus on this promising technology, working in close cooperation with research institutes and industry partners to further increase the application spectrum of laser ablation.

Ralph Zoberbier graduated in 2001 from the University of Applied Sciences in Nuremberg with a Dipl.-Ing. (FH) degree in Microsystems Engineering. He has started his career at SUSS in May 2001 as R&D engineer and took over the role as R&D project manager for the development of the 300mm mask aligner platform in 2003. In 2006 he earned a degree for Master of Business Administration (Entrepreneurship) from post-graduate studies at the University of Louisville, Kentucky. Since 2010 he works as Director Product Management Aligner within the Lithography Division of SUSS MicroTec.

Matt Souter graduated in 1992 from CSULB in California with a BS in Mechanical Engineering. He joined Tamarack Scientific in 2001 and has been active in the role of VP of Sales and Marketing for both the Laser Ablation and Photolithography product lines. Much of his focus as of late, has been in the research and development of alternative patterning techniques using Excimer laser ablation as a means to not only meet next generation Advanced Packaging requirements, but also address a means to lower manufacturing costs. Matt has recently authored an exciting new laser process for the removal of metal seed layers in lieu of standard processing approaches, addressing both technical limitations as well as a reduction in manufacturing costs. This process is currently patent pending. With the recent acquisition, he currently works as Global Sales Director and Laser System Product Manager for SUSS MicroTec.

SIMULATION FOR ADVANCED MASK ALIGNER LITHOGRAPHY

Ulrich Hofmann, Daniel Ritter, Balint Meliorisz, Nezih Unal, GenISys GmbH, Eschenstr. 66, 88024 Taufkirchen, Germany
Michael Hornung, Ralph Zoberbier, SUSS MicroTec Lithography GmbH, Schleissheimer Str. 90, 85748 Garching, Germany

1. INTRODUCTION

Lithography simulation has been a key enabler for IC manufacturing to keep track with Moore's law. 30 years ago, the end of optical lithography had been projected for feature sizes smaller than 1 µm. Just now, Intel announced[1] that they will still use optical lithography for the nodes down to 14 nm. Without lithography simulation and the simulation based source mask optimization technology this would never have been possible.

The history of lithography simulation starts in the 70 s when Rick Dill at IBM Yorktown Heights Research Center created the mathematical equations[2] that describe the basic steps of lithography processes. This was successfully applied to fight a "yield bust" at an IBM factory[3] and thereby became an important tool for understanding and improving lithography tools and processes in the 80 s. Simulation enabled sub-wavelength lithography in IC manufacturing through the introduction of OPC technologies, "source shaping" (off-axis, multi-pole, quasar,… illumination), introduction of phase-shift masks and recently the "source-mask-optimization" technique.
Mask Aligners in the past did not require lithography simulations since they were regarded as tools for "non-critical" applications. However, key differentiators such as cost advantage (e.g. low cost LED), the capability to print on large (e.g. displays) and non-planar (e.g. 3D packaging, MEMS) substrates require mask aligners to push the resolution limits. The application of simulation based resolution enhancement techniques will obviously enable extensions into markets that otherwise could not be served by mask aligners. SUSS MicroTec and GenISys offer mask aligner users the capability to apply techniques like OPC, source-shaping, source-mask-optimization, grey-tone or phase-shift technology to continue using cost effective mask aligner manufacturing beyond the limits of current processes.
The recent development of the MO Exposure Optics for SUSS mask aligner systems in combination with lithography simulation technology enables mask aligners to be used for critical applications with high demands on resolution, topography, large gaps and process window. SUSS mask aligners allow the ability to "shape" the illumination source, GenISys' simulation platform Layout LAB allows finding the optimum combination of source shape and mask layout to print the desired result on the wafer without producing masks, running experiments, and wasting material and time.

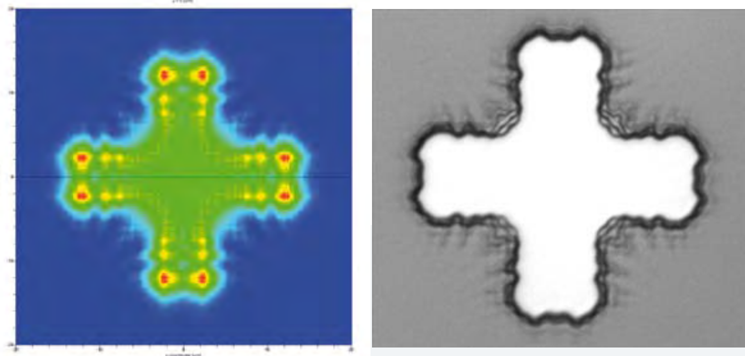


Figure 2. (left) Calculated intensity distribution of a cross-type mask pattern (10 µm line width) at a 30 µm proximity gap. (right) experimental verification (1 µm thick AZ 1518 photoresist on Si)

2. MASK ALIGNER SIMULATION SOFTWARE

2.1 SIMULATION SOFTWARE WITH ACCURATE MODELING OF SUSS MASK ALIGNER

GenISys started to develop the proximity lithography simulation software Layout LAB five years ago. A first market validation came from the flat panel display market, where Layout LAB software was successfully applied to advance the manufacturing of high resolution displays for smart phones by optimizing mask layouts (OPC) and process conditions.

Three years ago, SUSS MicroTec and GenISys joined forces to transfer this potential opportunity to mask aligner lithography applications. The accurate modeling of the SUSS mask aligner tools was developed and integrated as part of the joint project MALS[4,5] that included Fraunhofer IISB in Erlangen, FH Vorarlberg and OSRAM. As a result, the Layout LAB simulation software includes an accurate modeling of SUSS mask aligner exposure optics, including the simulation and optimization of the IFP design (illumination shape), and/or the mask layout in connection with the new MO Exposure Optics.

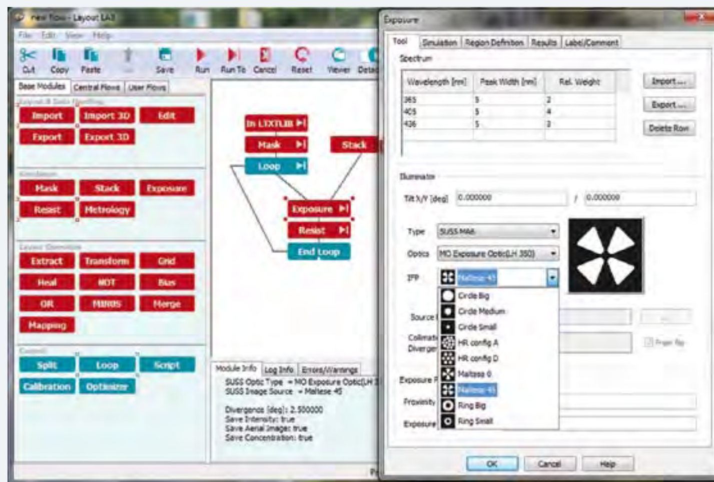


Figure 1. Layout LAB user interface showing the modeling of the SUSS Mask Aligner models with their different illumination types. Also included is the new MO Exposure Optics with the available IFP designs, and the capability to model and optimize customized source shapes.

2.2 SIMULATION OF INTENSITIES IN THE RESIST

The simulation software Layout LAB uses a fast algorithm for calculating the so called “aerial image” (the intensities in air at a given distance below the mask) based on Kirchhoff scalar diffraction theory. The model takes into account a broad band light source (e.g. spectrum of mercury lamp), and the source shape (either circular with collimation angle, or arbitrary, either loaded from a database of measured SUSS mask aligner source shapes, or custom designed). The mask is assumed to be a “thin mask” with the capability to model any transmission (grey tone) and phase-shift. The intensity image is calculated in “one shot” at an arbitrary gap, meaning the calculation time does not depend on the gap. The “aerial image” is transferred into the resist by the “Transfer Matrix Method”, which models the light propagation in the resist and all material layers underneath the resist. All back-reflections from the substrate and the coatings are modelled accurately considering the refractivity and extinction of the materials (n and k values). Layout LAB is also able to model the “bleaching” of the resist (change of absorption coefficient during exposure). The accuracy of the algorithm has been validated by both benchmarking it with rigorous methods, and actual measurements and exposure tests at SUSS MicroTec and mask aligner users. The time for simulating the full 3D intensity image for a typical area of 100 x 100 µm is in the minute range, meaning that hundreds of simulations with

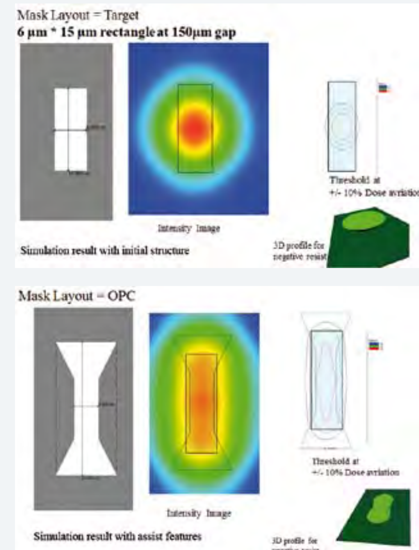


Figure 3. Effect of assist features on figure fidelity. The target shape (6 µm*15 µm rectangle) on the left cannot be printed at a 150 µm proximity gap, whereas the OPC'd structure is much closer to the target.

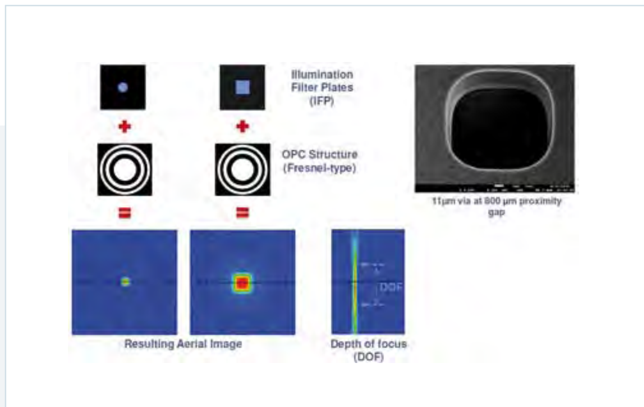


Figure 4. Creative use case for mask aligners – the Fresnel lens on the mask images the source shape directly onto the wafer

different conditions (gaps, source shapes, mask layouts,…) can be done in a few hours.

As the intensity image already contains most of the information on how the structure will print, optimizing mask layout (OPC), source shape (e.g. IFP design), gap and dose variation is typically done based on simulating the intensity image in the resist. The following example demonstrates the beneficial effect of assist features on feature fidelity – both size and position of the assist features were optimized using simulations.

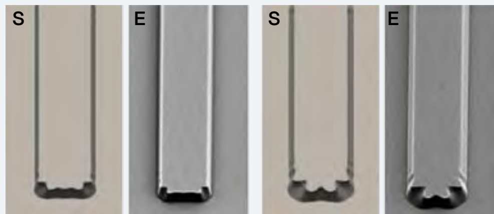


Figure 5. Comparison of simulated (S) and experimental (E) resist profiles for two different illumination settings. Large circular illumination (left) and small circular illumination (right)

Another example of creative use for mask aligners is the following through silicon via (TSV) application. The source shape is the contact to be printed, and on the mask are Fresnel lenses that focus the source shape onto the wafer. This results in a tremendous depth of focus (DOF), required for TSV applications.

2.3 SIMULATION OF 3D RESIST IMAGES

Layout LAB also includes the 3D simulation of the resist development process based on the Dill Model for transferring intensities to photo-active-compounds PAC concentration (depending on sensitivity of the resist) and the MACK4 model describing the removal of the resist during development. The MACK4 is an empirical model with four parameters, modelling the resist development rate depending on the PAC concentration. This parameter need to be calibrated using experimental data from DRM (development rate monitor) or contrast curve. The automated resist parameter calibration to experimental data is included in Layout LAB.

2.4 VIEWS AND ANALYSIS TOOLS

Just looking at a simulated image is a first step in validating printability, but typical questions to a simulation platform go way beyond that. In order to find out the optimum print conditions for a given layout, one will need qualitative and quantitative methods to help sort out various issues.

Qualitative methods include 2D image views as well as their 1D cross sections, and matrix views that allow visualizing the same structure at various process conditions. Matrix views can be collapsed into overlay views to allow a better comparison of the image slope at the target CS position. In order to also be able to make quantitative predictions, the graphs allow reading intensity values, slopes and log-slopes at all positions in the layout.Thereby allowing computing exposure latitude, an important factor for process stability.

From these matrix views, one can quickly generate an analysis view that shows trends and thereby allows the computation of sensitivity values. For example, one can derive the line width sensitivity to gap and collimation angle, which allows generating specs on how accurate the proximity gap needs to be set.

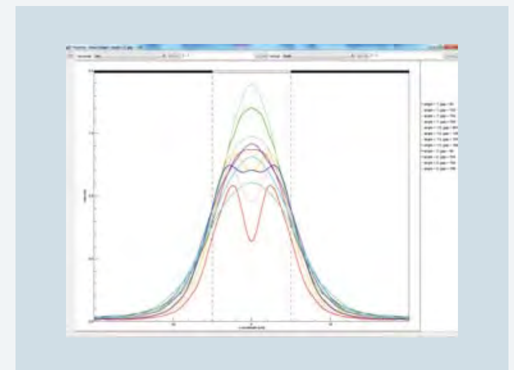


Figure 7. Overlay View (collapsed matrix view) for the same scenario

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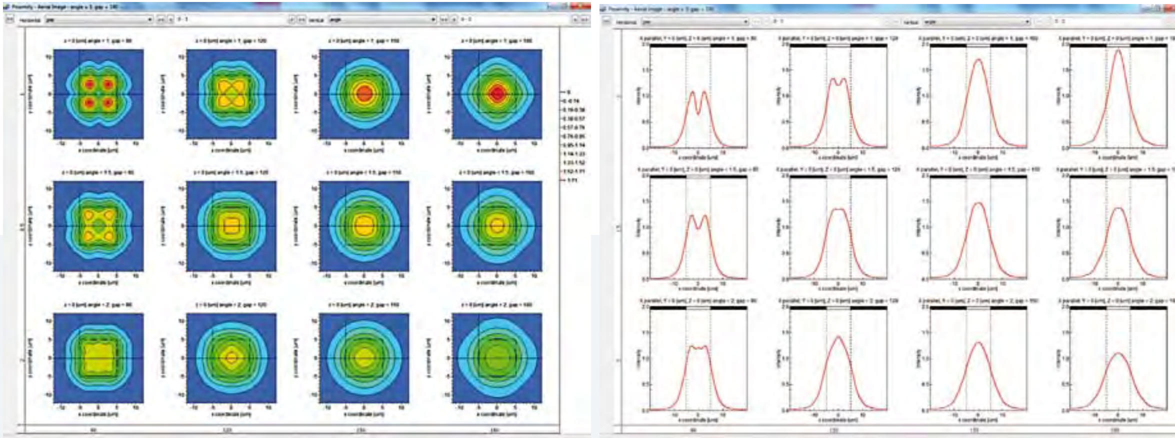

Figure 6. Matrix view for variation of 2 process parameters (gap and collimation angle) for a 15µm square to optimize the collimation angle for maximum proximity gap range

3. SUMMARY AND OUTLOOK

Lithography simulation enables the ability to transfer the benefits of mask aligners beyond the classical limits by resolution enhancement techniques such as layout optimization (OPC), source shaping, advanced mask technologies (grey-tone, phase shift), or combinations thereof such as source-mask-optimization.

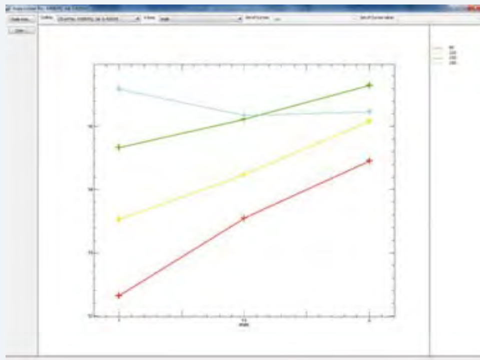

Figure 8. Analysis view showing the trends for the same process parameters gap and collimation angle.

Layout LAB is a dedicated simulation software including an accurate model for SUSS mask aligner, including the support of the new SUSS MO Exposure Optics. SUSS MicroTec is offering the simulation software Layout LAB to existing and new mask aligner user and provide in co-operation with GenISys training and support to apply the new technology to advance their products. GenISys and SUSS MicroTec will continue to enhance the combination of simulation, exposure tool and process in close cooperation with users, offering the highest value to the customer.

THE AUTHORS

As Vice President Marketing & Sales at GenISys GmbH in Munich, Germany, Nezih Unal is one of the company's key figures in creating unique solutions that make a difference. With over 25 years experience in various engineering and management positions in the semiconductor industry, Nezih worked on diverse technologies such as MEMS devices, optical lithography simulation software, and e-Beam lithography software.

Nezih Unal received his Diploma in Electronics Engineering at the University of Wuppertal in Germany in 1988, with a focus area on semiconductor technology. After his thesis on plasma and ion sources for micro-patterning processes he has started to work on the development of Reactive Ion Etching (RIE) processes for sub-micron IC manufacturing at Motorola. In 1992 he joined the new start-up microParts GmbH to develop and manufacture 3D MEMS devices using X-ray lithography (LIGA technology). Nezih joined SIGMA-C GmbH as director of Sales in 2003, and positioned the optical lithography simulation software SOLID as a strong #2 in the market. Early 2006, Nezih joined GenISys GmbH in his current role.

Ulrich Hofmann has more than 20 years experience in the semiconductor industry. Before founding GenISys, Ulrich worked in various technical and management positions on E-beam technologies as well as optical lithography technologies.

Ulrich Hofmann received his Diploma in Physics at the Technical University Munich in 1987. For the thesis in theoretical nuclear physics, he developed a new model on how to compute magnetic moments for nuclei. His first contact with the Semiconductor world was with Sigma-C in 1989, developing the first working hierarchy engine for E-beam lithography, data preparation and proximity effect correction, enabling full chip proximity effect correction on a single desktop computer. After joining Etec Systems in Hayward, CA in 1996, Ulrich pioneered technologies such as real-time proximity effect correction, hierarchical data processing, and ultra-high bandwidth datapath for massive parallel E-Beam direct write, and later became responsible for the commercial development and factory integration of the RSB next generation mask lithography tool. In 2005, he founded GenISys GmbH, a software house providing solutions for the optimization of microstructure fabrication processes for R&D, semiconductor manufacturers and equipment suppliers throughout the world.

Michael Hornung is Technical Marketing Manager at SUSS MicroTec Lithography based in Garching, Germany. During his career at SUSS MicroTec he passed further functions. So he was project manager in R&D responsible for the (nano) imprint technology and other new technologies for mask aligners. He also worked as application engineer for a while and lead the application group at SUSS MicroTec for two years.

Before he joined SUSS MicroTec he was project manager at CERN in Geneva, Switzerland, working at the inner detector for the ATLAS project.

Michael Hornung holds a Ph.D. degree in Natural Science from the University of Freiburg, Germany and an MBA from the University of Applied Science of Ludwigsburg, Germany.

ADVANCED MASK ALIGNER LITHOGRAPHY (AMALITH)

Reinhard Voelkel, Uwe Vogler, Arianna Bramati, Tina Weichelt SUSS MicroOptics SA, Jaquet-Droz 7, Neuchâtel CH-2000, Switzerland
Nezih Ünal, Ulrich Hofmann GenISys GmbH, Eschenstr. 66, 88024 Taufkirchen, Germany

ABSTRACT

Starting in the early 1960s, mask aligners were the dominating lithography tool for the first 20 years of the semiconductor industry. In the early 1980s industry changed over to projection lithography. However, mask aligners were never sorted out. Still today hundreds of new mask aligners are sold each year. This continuing success of mask aligner lithography is related to two basic trends in lithography: (a) Costs for leading-edge lithography tools double approximately every 4.4 years; and (b) the number of lithography steps per wafer was increasing from a few litho-layers to more than 35 layers now. This explains why mask aligner lithography, a very robust and cost-effective solution for uncritical litho-layers, is still widely used today. Mask aligner systems have much evolved, from manual 1" aligner to fully automatic 300 mm cluster systems of today. Interestingly, the shadow-printing lithography process itself was never improved. Illumination systems of most commercially available mask aligners are still based on technology developed in the 1970s.

SUSS MicroTec has now introduced a novel mask aligner illumination system, referred as MO Exposure Optics (MOEO)[1,2]. The MO Exposure Optics system is based on high-quality microlens arrays in Fused Silica. MO Exposure Optics stabilizes the illumination against misalignment of the lamp, provides improved light uniformity, telecentric illumination and allows freely shaping the angular spectrum of the illumination light. Full control and light shaping are the key to optimize mask aligner lithography beyond today's limits.
SUSS MicroTec and GenISys now provide Layout LAB, a lithography simulation software designed for full 3D simulation of proximity lithography in mask aligners[3]. Layout LAB allows the optimization of critical lithography steps, to improve resist pattern fidelity and helps to save costs in process development and to significantly improve the yield in production. Illumination control also opens the door to a new era of Advanced Mask Aligner Lithography (AMALITH), comprising Front-End-of-Line (FEOL) lithography techniques like Customized Illumination (CI), Optical Proximity Correction (OPC), Phase Shift Masks (AAPSM), Source Mask Optimization (SMO) as well as unconventional approaches like Talbot, Pinhole-Talbot, Grey-Level Lithography and more sophisticated wave front shaping techniques[4].

MASK ALIGNER, A SUCCESS STORY FOR 50 YEARS

Jean Hoerni's revolutionary "planar process", invented in 1957 and transferred to mass production at Fairchild Semiconductor in 1959, set out the technology path that semiconductor industry still uses today. Hoerni's planar process used optical lithographic techniques to partially protect a silicon substrate, to diffuse the base of a transistor into the collector and then diffuse the emitter into the base. Hoerni's planar process allowed for the manufacture of many transistors side-by-side on a planar Silicon substrate or "wafer". These wafers were micro-structured by using photosensitive resist, light exposure through photographic "mask" and chemical development. Hoerni's 3 to 4 masking steps required an alignment of a mask versus a previously structured pattern, a "mask alignment". The planar process was soon licensed to other companies and revolutionized the semiconductor industry. In the early days of the „integrated circuit

explosion“, the chip makers had to develop their manufacturing equipment on their own. But soon, the rapidly growing industry triggered a large request for manufacturing and testing equipment. The first semiconductor equipment manufacturer appeared on the scene and started to build mask aligners for 1” wafers.

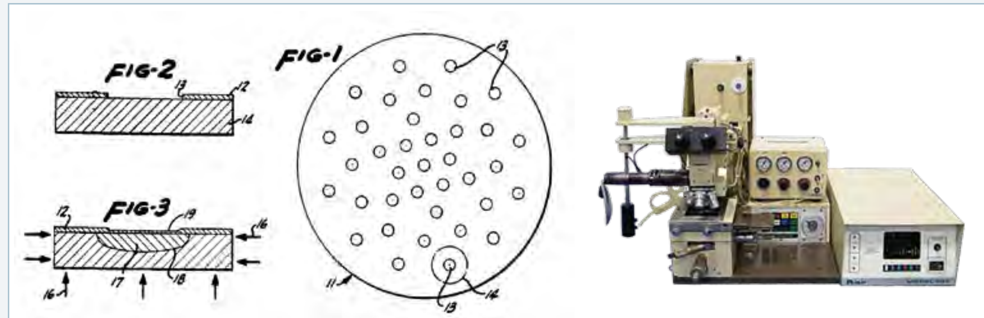

Figure 1. (left) Schematic drawing of a wafer having removed the masking layer within circles, taken from Jean A. Hoerni's famous patent US 3,064,167, filed in 1957; (right) Karl Süss MJB3 manual contact mask aligner.

In 1962 Karl Süss, local sales representative for Leitz Microscopes in Southern Germany since 1949, was approached by Hans Rebstock from Siemens Munich to build equipment for their IC development department. Beside microscopes, Leitz also offered precise translation stages, large substrate illumination systems and other useful parts which were used by Karl Süss and his technician Hans Fieser to build first prototypes of a mask aligner, a wirebonder and a prober for Siemens. Traveling frequently to the US, Ekkehard Süss, the elder son of Karl Süss, got in contact with Fred Kulicke from Kulicke & Soffa (K&S). Ekkehard Süss negotiated an agreement with K&S to distribute their mask aligners in Europe and quickly stopped the mask aligner development. A few years later, when K&S phased out their manufacturing of mask aligners, the Karl Süss KG had to re-start building mask aligners. Winfried Süss, the younger son of Karl Süss, joined the company and conducted the development of the MJB3 mask aligner. More than 2000 systems of the manual MJB3 mask aligner have been sold since then, until the MJB3 was finally replaced by the MJB4 in 2004.

Projection lithography pushed mask aligner lithography out of semiconductor front-end in the early 1980s. However, mask aligner lithography was never phased-out. The installed mask aligners remained in operation for less critical layers. The semiconductor Back-End-of-Line (BEOL), Advanced Packaging, MEMS, TSV for 3D-IC, and - most recently the very cost-sensitive LED manufacturing - maintained a continuous demand for some hundreds of new mask aligners installed every year in industry. Mature and robust technology, high throughput, ease of operation, low maintenance, moderate capital costs, attractive cost-of-ownership (COO) and low Cost-per-Litho-Layer are the key factors.

MO EXPOSURE OPTICS®

Over 50 years, the mask aligner systems have changed tremendously. Semiconductor manufacturing moved from 1” wafer size to 2” in 1969, to 3” in 1972, to 4” in 1976, to 6” in 1983, to 200 mm in 1993 and finally to 300 mm in 1998. Starting from a manual table-top exposure tool equipped with a single alignment microscope; the mask aligners have evolved to fully automatic cluster systems, providing a throughput of more than 150 wafers per hour. However, only little effort was undertaken to improve the shadow printing process itself. The illumination optics of modern mask aligners still looks very similar to the optics developed for first proximity aligners in the 1970s. Just recently, SUSS MicroTec has introduced a novel illumination system, the MO Exposure Optics. The new optics is based on two Köhler integrators consisting of double-sided microlens arrays. These high-quality microlens arrays are manufactured by SUSS MicroOptics exclusively for SUSS Mask Aligners and have been well optimized for mask aligner illumination. The two-stage homogenization of MO Exposure Optics is a novel illumination concept (patent pending). MO Exposure

Optics improves the light uniformity, provides telecentric illumination and the freedom of freely shaping the angular spectrum of the illumination light. For more details about the optical concept behind the MO Exposure Optics illumination system please review related publications[1,2,4] and the SUSS report from Dec 2010.

The most important benefits of the new MO Exposure Optics are

+ stabilization of the illumination against misalignment of the lamp,
+ improved light uniformity and telecentric illumination;
+ optimization of the angular spectrum of the illumination light to reduce diffraction effects;
+ and the possibility to use lithography enhancement techniques like Customized Illumination (CI), Optical Proximity Correction (OPC), Talbot-Lithography, Phase Shift Masks (AAPSM) and Source Mask Optimization (SMO) in mask aligners.

Since the market introduction more than 70 MO Exposure Optics systems have been installed in SUSS Mask Aligners worldwide. Yield improvement and cost savings have been so significant, that beta-customers have already completely upgraded production fabs to the new technology. Advanced Mask Aligner Lithography (AMALITH) research teams have been formed at universities and research centers.

PROXIMITY LITHOGRAPHY IS LIMITED BY DIFFRACTION EFFECTS AT THE PHOTOMASK

The performance of mask aligner lithography is determined by two parameters: Resolution also referred to as minimum critical dimension (CD), and overlay. Resolution is defined to be the minimum feature size that can be transferred with high fidelity to a resist layer on a wafer. Overlay is a measure of how accurately patterns on successive masks can be aligned or overlaid with respect to previously defined patterns on the same wafer. The resolution in shadow printing lithography is limited by diffraction effects. Submicron resolution is achieved for vacuum contact, where the air in-between mask and wafer is evacuated. For vacuum contact lithography, very tight requirements regarding flatness and cleanliness apply. Any remaining particle will increase the mask-to-wafer distance and will deteriorate the printing results. In production environment, with the demand for low costs and high throughput, proximity lithography is used. Here wafer and mask are separated by some 30 to 200 microns proximity gap. The achievable resolution decreases with increasing proximity gap due to diffraction[5]. As already proposed by Abbe, diffraction effects like side lobes, higher orders and interference effects could be altered by spatial filtering of the illumination light, changing both the angular spectrum and the spatial coherence properties of the illumination light. In projection lithography, a spatial filtering of the illumination light is referred as “customized illumination” and a well-established resolution enhancement technology (RET). MO Exposure Optics now offers a quick and easy change of the angular spectrum of the illumination light. Exchangeable illumination filter plates (IFP) allow altering the angular spectrum and the coherence properties of the mask illuminating light in the mask aligner[6].

CUSTOMIZED ILLUMINATION

Figure 2 a) shows schematically a simple lithography model for the use of MO Exposure Optics for proximity lithography[4]. The photomask is assumed to have a single square opening similar to a pinhole. Thus, the lithography system is reduced to three planes: The illumination filter plane, defining the angular spectrum, the mask plane and the wafer plane, where the resulting aerial image is recorded in photoresist. In this simple model, the opening of the photomask acts like a pinhole camera and images the illumination filter pattern onto the photoresist. As shown schematically in Figure 2 b) the illumination

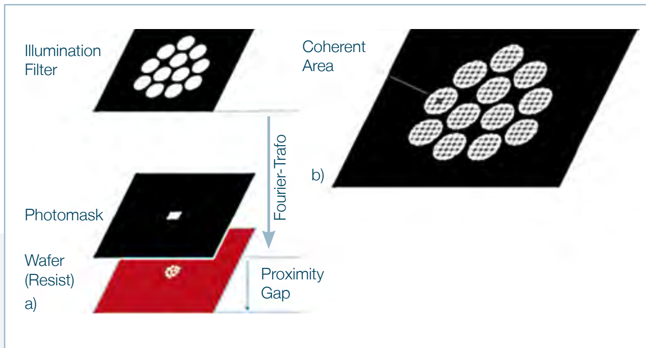

Figure 2. Simplified lithography model for the use of MO Exposure Optics in proximity lithography introduced by Stürzebecher[4]. (a) For a single opening in the mask the illumination filter pattern is imaged to the wafer plane. (b) The illumination filter plane is assumed to be subdivided in a multitude of coherent areas, where each is considered to be an ideal coherent source, but no coherence between different areas is assumed. The geometry of the illumination filter plate defines which of the coherent areas are transmitted and can contribute to the mask illumination.

filter plane is assumed to be subdivided in a multitude of coherent areas, where each is considered to be an ideal coherent source, but no coherence between different areas is assumed.

The geometry of the illumination filter plate defines which of the coherent areas are transmitted and which areas contribute to the mask illumination. In this simplified model, the optical system performs a Fourier transformation from the illumination filter to the mask. Thus, every coherent area in the illumination filter plane is creating a tilted plane wave while the tilt corresponds to the position of the considered area in the filter plane. Each of these plane waves is coherent, but different waves are incoherent to each other. The mask aligner is considered to be a device which is creating a set of non-interacting plane waves in which the composition of angular components is selected by choice of the illumination filter plate. This simple model is useful to predict the resulting aerial image and to optimize the illumination to improve resolution and fidelity of the resist prints[4].

OPTICAL PROXIMITY CORRECTION (OPC) AND SOURCE-MASK OPTIMIZATION (SMO)

Optical proximity correction (OPC) is a resolution enhancement technology (RET) commonly used to compensate for errors and irregularities like corner rounding, line width narrowing and edge shortening. Optical proximity correction corrects these errors by moving edges or adding extra polygons to the photomask pattern. If both customized illumination and optical proximity correction are used this is referred as source-mask optimization (SMO). Primary goals are enhanced CD control, increased resolution and depth of focus, improvement of the manufacturability for critical lithography steps and enlargement of the process window. Source-mask optimization allows pre-compensating print errors due to diffraction and process effects. MO Exposure Optics and source-mask optimization technology have a strong impact on process window enlargement and yield improvement in production environment.

LAYOUT LAB - SIMULATION TOOL FOR ADVANCED MASK ALIGNER LITHOGRAPHY (AMALITH)

Layout LAB from GenISys[3] provides full 3D simulation for proximity lithography processes. Simulation shortens the development cycle, enables Design For Manufacturing (DFM) to save costs on process development and allows for pushing mask aligner lithography beyond its current limits. This “ease-of-use” software, geared towards casual users as well as power users is capable of modeling the illumination of a broadband source and the different illumination types of SUSS Mask Aligners, including the capability to model the new MO Exposure Optics with arbitrary illumination filter plate (IFP) designs. It rapidly calculates the intensity image for arbitrary mask layouts (including grey-tone and phase-shift) at any proximity gap. The reflections and absorption of the light in the wafer stack is accurately modeled, resulting in a 3D intensity image in the resist. The calculated intensity image allows the optimization of IFP design and mask layout in combination, without high expenses for photomasks and experimental wafer exposure series.

Improving proximity lithography is of much interest for all production-related mask aligner processes. For large wafer sizes like 200 mm and 300 mm and high volume production a proximity gap of $\geq$30 µm is needed to avoid any contact of mask and wafer. This proximity gap of 30 µm

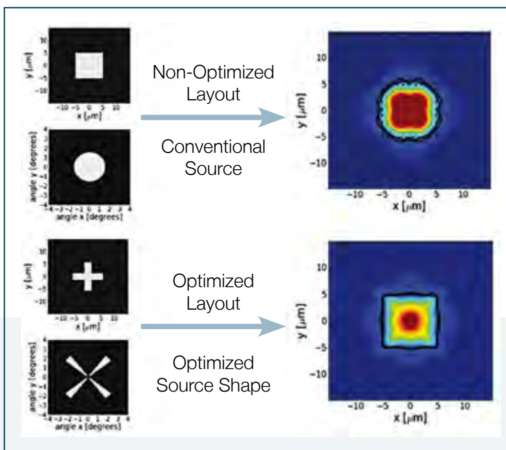

Figure 3. Simulation of a 10µm square exposed at a gap of 50µm. The simulation of the non-optimized mask layout with a conventional source shape shows that the intensity image at 40-50µm gap is distorted. Optimization of mask layout (cross) and the source shape results in a better figure fidelity to the square shape over the gap range.

limits the obtainable resolution to some 3µm, a severe limitation which had driven mask aligner lithography out of the semiconductor front-end in the early 1980s.

Figure 3 shows that the fidelity of a square-type mask pattern with 10 µm features to be printed at a proximity gap of 50 µm could be improved by optimizing the mask layout and the illumination shape (IFP design) in combination.

Without simulation it would not be intuitive that the cross mask layout combined with a 45° rotated cross-like IFP design results in a perfect square.

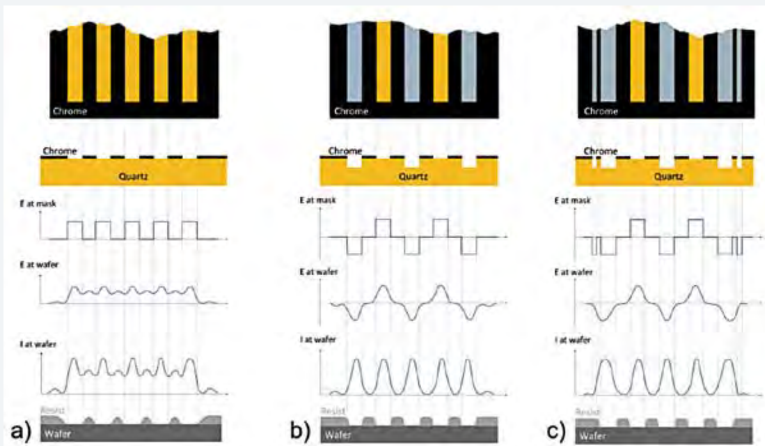

Figure 4. Three different types of photomasks: a) binary photomask, b) alternating aperture phase-shift mask (blue: additional phase step), and c) alternating aperture phase-shift mask (AAPSM) with additional OPC scattering bar.

Layout LAB also includes the 3D modeling of the resist development process. Please see the article “Simulation for Advanced Mask Aligner Lithography” in this SUSS report for more details on the simulation software Layout LAB and its application.

ALTERNATING APERTURE PHASE SHIFT MASKS (AAPSM)

In a next step phase shift masks (PSM) were examined for resolution enhancement. Figure 4 a) shows a binary photomask, where light is either reflected and just partially absorbed by the chromium layer (black) or passes openings (yellow). The shadow pattern at a certain distance behind the mask is affected by diffraction and interference effects. Light also propagates in the dark areas and bright areas are darkened partially.

For alternating aperture phase shift masks (AAPSM), shown in 4 b) and c), a phase step (blue) is added to the binary mask structure. Light passing the glass and phase step openings are shifted in phase by 180° versus each other. As shown in 4 b), this phase shift improves the contrast for proximity lithography significantly. 4 c) shows an alternating aperture phase-shift mask (AAPSM) with additional OPC scattering bars. The additional OPC scattering bar corrects the intensity, width and position of the outer lines. OPC correction of line-end shortening is also possible, but was not applied for this evaluation.

A five-bar pattern was printed in 1 µm thick AZ1512 resist at 30 µm proximity gap (365 nm wavelength) for verification of the simulation results. Figure 5 a) - c) shows a similar 2 µm (half-pitch) five-bar pattern printed at 30 µm proximity distance. For Figure 5 a) using a standard binary photomasks, only 4 instead of 5 lines are observed (reversal of image contrast), the pattern is not resolved. For the AAPSM shown in Figure 5 b) the pattern is resolved, however, the outer lines are not exposed with a similar dose and remain

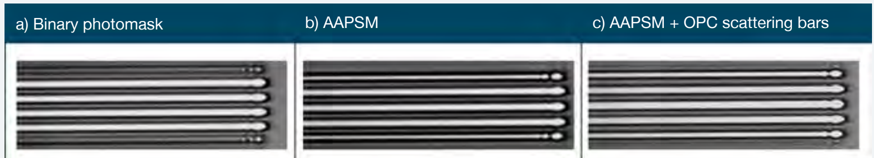

Figure 5. Prints in photoresist for a 2 µm (half-pitch) five-bar pattern printed at 30 µm proximity gap using three different types of photomasks as defined in Figure 4: a) the pattern is not resolved with a binary mask, b) a phase-shift mask (AAPSM) allows to resolve the pattern, c) additional OPC scattering bars allow to correct intensity, width and position of the outer lines. No correction of line-end shortening had been applied.

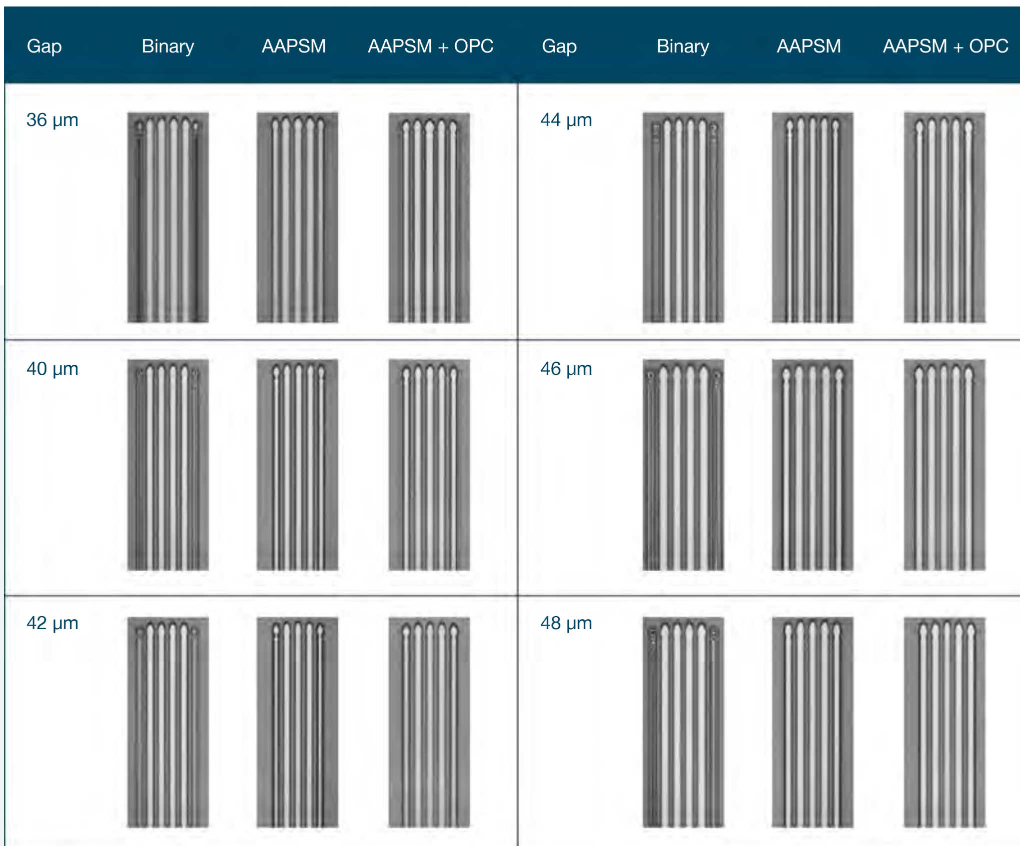

Figure 6. Prints in photoresist for 2 µm openings (lines & space pattern) similar to , but at different proximity gaps. The prints from the alternating aperture phase shift mask (AAPSM) with OPC scattering bars demonstrates a resolution of 2 µm for a proximity range of operation from 30 µm (see f) to 48 µm.

smaller. This remaining error is solved by adding OPC scattering bars shown in Figure 5 c).

Figure 6 shows photoresist prints (1 µm thick AZ1512 resist, 365 nm) for the three different photomask (similar to Figure 4 and 5), but at different proximity distances behind the mask. The prints from the alternating aperture phase shift mask (AAPSM) with OPC scattering bars show a resolution of 2 µm (half-pitch) for a proximity distance from 30 µm up to 48 µm. Simulation and experiment proofed that AAPSM and OPC allow enhancing the resolution at proximity lithography. In practice, special care has to be taken in OPC algorithms for mask aligners to generate layouts with manageable manufacturing and inspection costs.

COSTS PER LITHOGRAPHY LAYER

Although semiconductor industry changed over from mask aligners to projection steppers/scanners in the early 1980s, mask aligners were never sorted out. Still today some hundreds of new mask aligners are sold each year. This continuing success of mask aligner lithography is due to two basic trends in lithography:

(a) Costs for leading-edge lithography tools double approximately every 4.4 years; and

(b) the number of lithography steps per wafer was increasing from a few litho-layers to more than 35 layers now. This explains why the mask aligner, a mature, very cost-effective and robust solution for uncritical litho-layers, is still widely used today.

As shown schematically in Figure 7, the costs for mask aligner lithography for uncritical layers (>5 µm resolution) are typically 3x lower than in a low-cost stepper and about 5x lower than in a wafer stepper from front-end. Mask aligner lithography achieves high yield in production, similar to a front-end lithography processes and typically CD uniformity (CDU) is not even monitored for cost reasons. In practice, the situation is often less favorable. Scientists and engineers always test the limits. The constant demand for higher resolution for a next generation of a device forces process engineers to constantly improve resolution and overlay. As shown schematically in Figure 7, already a resolution of 4 µm is related to higher costs, usually provoked by the lower yield. For 200 mm or 300 mm wafers in a production environment it is not trivial to maintain a constant and accurate gap over the full wafer, and a gap mismatch is getting more critical if the structures are close to the resolution

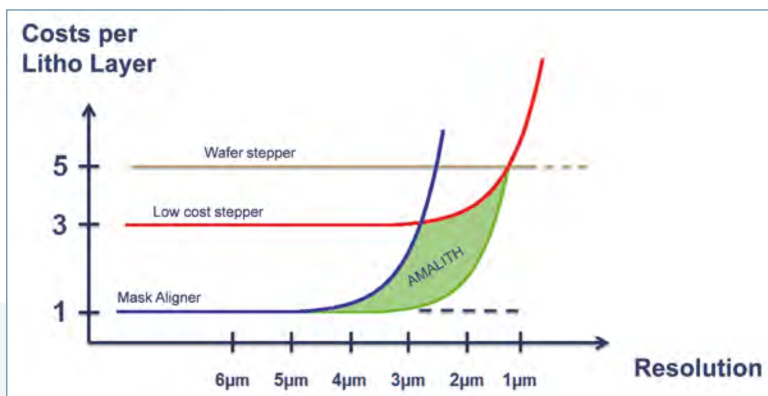

Figure 7. Scheme for the costs per lithography layer for mask aligners (proximity lithography), low-cost steppers and high-resolution wafer steppers related to the required resolution. Costs per layer increase if the technology is reaching its resolution limits due to yield problems. Advanced Mask Aligner Lithography (AMALITH) allows to push the resolution limits, to increase yield of established but critical processes and to compete with low-costs wafer steppers.

limit of 3 µm at 30 µm proximity gap. If mask aligners can't handle it anymore, a painful and cost intensive switch to higher-resolution projection lithography is required. High investment costs, new process development, and higher costs per litho-layer are the price. Often, a switch to projection lithography is not possible at all. Especially for very thick resist layers, the limited depth-of-focus (DoF) of a projection system is not sufficient. As a consequence, the process engineers try to optimize mask aligner lithography to the very limit. The process window is narrowing and the lithography steps become critical and relevant for the overall yield.

Astonishingly, this unfortunate situation is tolerated, at least as long as the costs for a technology switch are higher than the costs introduced by a lower yield. MO Exposure Optics and Advanced Mask Aligner Lithography (AMALITH) now offer a unique chance to significantly improve resolution and yield for established but critical processes in production. After 30 years of standstill with no roadmap for resolution and quality improvement, it is possible to push mask aligner lithography beyond today's limits. MO Exposure Optics is available for all generations of SUSS MicroTec mask aligners.

CONCLUSION AND OUTLOOK

The shadow printing lithography process in a mask aligner has not improved since mask aligners were moved out of front-end lithography in the early 1980s. Still today, contact-less proximity lithography in a mask aligner is limited to some 3 µm resolution for 30 µm proximity gap. Recently, a novel illumination system for mask aligners, referred as MO Exposure Optics, has been introduced. The MO Exposure Optics consists of two microlens based Köhler integrators, providing excellent uniformity of both intensity and angular spectrum of the illumination light. MO Exposure Optics uncouples the light from misalignment and lateral instabilities of the lamp. MO Exposure Optics allows implementing resolution enhancement technology (RET) known from front-end projection lithography, like, customized illumination, optical proximity correction (OPC) and source-mask optimization (SMO) in mask aligner lithography. Layout LAB proved to be a powerful simulation tool for mask aligner lithography. Resolution enhancement by using AAPSM and OPC scattering bars was demonstrated. The results show the high potential to improve mask aligner lithography beyond today's limits. The presented approach for lithography and resolution enhancement in mask aligners will have much impact on yield and costs in production. This new era of mask aligner lithography is referred as Advanced Mask Aligner Lithography (AMALITH).

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THE AUTHORS

Dr. Reinhard Voelkel
Diploma (1989) and PhD (1994) in Physics at University of Erlangen, Germany, working with Prof. Adolf W. Lohmann and Prof. Johannes Schwider
Post-Doc/Scientist at Institute of MicroTechnology in Neuchatel, Switzerland, working with Prof. Rene Dandliker and Prof. Hans Peter Herzig (1994-1999).
Co-founder and CEO of SUSS MicroOptics SA, Neuchatel, Switzerland, since then.
More than 25 years of experience in Optics, Micro-Optics, Optical Communication, Imaging Systems, Microtechnology and Semiconductor Manufacturing Technology.
Technical: Diffractive, Refractive and Hybrid Optical Elements, Microlens Arrays, Optical Design, Optical Interconnections, Fiber Optics, Optical Bio-Chips, Chemical Micro-Chips, Optical Sensors, Metrology, MEMS, MOEMS, Miniaturized Cameras, Ultra-Flat Cameras, Wafer-Level Cameras, Wafer-Level Packaging, Wafer-Based Micro-Fabrication, Photolithography.
Organization: General Management, Technology Management, Research & Development, Strategic Planning, Business Development, Project and Program Management, Relationship Development, Intellectual Property, Quality Assurance, Problem Resolution, Communications, Technical Publications and Presentations.

Uwe Vogler
After studying mechanical engineering at the Technical University Ilmenau, Germany, Uwe Vogler joined SUSS MicroOptics in 2009 as optical engineer. He has specialized on illumination systems and as Junior Product Manager has been responsible for the product line MO Exposure Optics since 2010.

Arianna Bramati
Bachelor (2008) and Master of Science (2010) in Physics Engineering at Politecnico of Milan in Italy with specialization in Micro-Nano Optics and Photonics Technologies.
After a brief experience in Industrial LASER applications and Optoelectronics for Biomedicine, she joined SUSS MicroOptics as Optical Engineer in 2010. Here she is mainly working on optical simulation of Proximity Lithography for Mask Aligner, MO Exposure Optics and AMALITH.

Tina Weichelt
Bachelor of Engineering in "Laser- & Optotechnology" at University of Applied Sciences, Jena, Germany in 2008
Master of Engineering in "Laser- & Optotechnology" at University of Applied Sciences, Jena, Germany in 2012
Internships at Schott Lithotec (2007), Carl Zeiss AG (2007) and University of Toronto, Canada, (2010), student assistant at Fraunhofer IOF (2009-2010), Master Thesis at SUSS MicroOptics SA, Neuchâtel, Switzerland (2011-2012)

Ulrich Hofmann has more than 20 years experience in the semiconductor industry. Before founding GenISys, Ulrich worked working in various technical and management positions on E-beam technologies as well as optical lithography technologies.
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As Vice President Marketing & Sales at GenISys GmbH in Munich, Germany, Nezih Unal is one of the company's key figures in creating unique solutions that make a difference. With over 25 years experience in various engineering and management positions in the semiconductor industry, Nezih worked on diverse technologies such as MEMS devices, optical lithography simulation software, and e-Beam lithography software.
Nezih Unal received his Diploma in Electronics Engineering at the University of Wuppertal in Germany in 1988, with a focus area on semiconductor technology. After his thesis on plasma and ion sources for micro-patterning processes he has started to work on the development of Reactive Ion Etching (RIE) processes for sub-micron IC manufacturing at Motorola. In 1992 he joined the new start-up microParts GmbH to develop and manufacture 3D MEMS devices using X-ray lithography (LIGA technology). Nezih joined SIGMA-C GmbH as director of Sales in 2003, and positioned the optical lithography simulation software SOLID as a strong #2 in the market. Early 2006, Nezih joined GenISys GmbH in his current role

ACKNOWLEDGEMENT

The authors would like to thank our colleagues and partners from SUSS MicroTec, Fraunhofer IOF, Fraunhofer IISB, CSEM Neuchâtel, EPFL Neuchâtel, Fachhochschule Jena, GenISys and Toppan Photomask for their valuable contribution and support. The presented work was partially financed by the Bavarian Research Foundation, project MALS: "Mask Aligner Lithography Simulation"; by the EU FP7-ICT Integrated Project SEAL: "Semiconductor Equipment Assessment Leveraging Innovation", sub-project FISMA; Swiss CTI-project 13254 AMALITH: "Advanced Mask Aligner Lithography".

SUBSTRATE CONFORMAL IMPRINT LITHOGRAPHY OF FUNCTIONAL MATERIALS – REVIEW OF A BFS-PROJECT

R. Fader, H. Schmitt, M. Rommel, A.J. Bauer, L. Frey, Fraunhofer Institute for Integrated Systems and Device Technology (IISB), 91058 Erlangen, Germany
R. Ji, M. Hornung, SUSS MicroTec Lithography GmbH, 85748 Garching, Germany
M. Brehm, DELO Industrial Adhesives, 86949 Windach, Germany
M. Vogler, micro resist technology GmbH, 12555 Berlin, Germany

1. INTRODUCTION

Substrate conformal imprint lithography (SCIL) is an innovative full wafer scale nanoimprint technology[1]. This sub-micrometer patterning method uses flexible PDMS stamps for the structure transfer. Originally, SCIL technology was developed for the transfer of structures into sol gel materials which hardened via diffusion of solvents into the PDMS stamp material. The work of Ji et al.[2] showed the extension of SCIL to UV-enhanced SCIL (UV-SCIL). With this new option, UV curable materials can be used as resists for the SCIL-method.

For the further development of this powerful technology, SUSS MicroTec and the Fraunhofer Institute for Integrated Systems and Device Technology (IISB) initiated the project "Substrate Conformal Imprint Lithography of Functional Materials" (SILFUMA) which was funded by the "Bayerische Forschungsstiftung" (AZ-864-09). As associated partners, DELO Industrial Adhesives and micro resist technologies substantially supported and strengthened the project.

SILFUMA was divided into three main work packages. Purpose of the first work package was the evaluation of purely organic resists for UV-SCIL. Common resists for SCIL or UV-SCIL contain inorganic chemistry[2,3]. This fact limits their suitability for dry etching processes. Furthermore, all common resists for SCIL or UV-SCIL need long curing times (3min – 15min)[2,3]. The advantage of purely organic materials used as etching masks is that they are well suited for standard dry etching processes. As shown, another advantage of UV polymers for UV-SCIL is the significant reduction of curing time compared to commonly used resists. So, using UV curing polymers shortens the overall SCIL process time essentially.

The Second part of the project is aimed at simplified stamp manufacturing. The molding of the fragile PDMS stamps from master structures is a process with several complicated steps and needs an experienced operator. Even then, however, many stamp rejections are produced because most process steps can cause defects on the stamp. For an industrial application of SCIL, however, it is necessary to have a rather simple manufacturing process for the PDMS stamps which produce reproducible stamps without any defects. This in turn, requires practical manufacturing tools.

The objective of the third work package was the development of a functional resist material and the evaluation of a UV-SCIL process for such a material. A common structure transfer process uses a structured resist layer as etching mask for an etch process which transfers the structure into a substrate. With a functional resist material, however, the etch process step can be saved and a functional element can be produced directly by UV-SCIL. Therefore, the functional resist material already needs to have the properties

necessary for the functional element (e.g. electrical conductivity, permittivity or refractive index). For this purpose, different kinds of nano-particles (which should provide the functionality) were mixed with polymer matrix materials and the resulting functional resists were evaluated with regard to imprintability and functionality.

2. UV-SCIL WITH ORGANIC UV POLYMERS

For industrial applications, the long curing times of common resists for UV-SCIL[2,3] limit the possible throughput and their inorganic components restrict their suitability for dry etching processes. Using purely organic UV polymers with fast curing times would shorten the overall SCIL process time essentially, and thus enable much higher throughput. In addition, these polymers have the advantage that they are well suited for standard dry etching processes in semiconductor technology. Also, many well-known processes from classical photo lithography with organic photo resists suit for further processing of substrates.

UV-SCIL EMULATION ON NPS 300

For first investigations on promising UV-curing polymers for UV-SCIL, the UV-SCIL process was emulated on a NPS 300 nanoimprint stepper. This emulation of the UV-SCIL process was necessary to be able to test many different polymers without spin coating them and in order to save costs for PDMS stamps. For that, stamp pieces with a size of 1cm² were prepared out of the wafer size PDMS stamps. With these small PDMS stamp pieces, imprints into several different manually dispensed UV-curing polymers were performed. The interaction between UV-curing polymers, silicon substrates, and PDMS were analyzed to assess well suitable polymers for UV-SCIL.

The results of those experiments are summarized in Table 1. They show that most of the investigated materials are not suitable for UV-SCIL. For example, some materials have a very strong adhesion to the PDMS stamp after the UV-curing. Other materials could not cure during the contact with the PDMS stamp because of oxygen inhibition[4]: Oxygen diffused from the atmosphere into the PDMS material inhibits the curing of most acrylate based polymers. Only two of the evaluated polymers exhibited suitable properties for UV-SCIL, i.e., mr-UVCur06 and DELO Katiobond OM VE 110707 (highlighted in Table 1). Thus, in the following all required process steps for their use as UV-SCIL resists were developed only for these two polymers.

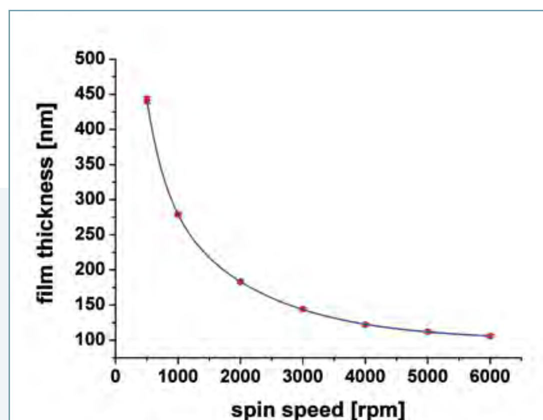

Figure 1. Spin speed curve for Katiobond OM VE 110707 diluted with 83wt% cyclo-pentanone

SPIN COATING

The deposition of the two most promising polymers (i.e. Katiobond OM VE 110707 and mr-UVCur06) on 100mm silicon wafers was realized by spin coating on the wafer. A manual coating system was used for the material deposition. For mr-UVCur06, a well-known coating process from micro resist technologies was used[5] and for Katiobond OM VE 110707 the coating process was developed within this project. For this spin coating process, Katiobond OM VE 110707 was diluted with cyclopentanone. After that surface conditioning of the silicon substrates, spin coating parameters for a manual coating system, and post coating proces-

Name of tested UV-curing polymer	Polymer base	Imprint result
NOA 61; Norland Products	Acrylates	Weak substrate adhesion
NOA 84, Norland Products	Acrylates	Curing not possible
NOA 89, Norland Products	Acrylates	No substrate adhesion
mr-UVCur21SF, micro resist technologies	Acrylates	Curing not possible
mr-UVCur06, micro resist technologies	Acrylates	Homogeneous imprint
Photobond OM VE 512494, DELO Industrial Adhesives	Acrylates	Curing not possible
Photobond GB310, DELO Industrial Adhesives	Acrylates	Strong adhesion to PDMS stamps
Katiobond OM VE 110707, DELO Industrial Adhesives	Epoxides	Homogeneous imprint

Table 1. Tested UV-curing polymers for UV-SCIL with their polymer base and their imprint result with PDMS stamps

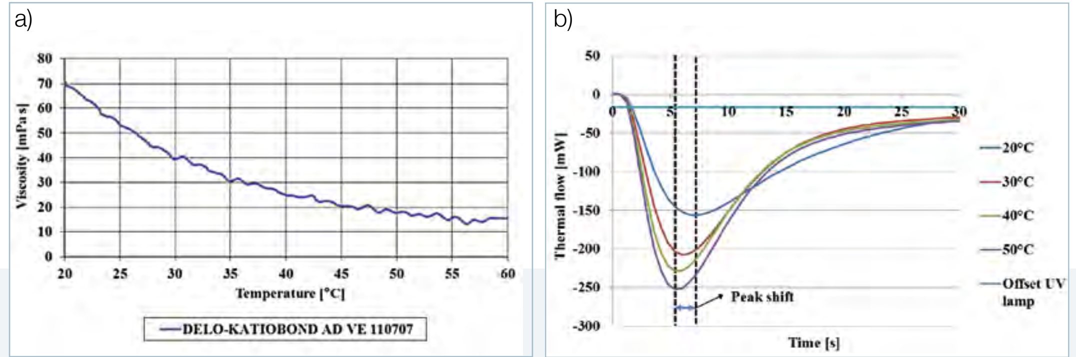

Figure 3. a) Viscosity of Katiobond OM VE 110707 at different temperatures and b) DSC measurement of the cross linking reaction

ses were evaluated. With the developed spin coating process for Katiobond OM VE 110707, film thicknesses from 50nm to 600nm with a standard deviation of 5nm can be achieved. Figure 1 shows a spin speed curve for Katiobond OM VE 110707 diluted with 83wt% cyclopentanone. The spin coating process for mr-UVCur06 uses mr-t 1070 from micro resist technologies as thinner[5]. With the process received from micro resist technologies, the film thicknesses of mr-UVcur06 can be adjusted homogeneously between 70nm and 500nm with a standard deviation of 5nm.

UV-SCIL IMPRINTING

The imprint processes were performed on a MA8/BA8 mask aligner with SCIL upgrade from SUSS MicroTec. The PDMS stamp used for these experiments contains a grating structure for resolution tests with feature sizes ranging from 100nm to 500nm. Figure 2a and Figure 2b show SEM cross section images of an imprinted line with mr-UVcur06 and with Katiobond OM VE 110707. Both imprints were performed with the same PDMS stamp. The comparison between Figure 2a) and Figure 2b) shows that the side walls of the line imprinted with Katiobond OM VE 110707 are much steeper than those of the line with mr-UVcur06.

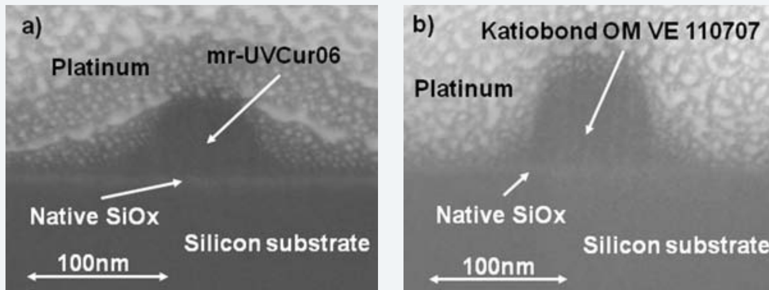

Figure 2a), b). SEM cross section images of an imprinted line with a) mr-UVCur06 and with b) Katiobond OM VE 110707, Platinum deposited for FIB cross sectioning

The exposure times were 17s for Katiobond OM VE 110707 and 3min for mrUVCur06. Compared to all commonly used resists the evaluated curing time for Katiobond OM VE 110707 is very short. The big difference between 17s for Katiobond OM VE 110707 and 3min for mrUVCur06 can be explained by oxygen inhibition of the polymerization of UV curing acrylates. The oxygen diffused in the porous PDMS stamp inhibits the polymerization reaction of the acrylate[4].

The curve of the viscosity measurement of Katiobond OM VE 110707 at different temperatures (Figure 3a) shows that the viscosity is reduced significantly at elevated temperatures compared to room temperature. The principle of UV-SCIL is based on capillary forces. These capillary forces increase with decreasing viscosity. Therefore, increased capillary forces accelerate the filling of structures in the PDMS stamp during the imprint process and, thus, the imprint speed can be increased. This faster imprint speed reduces the overall process time.

The differential scanning calorimetry (DSC) of the cross linking reaction of Katiobond OM VE 110707 at different temperatures indicates that the UV initiated reaction runs faster at elevated temperatures (Figure 3b). Therewith the exposure time at elevated temperatures can be shorter, which additionally reduces the overall process time. The imprint results with Katiobond OM VE110707 and the temperature dependent measurements led to the idea to further reduce the overall UV-SCIL process time by using an electrically heated chuck which then was designed

Chuck temperature	21°C (RT)	30°C	40°C
Exposure time	17 s	10 s	5 s
Imprint speed	3.5 mm/s	5 mm/s	8.3 mm/s
Delay before exposure	20 s	10 s	5 s
Delay after exposure	10 s	10 s	10 s
Separation speed	8.3 mm/s	8.3 mm/s	8.3 mm/s
Process gap	20 µm	20 µm	20 µm
Total process time for 180mm imprint area	**120.1 s**	**87.7 s**	**63.4 s**

Table 2: Evaluated UV-SCIL process times for Katiobond OM VE 110707 at different temperatures of the electrically heated chuck

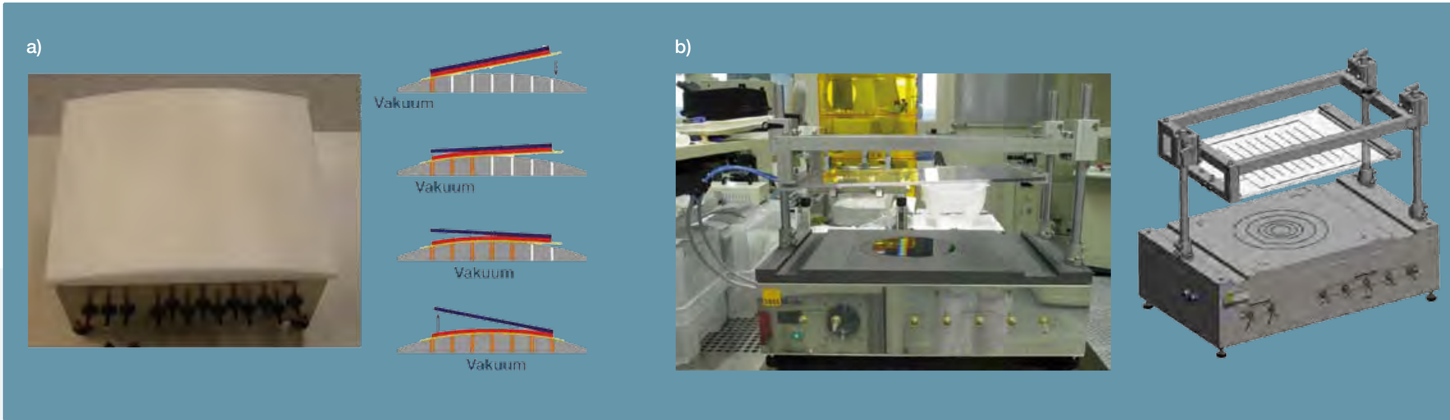

Figure 4a). Schematic drawing of the functionality of the first separation tool and b) pictures of the redesigned tool

by SUSS MicroTec within this project.
Table 2 compares the different UV-SCIL process times for Katiobond OM VE 110707 at different temperatures. It shows that if the temperature of the heated chuck is 40°C, the process time is half of the process time at room temperature because of a higher imprint speed and a shorter exposure time.

3. PDMS STAMP MANUFACTURING

In order to produce defect free PDMS stamps for an industrial application of SCIL it is necessary to have reliable and mature manufacturing tools and a stable manufacturing process. Within the project the tools were partly redesigned for improved usability. With these new tools a stable fabrication process could be achieved. The lifetime and the compatibility of the produced stamps with the Katiobond OM VE 110707 were finally tested with a new low cost method.

REPLICATION AND SEPARATION TOOL

Two different tools are used for the stamp manufacturing: the replication tool and the separation tool. With the replication tool the molding of the master structure is performed. The design of this tool was not changed within the project. Just a construction was added which allows dispensing the PDMS on the master wafer with strongly improved reproducibility.
The separation tool is required for the separation of the cured PDMS stamp with the glass carrier sheet from the master wafer. Figure 4a) shows a schematic drawing of the tool before the redesign. In principle it consisted out of a curved surface with vacuum grooves, where the bond out of PDMS stamp and master wafer was placed on top. By sequential switching of the vacuum grooves the wafer is separated from the stamp. The experimental work with this tool showed that the risk of breaking the stamp using this tool is rather high. Figure 4b) shows a picture of the newly designed separation tool. This tool consists out of a wafer chuck and an up and down movable flexible acrylic glass chuck above. The bond out of PDMS stamp and master wafer can be fixed between those two chucks, top side with PDMS stamp on the acrylic glass chuck and bottom side with the master wafer on the wafer chuck. By turning a screw the acrylic glass sheet can be bended round and the flexible PDMS stamp gets separated from the fixed stiff master wafer. With this new separation tool the risk of breaking stamps within this process step could be strongly reduced.

LIFETIME OF PDMS STAMPS

After the development of an optimized manufacturing process for PDMS stamps with the newly designed tools, the quality and the lifetime of the PDMS stamps were tested. Therefore, again the SCIL process was emulated on a NPS 300 nanoimprint stepper like described before in chapter 2. Here, the emulation was necessary to be able to perform many imprints (>1000) with one stamp in an automated cost effective way. Because of the small stamp size (1cm^2) more than 200 imprints could be performed on one 6inch substrate. The NPS 300 allows programming an automated process where all imprints on one substrate were performed without intervention of an operator. At the NPS 300, the stamp is separated at once from the hardened resist and not peeled off like in the normal UV-SCIL process. This means that there is a higher mechanical wear and the determined lifetime probably gives an underestimation of the lifetime of a real UV-SCIL stamp. The applied imprint resist for these experiments was Katiobond OM VE 110707.
Corresponding results are shown in Figure 5a), b) and c). The SEM pictures show structures in Katiobond OM VE 110707 transferred with the same PDMS stamp. After imprint no. 500

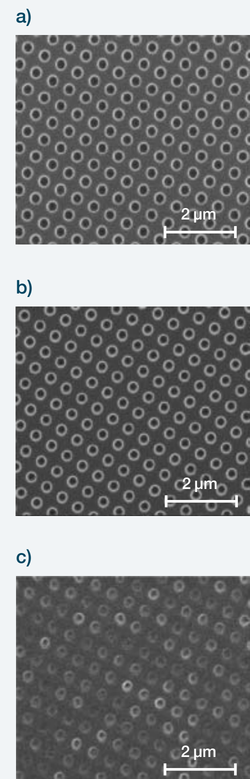

Figure 5. SEM pictures of imprinted patterns in Katiobond OM VE 110707 after a) 1st, b) 500th and c) 1000th imprint

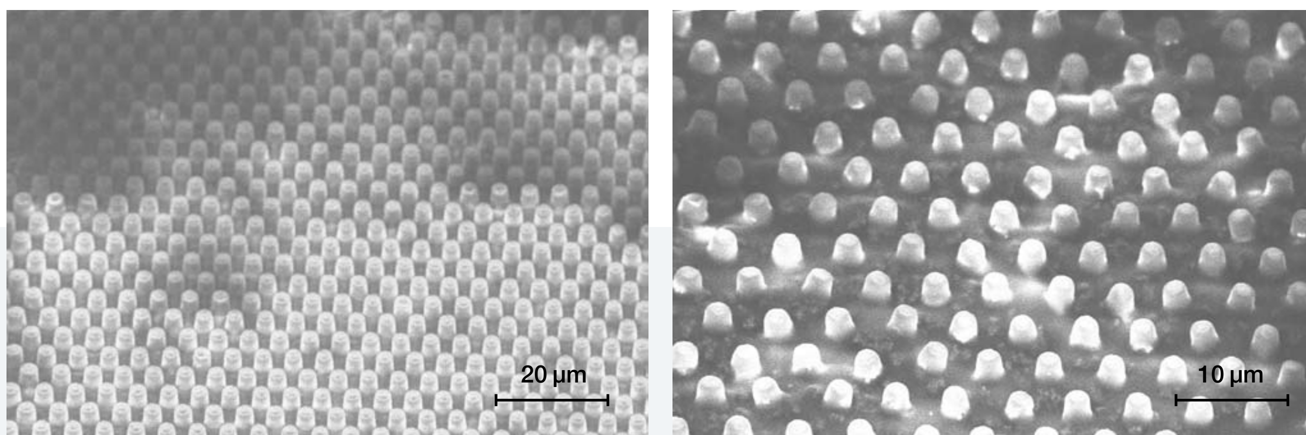

Figure 6. SEM pictures of pillar structures imprinted with UV-SCIL into a silver particle resist layer

(Figure 5b)), the structures are still well defined and no significant difference compared to the structures after the first imprint (Figure 5a)) can be detected. Compared to imprint no. 1, on the other hand, the structures after imprint no. 1000 (Figure 5c)) are weakly defined and diffuse. The PDMS stamp shows strong mechanical wear after 1000 imprints. In summary, these experiments show that minimum 500 imprints can be performed with the PDMS stamps for UV-SCIL.

4. FUNCTIONAL MATERIALS

For the design of functional resist materials for UV-SCIL different nanoparticles were mixed with UV polymers. Several different UV polymers served as matrix material for the nanoparticles. Two kinds of nanoparticles were investigated, silver particles and silicon dioxide particles. The silver particles were supposed to create a material with a certain electric conductivity. The functional resist composed out of silicon dioxide particles and a UV polymer could serve as a printable material for e.g. anti-reflection layers.

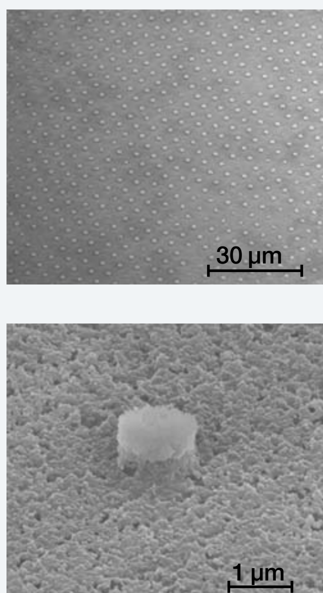

Figure 7. SEM pictures of pillar structures imprinted with UV-SCIL into a silicon dioxide particle resist layer

The first step for both materials was to disperse and to stabilize the particles in the polymer matrix. Therefore, many different dispersing methods were tested. Finally, the best results for both systems could be achieved with an ultrasonic finger. With this technique the application of energy into the particle-polymer-mixture was high enough to break agglomerated particles. The functional materials with homogenously dispersed nanoparticles are stable for some hours. The material deposition of both systems on different substrates was realized with developed spin coating processes.

FUNCTIONAL MATERIAL WITH SILVER PARTICLES

The specific resistance of the functional material was measured with the van der Pauw (vdP) method. Therefore, structures for vdP measurements were fabricated with nanoimprint lithography. After some post processing steps to remove the polymer matrix and to bake the particles together the measurements were performed. The lowest measured specific resistance was $1.8*10^{-5}\Omega*cm$. This value is in the same range as the specific resistance of commercially available silver inks treated with the same post process. In comparison, the specific resistance of bulk silver is $1.6*10^{-6}\Omega*cm$. As the size of the silver particles in the silver ink is of several micrometers, the inks cannot be used for the direct imprinting of functional elements in the micro- or even nanometer range. Figure 6 shows SEM pictures of pillar structures imprinted with UV-SCIL into a silver particle resist layer. The UV-SCIL process with the silver particle resist enables the transfer of structures in the µm range (<10µm). However, after the imprint, the PDMS stamps showed strong impurities. Residuals of the resist stuck on the PDMS surface of the stamp. Therewith, the stamps could only be used for one imprint with this material.

FUNCTIONAL MATERIAL WITH SILICON DIOXIDE PARTICLES

After testing different post processes for spin coated silicon dioxide particle containing resist layers SEM pictures showed that after an 1100°C annealing step the silicon dioxide particles form a compact layer. Annealing steps between 340°C and 900°C remove the polymer matrix and leave a porous fragile silicon dioxide

layer. Figure 7 shows SEM pictures of pillar structures imprinted with UV-SCIL into a silicon dioxide particle resist layer. Compared to the process with the silver resist, only little impurities were observed on the stamp after imprinting. These impurities can be removed by rinsing the stamp with 1% HF solution. With such silicon dioxide resist antireflection layers on e.g. solar cells can be fabricated by UV-SCIL without further complicated etch process steps or material deposition.

5. CONCLUSION

The SILFUMA project introduced for the first time two kinds of fully organic polymers for UV-SCIL, Katiobond OM VE 110707 and mr-UVCur06. Using these polymers for UV-SCIL, the exposure time and thus, the overall process time can be reduced essentially compared to all commonly used resists. Especially with Katiobond OM VE 110707 and an electrically heated chuck, the exposure time was reduced down to 5s. Additionally, the fully organic polymers are well suited for standard dry etching processes in silicon technology. Many well-known processes from classical photo lithography can be used for further processing of substrates.

Within this project the manufacturing process for PMDS stamps was strongly simplified and matured by reconstructed replication and separation tools. The risk of breaking stamps was strongly reduced using the redesigned tools. With a developed process, defect free stamps can be manufactured that have a lifetime of more than 500 imprints.

First experiments with two different functional materials showed that the direct imprinting of functional elements is possible. A functional resist for UV-SCIL with silver nanoparticles dispersed in a polymer matrix enables the direct imprinting of conductive elements. With a functional resist containing silicon dioxide particles, the direct imprinting of e.g. an antireflection layer is possible by UV-SCIL. Therewith, these resists enable new applications for UV-SCIL.

Acknowledgments

The authors gratefully acknowledge the financial support of the Bavarian Research Foundation (AZ-864-09).

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Robert Fader studied physics at the Friedrich-Alexander-University in Erlangen. After graduating in 2010, he continued doctoral research at the Fraunhofer Institute for Integrated Systems and Device Technology IISB in Erlangen in electrical engineering. Subject of his doctoral thesis is Substrate Conformal Imprint Lithography.

Holger Schmitt studied material science at the Friedrich-Alexander-University (FAU) in Erlangen. After graduating in 2004, he continued doctoral research at the "Chair of Electron Devices" at the FAU in Erlangen. He received his doctoral degree in 2008. The title of his doctoral thesis was "Investigation of the UV nanoimprint lithography as patterning technique for electron devices". Currently he is working for the BROSE Fahrzeugteile GmbH in Hallstadt.

Michael Hornung is Technical Marketing Manager at SUSS MicroTec Lithography based in Garching, Germany. During his career at SUSS MicroTec he passed further functions. So he was project manager in R&D responsible for the (nano) imprint technology and other new technologies for mask aligners. He also worked as application engineer for a while and leads the application group at SUSS MicroTec for two years. Before he joined SUSS MicroTec he was project manager at CERN in Geneva, Switzerland, working at the inner detector for the ATLAS project. Michael Hornung holds a Ph.D. degree in Natural Science from the University of Freiburg, Germany and an MBA from the University of Applied Science of Ludwigsburg, Germany.

REDUCTION OF PROXIMITY INDUCED CORNER ARTIFACTS BY SIMULATION SUPPORTED PROCESS OPTIMIZATION

Marc Hennemeyer, Volkan Cetin, Ar-chaow Pun-Utaiwat, Dietrich Tönnies
SUSS MicroTec Lithography GmbH, Schleissheimer Str. 90, 85748 Garching, Germany

ABSTRACT

Reducing proximity artifacts is the most common challenge occurring in mask aligner lithography especially when exposing substrates at larger proximity gaps. Typically, proximity artifacts are most prominent at positions where the symmetry of the structures that should be produced is broken, i.e. line ends or corners. The tests presented here focused on various process parameters expected to influence the occurrence of proximity induced corner artifacts, including geometrical design of the mask structures, as well as exposure optics, gap and dose. It could be shown, that the artifacts can greatly be reduced by a combined optimization of the parameters stated before.

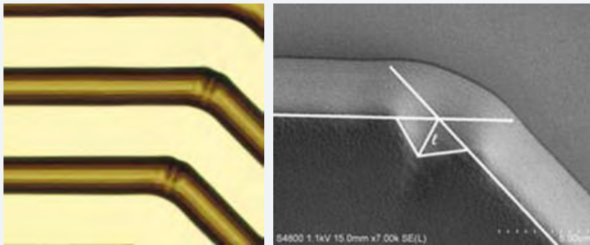

Figure 1. Optical microscopy image (left) of resist structures on top of a copper metallization. The resist structures serve as etch mask for producing conductor lines (bright: conductor path, dark resist structure). The resist structures at the inner corners of the conductor paths present a diffraction induced resist abrasion, visible as darkening in the resist lines, that reaches through the complete resist width. In the SEM image (right) it can clearly be seen, that the proximity artifact is strongest at the resist surface. The lines drawn into the SEM image illustrate the construction of the quantifying number ℓ that was used to control the influence of the process optimization. The drawn lines follow the strongest contrast along the main resist profile. Protrusions in the close vicinity of the eroded area were disregarded.

DESCRIPTION OF ISSUE AND DEFINITION OF TARGET OF THE STUDY

The process under investigation in this study worked on a 7 µm thick film of AZ P4620, but similar phenomena were reported in other resist film thicknesses and resists. The size of the features under observation was about 20 µm. Before the process optimization the wafer was exposed with Large Gap Optics (LGO) at an exposure gap of 50 µm. The exposure dose at the beginning of the study was reported to be around 800 mJ/cm², well above the dose recommended by the resist manufacturer.

Figure 1 illustrates the artifacts as observed in the baseline process. In the optical microscopy image the artifacts are clearly visible as darkening protruding into the resist (amber colored regions) at the inner corners of conductor paths (bright yellow area, i.e. regions free of resist). The artifacts reach far into the resist structure and even change the geometry of the conductor path. Also in the electron microscopy image on the right side the defect is clearly visible as a resist abrasion. As can be seen from the SEM image, the proximity artifact is the strongest at the resist surface. In the following the extent ℓ of the artifact at the resist surface will be used to quantify the defect.

DOE AND SIMULATION

To optimize the process the influence of a wide range of process parameters was investigated by process simulation and experiment. However, due to the amount of the performed tests not all results can be reported in full detail in this article. Therefore, the report will mainly focus on the three individual parameters exposure gap, exposure optics and exposure dose and on the parameter space of geometrical variations of the mask. The influence of soft baking conditions was investigated in the first part of the study. The influence of soft bake temperature T_{SB} and time t_{SB} were found to be of minor

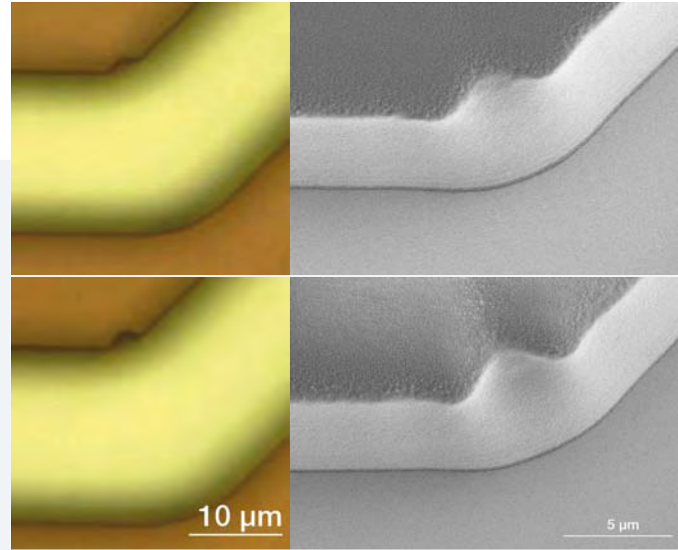

Figure 2. Optical (left) and electron (right) microscopy images of the corner artifact induced by a dose of 510 mJ/cm² (top) and 800 mJ/cm² (bottom). The erosion zone is larger with a higher dose

importance, as long as they were kept within a reasonable process window (90°C < T_{SB} < 110°C, 90 s < t_{SB} < 180 s). The film thickness variation caused by the varying baking conditions were tracked but could not be assigned as relevant influence on the results in the following tests. A byproduct of the test was the result that the development medium has a noticeable influence on the resist abrasion. The KOH based developer showed a reduced artifact in comparison to the TMAH based developer. However, as in most fabs TMAH based developers are used, the following tests focused on those.

Main parameters for the exposure process tests were the exposure gap, the optics configuration and geometrical variations of the mask design. Besides these three parameters the exposure dose was also assessed, as influence of the dose has to be expected. However, due to other process restrictions the dose of the process is not always adjustable at customer sites. The complete DOE performed in experiments spanned 168 parameter configurations. Additionally, geometrical variations were evaluated in simulation calculations. At this end the influence of line width, edge angles and the radius of corner roundings (fillets) were reviewed. A list of the varied parameters and the respective value range can be found in table 1.

For process simulation the software LayoutLab from GenISys GmbH was used. For a detailed introduction to this software please refer to the article “Simulation for Advanced Mask Aligner Lithography” in the same issue of the SUSSreport.

RESULTS

DOSE

Variation of dose had a clear influence on the length ℓ of the artifact area in the conductor path edges. As can be seen in Figure 2, the artifact area length was reduced by lowering the exposure dose.

Measurements resulted in a length of 5 µm when exposing the resist with 800 mJ/cm² and of 3.5 µm when exposing with 510 mJ/cm². In order to understand the underlying effects a threshold simulation was performed with the LayoutLab software. By performing a threshold simulation it is easily possible to compare the influence of relative dose changes on the exposure result even without a precise calibration of the used resist media and development process conditions.

Figure 3 shows the result of the simulation. The color coding represents the different doses that are reached in different areas of the simulated area, red showing the highest dose, blue the lowest. From the graphics it can be understood that the areas affected by the proximity artifact are exposed with significantly lower intensities than the main area of the conductor paths. An easy model for the behavior of photolithographic resists is that of a simple threshold, meaning that resist is either developed, if the threshold dose is reached, or stays on the wafer untouched, if the actual dose is smaller than the threshold. From this model it can be easily understood, that an increase in total dose will bring even areas with lower intensities over the threshold of the resist, worsen the proximity artifact in the structure corner, analogous to the changing shape of the iso-intensity-lines in the simulation.

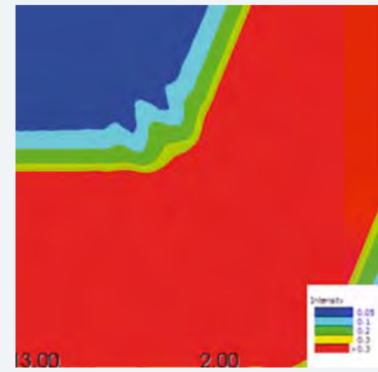

Figure 3. Iso-intensity-lines simulated for the same structure as in figure 2. The different colors represent areas exposed by at least the referenced intensity. Increasing exposure time, i.e. increasing doses, will lift the more corrugated areas of lower intensities over the dose threshold of the resist.

Parameter, Unit	T_{SB}, °C	t_{SB}, s	Dose, mJ/cm²	Gap, µm	Line width, µm	Fillet radius, µm	Corner angle, °C	Optics configuration
Min value	90	90	510	30	15	0	90	LGO
Max value	110	180	800	50	50	33	157.5	HR optics

Table 1: Parameters and their respective extremal values as used in experiments and simulation (middle blue). For most parameters more than 2 different values had to be used in the DOE due to the nonlinear response of the results on the input values.

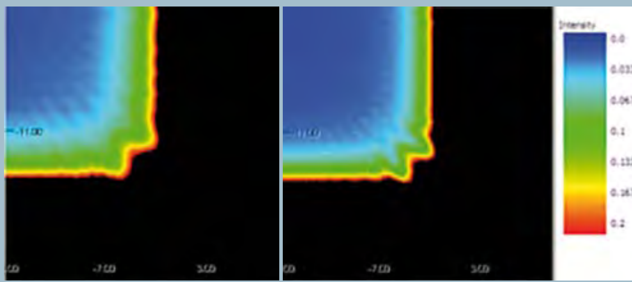

Figure 4. Images of the simulation results for a sharp 90°C corner. The left image represents the situation at 50 µm, the right image at 30 µm gap. In 50 µm gap the corrugation has a longer wavelength, a slightly bigger amplitude and a stronger attenuation.

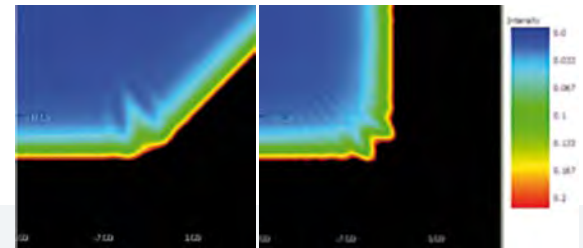

Figure 5. Images of the simulation results for a 90° C and a 135° C corner calculated for LGO optics and an exposure gap of 30 µm.

EXPOSURE GAP

Experiments to evaluate the influence of the exposure gap onto the size of the abrasion area were not conclusive in the range of exposure gaps relevant for the processes under examination. Whereas at higher doses an influence of the gap could not be excluded, at lower doses no significant influence could be observed in the experimental results. Also simulation calculations could not clearly prove an influence on the length of the artifact area. Figure 4 shows the result of the simulation for large gap optics. The figure represents simulation results for a 90° C sharp corner in 50 µm gap (left) and 30 µm gap (right).

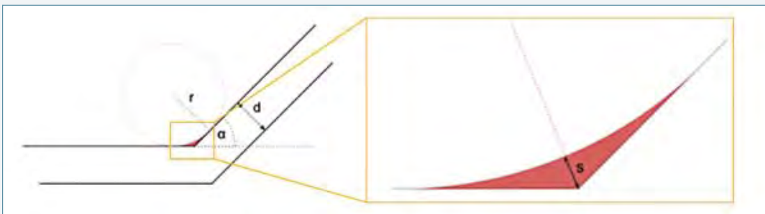

Figure 6. Schematic drawing of the geometrical parameters defining the fillet. With increasing radius r and decreasing corner angle the fillet distance s increases.

No decrease in length of the artifact area could be measured in the simulation results. Additionally, in the same time the artifact area widens. However, the level of the corrugation, i.e. the slope of the intensity at the edge as well as the ratio between corrugation period and depth was decreased by increasing the gap. Whether these results are beneficial for the actual process has to be decided on a case-by-case basis.

GEOMETRICAL VARIATIONS, LINE WIDTH, EDGE ANGLE AND FILLETS

The line width of the conductor paths was assessed in simulations only. For all line widths which were analyzed the simulation results predicted the same corner artifacts. This result can also intuitively be understood, as at line widths of 15 µm and more at the scrutinized gaps no influence of the opposite edge is expected.

In contrast, the variation of the corner angles showed a reasonable influence on the corner artifacts in the simulations. Also this can be understood intuitively, as the distance between two points that have the same distance from the corner origin will be bigger for bigger corner angles. Therefore, also the interference of the diffraction pattern will be reduced. Figure 5 shows images of corner angles of 90° C and 135° C, simulated with LGO optics at an exposure gap of 30 µm. For the 90° C angle amplitude, frequency and number of visible undulations is higher than for the 135° C angle.

As third geometrical parameter the use and size of a fillet, i.e. a rounding of the inner corner, was determined. Fillets were simulated for curvature radii ranging from 2.5 µm up to 33 µm. However, the maximum reasonable curvature radius depends on the length ℓ of the artifact area and on the angle of the corner. The fillet distance s should not exceed the length ℓ of the artifact area thus restricting the curvature radii of the fillets to 20 µm and smaller. Figure 7 shows a comparison between simulations performed for a corner without fillet and with a fillet of 5 µm curvature radius. The diffraction artifact is considerably reduced, most prominently visible for the 90° C corner, where the corrugation visible at the structure without corner rounding is completely removed The experimental results shown in the optical microscopy image clearly support the results from the simulation. The length of the abrasion area ℓ at the resist surface was almost reduced to half the value without fillet.

EXPOSURE OPTICS

Even more then fillets, the choice of the exposure optics had a significant influence on the exposure result. Both, experimental data as well as simulation results proved, that by using HR optics the presence of corrugations can be drastically suppressed for all corner shapes, at all observed exposure gaps. In the optical

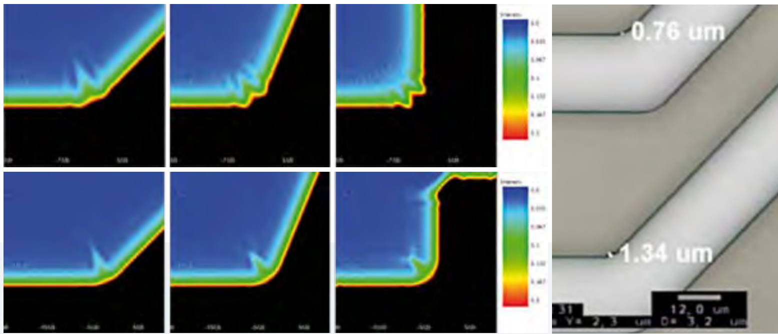

Figure 7. Comparison between the simulation results of a sharp corner (fillet radius 0, top row) and a corner smoothed with a filled of radius 5 µm (bottom row). This simulation was performed for LGO optics in 30 µm exposure gap. The optical microscopy image shows the results of consequential experiments with a mask having rounded corners (top conductor path) and sharp corners (bottom conductor path).

microscopy, which is depicted in Figure 8, distinct resist abrasion can be observed at the inner corner of the conductor paths created by LGO optics exposure (Figure 8 left). In this case the resist abrasion is strong enough to reach down to the bottom of the resist wall, changing the actual shape of the conductor path at the corner even at the wafer surface. Additionally, it is easily recognizable from the image that the artifact

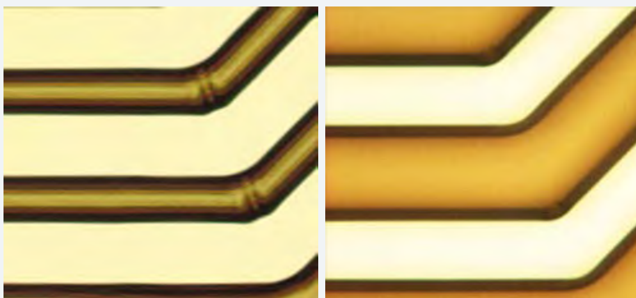

Figure 8. Optical microscopy images of corners in the conductor paths. The image on the left depicts the situation after exposure with LGO optics, the picture on the right after exposure with HR optics. The artifacts in the corner are significantly reduced.

continues towards the resist surface, interfering with the designed structure throughout the complete resist thickness. In contrast to that, in the image of the conductor path, created with HR optics exposure, no resist abrasion is detectable at the wafer surface. Even on the top side of the resist hardly any proximity artifact can be distinguished. The results of simulation calculations affirm the experimental results.

Figure 9 represents the results of simulations done for LGO optics (left hand image) and HR optics (right hand image). While in the LGO result a strong corrugation of the edge is visible, the HR results show hardly any corrugation. These results identified the optics of one of the main parameters to reduce the proximity induced corner artifacts.

CONCLUSIONS

From the results of the presented study three main claims can be made. First, the study proved the capability of the simulation software to support the process development by reducing the amount of experimental time and cost. By assessing the effect of corner fillets and the influence of the curvature radius the mask design could be optimized without the need to do several design iterations.

Second, the effect of fillets on the reduction of proximity induced corner artifacts could be proved and a quantitative support for the mask design could be derived. Third, the significant influence of the optics, selection on the reduction of diffraction phenomena could be visualized. The results emphasize the high importance for selecting the right optics configuration in order to keep unwanted proximity artifacts at the smallest possible level. In combination with the use of fillets the formation of proximity artifacts can be minimized.

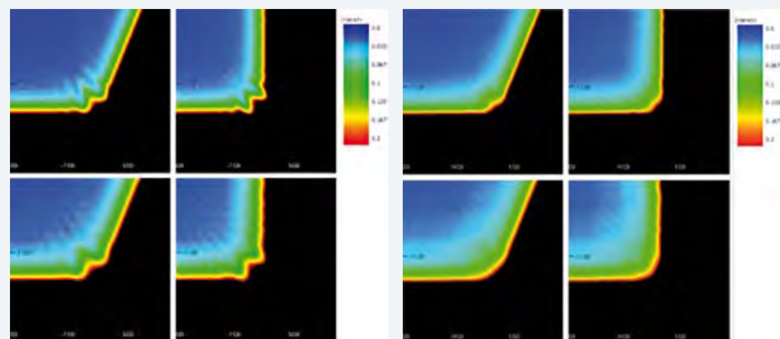

Figure 9. Images of simulation results calculated with LGO (left) and HR optics (right), at 30 µm (top) and 50 µm (bottom) gap, respectively. In the images calculated with LGO optics distinct corrugations can be seen for both gaps. The results obtained with HR optics show drastically reduced corrugations, with having slightly better results when exposing at 50 µm gap, where no corrugation but only a corner rounding can be observed.

Dr. Marc Hennemeyer is Application Scientist at SUSS MicroTec Lithography. He works on coaters and mask aligners and was responsible from SUSS MicroTec side for the evaluation of the LabView simulation software. Marc graduated in Physics at University of Munich where he also received his PhD working on micro fluidic systems for biological applications. He authored and co-authored several papers on various topics, including micro imprinting and lithography and lithography simulation.

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SUSS MICROTEC AND GENISYS ANNOUNCE COOPERATION ON MASK ALIGNER LITHOGRAPHY SIMULATION SOFTWARE

February 21, 2012

SUSS MicroTec and GenISys GmbH, provider of high-performance software solutions for nano scale fabrication, today announced a cooperation agreement to combine the SUSS MicroTec mask aligner tools with the GenISys simulation software Layout LAB.

SUSS MICROTEC LAUNCHES RCD8: THE NEW RESIST COAT AND DEVELOP PLATFORM

March 19, 2012

launched the RCD8, a new manual Resist Coat and Develop Platform for substrates. The new platform offers a high application variety coupled with low investment costs as well as an easy transfer of processes from the RCD8 manual platform to a SUSS MicroTec production tool.

ACQUISITION OF TAMARACK SCIENTIFIC CO., INC. – EXPANSION OF TECHNOLOGY COMPETENCE IN PHOTOLITHOGRAPHY

March 29, 2012

SUSS MicroTec announces the acquisition of Tamarack Scientific Co. Inc. (Tamarack), Corona, California, USA. Both parties signed a corresponding purchase agreement. The agreement stipulates the purchase of 100% of Tamarack's shares for a total price of $ 9.34 million plus an additional variable earn-out component which depends on the development of revenues for the upcoming three financial years.

The requirement for more functionality and higher performance of electronic devices drives the increasing performance needs for semiconductor components and higher complexity at the same time.

"With this acquisition, we enlarge our company's lithography segment by adding a new product line and core technology, both of which are highly complementary to our existing exposure capability."

Frank P. Averdung,
President and CEO, SUSS MicroTec

SUSS MICROTEC LAUNCHES ACS200 GEN3: THE NEW GENERATION 200 MM AUTOMATED COATER / DEVELOPER PLATFORM

July 9, 2012

SUSS MicroTec launches the third generation of the ACS200 Coating and Developing Platform. This newly developed tool offers an excellent mix of innovation and production proven technology components of the well-established ACS200Plus and Gamma platforms.

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	MNE	Toulouse, France	Sep 16 - 20
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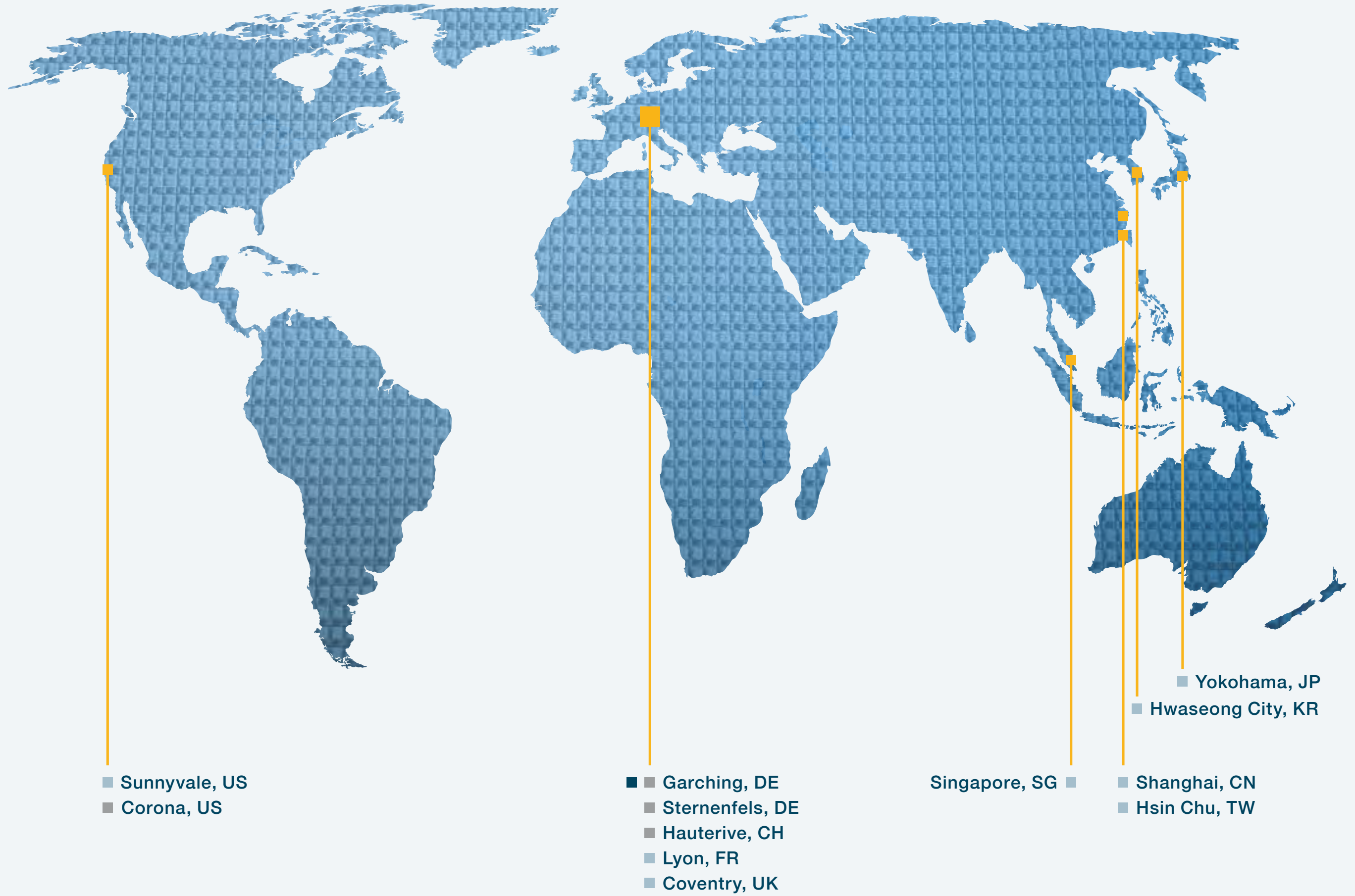

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Imprint

Publisher:
SÜSS MicroTec AG
Schleissheimer Str. 90
85748 Garching
Germany
info@suss.com

Chairman:
Dr. Stefan Reineck

Executive Board:
Frank Averdung (CEO)
Michael Knopp (CFO)

Register Court Munich
HRB Nr. 121347

Value added tax identification number:
DE192123619

Editorial:
Hosgör Sarioglu, Corporate Marketing Manager

Print: BlueMedia GmbH, Munich

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