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STRONG PARTNERS FOR TECHNOLOGY LEADERSHIP

Low-Temperature Wafer Bonding Using Sub-micron Au Particles

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+ FULL VIEW

Frank Averdung
President & CEO
SÜSS MicroTec AG

Over the last months the global macroeconomic environment was affected by the uncertainty about currencies and country debt levels.
Politics could do little to mitigate the concerns of consumers, customers and suppliers that the financial constraints of certain countries might have an impact on the „real economy".
But regardless of these uncertainties, SUSS MicroTec with its strong market position has laid the foundation for long term profitable growth. We achieved market leader status in three out of our four product areas as a result of continuous innovation and a product portfolio perfectly matching the requirements of our global customer base. Key is the close interaction with the users of our equipment.

Tradeshows and exhibitions are an excellent opportunity to stay in touch with market trends and customers.
At this year's Semicon West SUSS MicroTec focused on the defining theme of the industry „Shrink. Stack. Integrate." presenting solutions for the 2D and 3D roadmap.Parallel to Semicon West we held a well attended 3D-Integration Technology Workshop. Industry experts in materials, equipment and processing joined SUSS MicroTec's workshop addressing the status of the 3D TSV infrastructure and recent advances in 3D processing technologies. The speakers included customers as well as representatives from our research partners, such as IMEC and Brewer Science®. SUSS MicroTec presented equipment and process solutions for Temporary Bonding.

In July we hosted the industrial seminar "Mask Integrity Challenges – Where Lithography Begins" at the Tokyo International Forum. The forum featured a day of technical presentations from customers and technology partners about significant challenges facing the next generation lithography reticles. Additionally new cleaning solutions guaranteeing the highest level of mask integrity were discussed during the seminar.

In September we conducted our first international suppliers' day in Sternenfels dedicated to increase the efficiency of our supply chain. In the light of the recent relocation of the wafer bonder division to Germany this meeting allowed the decision makers of all parties as well as engineers and constructors to get to know each other and cooperate efficiently.
As a leading equipment provider we permanently strengthen our product portfolio by innovations and technological improvements.
A recent example is the newly introduced MaskTrack Pro InSync. With this equipment we were able to introduce the first holistic in-fab EUVL mask management offering in the market. MTP InSync is a stand-alone or clustered handling system which seamlessly synchronizes mask cleaning, handling, inspection and storage in a single controlled environment. It is a critical element within the EUVL production infrastructure.

More projects are highlighted in this issue.

LOW-TEMPERATURE WAFER BONDING USING SUB-MICRON AU PARTICLES

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INTRODUCTION

Metal-to-metal wafer bonding has recently been increasingly studied in the field of MEMS packaging since the technique could decrease the sealing line area, which would result in the chip size reduction, realize hermetic sealing and also enable electrical interconnections between the two bonded wafers[1], [2]. Low-temperature wafer bonding has also become important for various purposes such as reducing the post-bond residual stress at mechanical structures in MEMS devices and preventing bowing or cracks when bonding two materials with dissimilar coefficients of thermal expansion (CTE).

In order to lower the bonding temperature, sub-micron or nano-scale metal particles, such as gold, silver, and copper, have been tested since they are reactive at low temperatures due to their very active surfaces[3–6]. Wafer bonding with these metal particles has another advantage of being able to adapt to a certain level of surface roughness and/or topography at the bonding surfaces in contrast to bonding with thin metal films, which requires nanometer-order surface smoothness. It was observed in a previous study[3] conducted by Tanaka Kikinzoku Kogyo K.K. that micro-bumps formed of sintered sub-micron Au particles could be bonded at 230°C with a thermocompression method and exhibited a good bonding strength.

In this paper, a wafer-level patterning and low-temperature wafer bonding with sub-micron Au particles were studied and the feasibility of hermetic sealing was investigated. In addition, a wafer-level pattern transfer will also be briefly introduced.

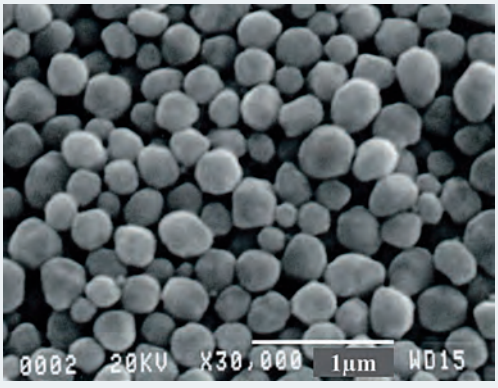


Figure 1: FE-SEM image of the sub-micron Au particles

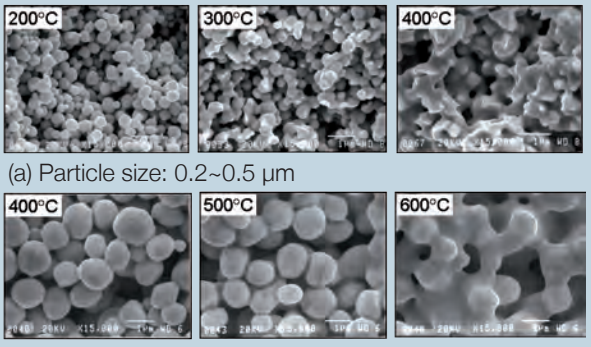


Figure 2: Temperature dependence of reaction behavior of sub-micron Au particles with different particle size; (a) 0.2 – 0.5 µm and (b) 1.0 – 2.5 µm.

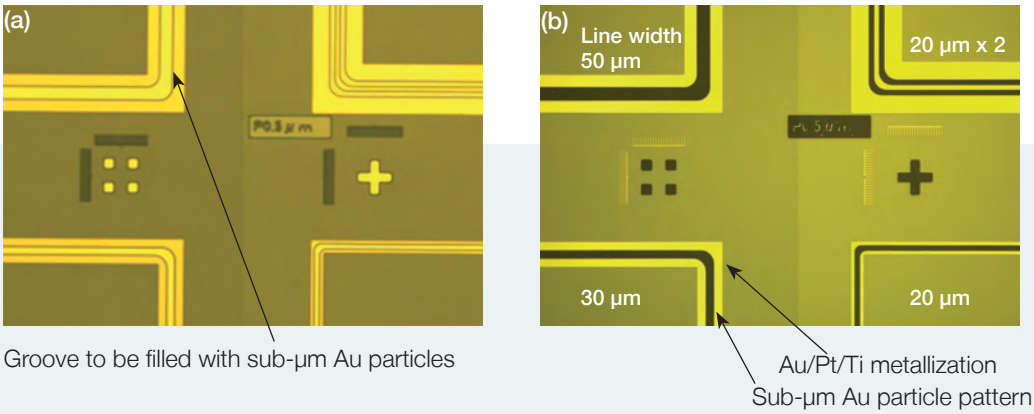


Figure 5: Microscope photos of (a) patterned photoresist mold layer and (b) sub-micron Au patterns after photoresist removal

EXPERIMENTAL

MATERIALS AND SAMPLES

The 99.95wt% purity, spherical sub-micron Au particles were obtained through a wet chemical processing method by mixing chloroauric acid solution with a reducing agent. The obtained particles shown in Figure 1 consisted of individual gold particles and their diameters were in the range of 0.1 µm – 0.5 µm[3]. Reactivity of the Au particles, or possible bonding temperature in actual processes, is significantly influenced by their size. As you can see in Figure 2, sub-micron-sized particles can be connected even at a temperature lower than 200ºC, but in contrast, those of a few microns diameter do not react very much up to 400ºC. Figure 3 shows the gold slurry used for actual patterning process, which was prepared by mixing the sub-micron Au particles with an organic solvent and surface active agents.

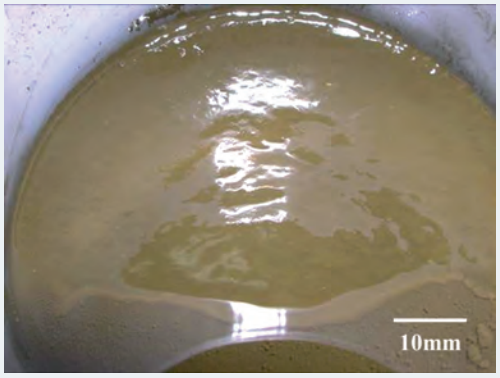


Figure 3: Photo of the Au slurry, the mixture of sub-micron Au particles and an organic solvent with addition of surface active agents

For the wafer bonding experiment, 100mm-diameter double-side-polished glass wafers (TEMPAX Float®, Schott AG, 500µm thick) were used to prepare two kinds of test wafers; one having only a patterned metallization layer and the other with the sealing-line patterns of sub-micron Au particles on the metallization layer. As the metallization layer, a 50nm-thick Ti, a 50nm-thick Pt and a 200nm-thick Au layer were sequentially deposited by sputtering. The sealing lines of sub-micron Au particles were formed by filling the Au slurry into the thick photoresist layer according to the process flow shown in Figure 4. The widths of the sealing lines for the bonding tests were set at 10 µm, 20 µm, 50 µm and 100 µm.

PATTERNING OF SUB-MICRON AU PARTICLES

Figure 5 shows the result of the patterning of sub-micron Au particles using a photoresist mold layer. Photo (a) shows the photoresist patterns after the process step 1 described in the process flow and (b) exhibits the sub-micron Au sealing line patterns formed on the metallization layer after the process step 6. It can be seen in photo (b) that the shape of the sub-micron Au particle sealing lines was well defined by the photoresist mold layer with no critical defects like an open path which directly causes a leakage.

The thickness and surface roughness (average roughness, Ra) of the sealing lines before bonding were measured with a laser microscope at 28 points across the 100mm-diameter wafers. The average height of the sealing line was calculated to be 18.0 µm with maximum and minimum heights of 19.1 µm and 17.3 µm, respectively, and a uniformity of 4.9%. The height uniformity of the sealing lines is similar to that of the

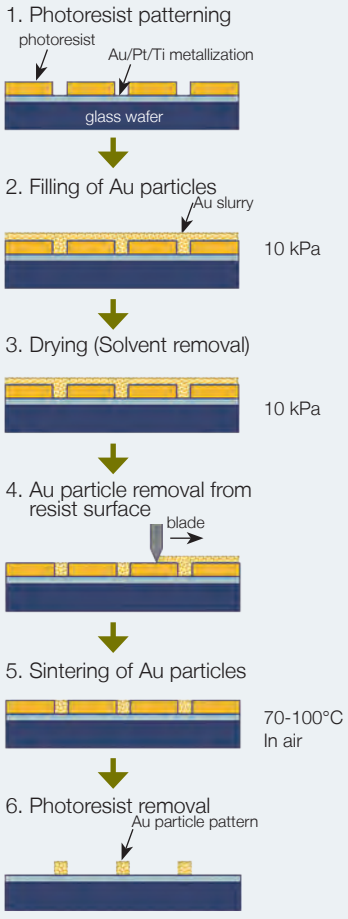


Figure 4: Process flow to form sub-micron Au particle sealing line patterns

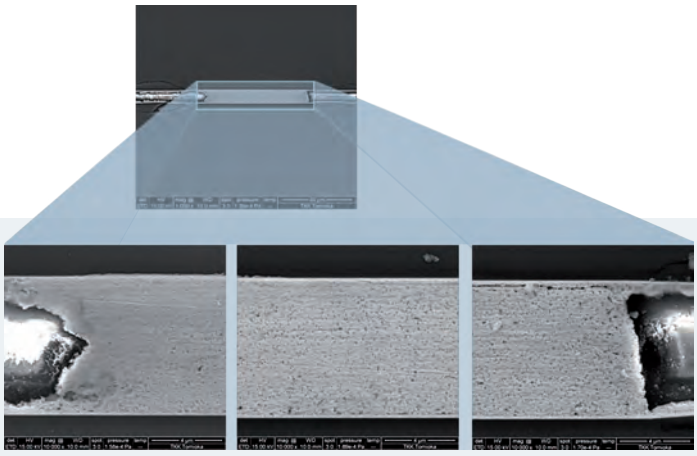


Figure 7: Cross-section SEM image of a sub-micron Au pattern after bonding at 200°C, 100 MPa for 10 min. The black areas correspond to the top and the bottom wafers and the bright part shows a densified Au particle sealing line. Au/Pt/Ti metallization layer was deposited on each glass wafer.

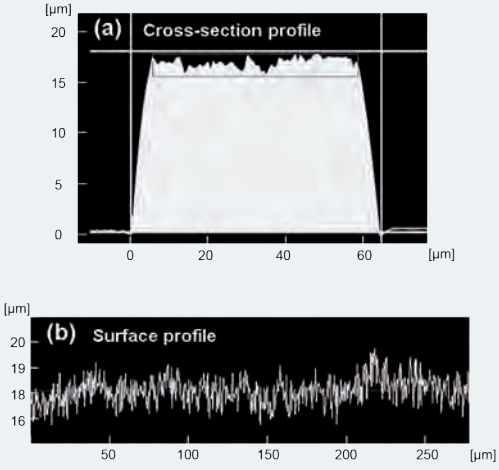


Figure 6: Measurement of the topography of sub-micron Au sealing lines. (a) cross-section view and (b) surface roughness in longitudinal direction of a 50 µm-wide line.

photoresist mold layer and this means that the shape of the sub-micron Au particle patterns can be properly controlled by the preceding lithography process of the photoresist mold layer. The cross-section view and the surface topography of a 50µm-wide sealing line are shown in Figures 6 (a) and (b), respectively. The measurement results indicate that the sealing lines have a surface topography with peak-to-valley distance of about 2 µm and an average roughness, Ra, of 0.56µm.

WAFER BONDING

Prior to wafer bonding, precise optical alignment was conducted on the SUSS BA8 bond aligner to align the sub-micron Au particle sealing lines on one wafer to the corresponding metallization patterns on the other wafer. The wafer bonding was performed in vacuum on the SUSS SB8e wafer bonder at bond temperatures of 150°C or 200°C and applied pressures of 50 MPa or 100 MPa, with 10 minutes duration at each defined condition. Figure 7 shows a cross-section SEM image of a sealing line bonded at 200°C and 100MPa. The photo demonstrates that the sub-micron Au particles were densified into a bulk solid after bonding process. It has been observed in a previous work[3] that sub-micron Au particles start to connect at their surfaces at temperatures as low as 70°C and grow to larger grains with increasing temperatures, and that they could be compressed into bulk Au with eliminating voids by applying pressure.

BONDING STRENGTH

The bonding strength was evaluated using 5mm x 5mm chips that were diced from the bonded wafers. Tensile strength was measured using the stud-pull method on a universal mechanical-strength tester and the average values were calculated using three chips for each bonding condition by dividing the tensile force by the sealing line area. Table 1 summarizes the result for three different bonding conditions for the samples with 50 µm-wide sealing lines. It was demonstrated that sample #1, bonded at 200°C and 100MPa, showed the maximum average strength of 45.8MPa and that all samples exhibited the bonding strength greater than 20MPa, even at a temperature as low as 150°C. These values are comparable to those of other hermetic bonding methods such as 18MPa for Au-Si eutectic bonding[7] and 10.1–10.7MPa for Au-Au diffusion bonding[8].

SAMPLE NO.	BONDING CONDITION		TENSILE STRENGTH [MPa]		
	TEMPERATURE [°C]	PRESSURE [MPa]	AVERAGE	MAX.	MIN.
# 1	200	100	45.8	57.4	38.1
# 2	150	100	33.9	40.9	25.3
# 3	200	50	22.0	29.9	15.3

Table 1: Result of tensile strength measurement of 5mm x 5mm chips with various bonding conditions

It can be seen from Table 1 that

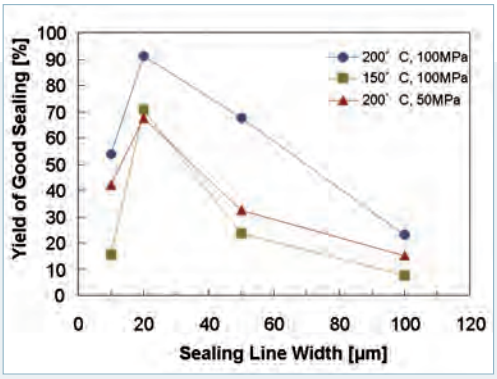


Figure 8: Dependence of the yield of good sealing on sealing line width for various bonding conditions. (●) shows the yield for bonding condition of 200°C, 100 MPa, (■) for 150°C, 100 MPa, and (▲) for 200°C, 50 MPa.

bonding strength improves with increasing bonding temperature or bonding pressure. Since sub-micron Au particles were well-densified, becoming bulk solid, bonding strength is considered to be determined by the bonding area where the Au particles are actually in contact with the Au metallization. The bonding area can be increased either by elevating the bond temperature, which promotes surface diffusion to bond the Au particles with the Au metallization, or by increasing the bonding pressure, which can flatten the pattern surface to enable tighter contact. It appears that the latter effect contributed more in the bonding temperature region as low as 150°C – 200°C.

HERMETIC PROPERTY

In order to check the sealing performance of the sub-micron Au particle bonding, the bonded wafer pairs were immersed into a low-viscosity hydrofluoroether liquid, Novec® (Sumitomo 3M Ltd.), in a vacuum container evacuated down to 10kPa. Gross leak can be easily checked by seeing whether the liquid flows into sealed areas or not.

The yield of good sealing was calculated for each sealing line width by dividing the number of "Good" chips by the total number of chips. The result was plotted in the Figure 8 as a function of sealing line width. The figure indicates that the yield reached a maximum value of 91.2% with a line width of 20μm. It should be mentioned that a yield of > 50% was obtained for a sealing line width of as narrow as 10μm. It is considered that the yield was strongly influenced by the quality of the sealing line patterns. For thinner lines, leak paths (or open voids) might be generated more easily due to insufficient filling of Au particles into the resist mold. On the other hand, for wider lines, it was confirmed that a few amount of Au particles were accidentally removed from some pattern surfaces during the patterning step 4 in Figure 4, which created relatively large recesses on the pattern surfaces. This topography could degrade the sealing yield. In order to improve the yield of good sealing and also bonding strength, it is important to improve the quality of the sealing line patterns; in other words, to realize well-filled and smoother surface Au particle patterns.

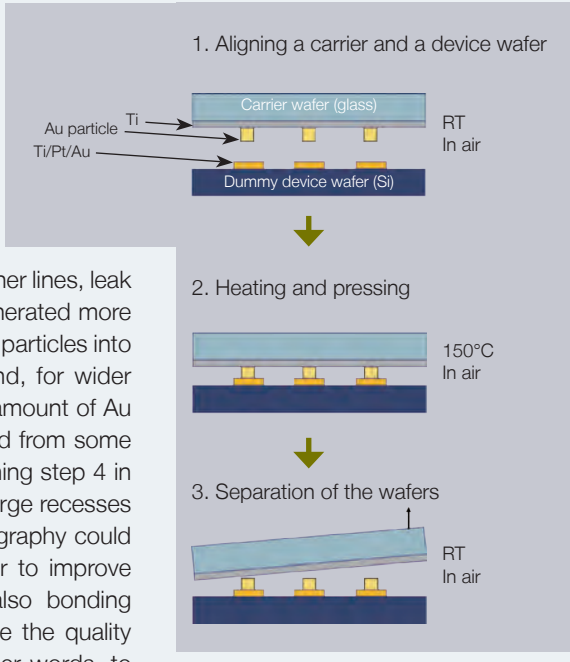
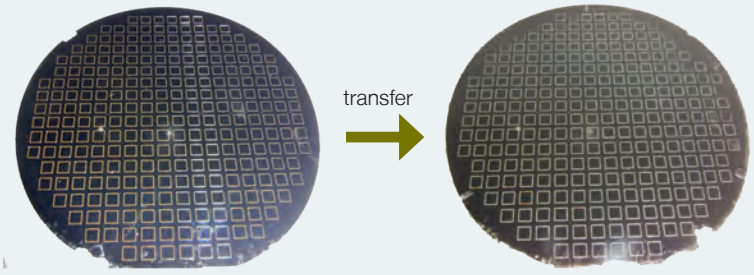


Figure 9: Process flow of a wafer-level pattern transfer of sub-micron Au particles.

WAFER-LEVEL PATTERN TRANSFER

Considering practical applications of this bonding technique, a wafer-level pattern-transfer method was developed so that sub-micron Au particle patterns can be formed even on wafers with



(a) Initial patterns (on carrier wafer)

(b) Transferred patterns (on dummy device wafer)

Figure 10: Photos of Sub-micron Au particle patterns; (a) on a carrier wafer (before transfer) and (b) on a dummy device wafer (after transter).

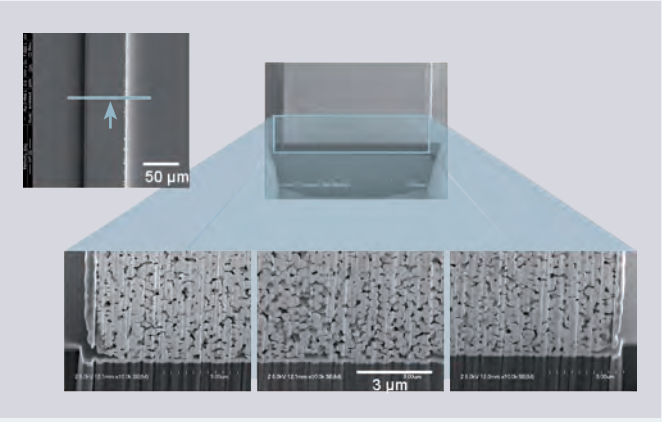


Figure 11: Cross-section SEM image of a sub-micron Au particle pattern after pattern transfer at 150°C, 20 MPa

fragile structures such as MEMS devices. Sub-micron Au particle patterns were formed on a 100mm-diameter glass "carrier" wafer with 50nm thick Ti metallization and the patterns were transferred to a silicon "dummy" device wafer with Au/Pt/Ti metallization layer. Figure 9 describes the process flow of a wafer-level pattern-transfer. First, precise optical alignment of a carrier wafer and a dummy device wafer was performed on the SUSS BA8 Bond Aligner to align the sub-micron Au particle seal lines to the corresponding metallization patterns.

Then, the aligned wafer pair was properly pressed on the SUSS SB8e wafer bonder in ambient atmosphere at a temperature of 150°C and applied pressure ranging from 5MPa to 30MPa with keeping for 10 minutes. Finally, the wafer pair was slowly separated outside the bond chamber and sub-micron Au particle patterns were transferred to a device wafer.

Figure 10 shows photos of sub-micron Au particle patterns (a) on a carrier wafer and (b) transferred onto a 100mm-diameter Si wafer at an applied pressure of 20MPa.

As you can see from the photo, Au particle patterns were successfully transferred across the wafer. As shown in Figure 11, transferred patterns maintain sintered particle structures and therefore can still exhibit its unique characteristics.

In order to evaluate the pattern-transfer performance, "transfer yield" was calculated by dividing the number of good patterns by the total number. Dependence of transfer yield on applied pressure is shown in Figure 12. The result indicates that the yield firstly improved with increasing applied pressure and then stabilized to be 70% ~ 80% at pressure above 20MPa. It is estimated that a reason for relatively

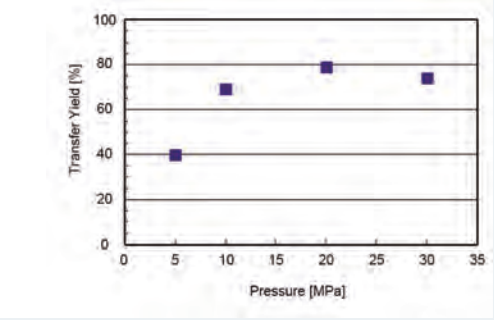


Figure 12: Dependence of pattern-transfer yield on applied pressure

REFERENCES

[1] N. Belov, T-K. Chou, J. Heck, K. Kornelsen, D. Spicer, S. Akhlaghi, M. Wang, T. Zhu, "Thin-Layer Au-Sn Solder Bonding Process for Wafer-Level Packaging, Electrical Interconnections and MEMS Applications", Proceedings of The 2009 IEEE International Interconnect Technology Conference (IITC), pp.128–130, 2009.

[2] Jay Mitchell, G.R. Lahigi, Khalil Najafi, "Long-Term Reliability, Burn-In and Analysis of Outgassing in Au-Si Eutectic Wafer-Level Vacuum Packages", Proceedings of Solid-State Sensors, Actuators, and Microsystems Workshop, pp.376–379, 2006.

[3] Toshinori Ogashiwa, Tadahiro Shibutani, Masayuki Miyairi, Yoshitomo Fujisawa, Kazunori Tsurumi, Qiang Yu, "Low-Temperature Bonding Technique Using Sub-Micron Au Particles", Journal of Japan Institute of Electronics Packaging, Vol. 10, No. 7, pp.560–566, 2007, (In Japanese).

[4] E. Ide, S. Angata, A. Hirose, K. F. Kobayashi, "Metal-metal bonding process using Ag metallo-organic nanoparticles", Acta Materialia, Vol. 53, pp.2385–2393, 2005.

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low transfer yield at lower applied pressures is poor surface flatness of initial Au particle patterns that may not sufficiently be pressed to be flattened and therefore may result in a less attached area for pattern transfer.

CONCLUSION

Wafer-level patterning of sub-micron Au particles was carried out employing a photo-resist mold layer and gold slurry filling. Sealing line patterns with widths of 10µm – 100µm and a pre-bonding height around 20µm were formed with a height uniformity of 4.9% across the 100mm-diameter wafer. The surface roughness of the sealing lines was measured as the average roughness, Ra, of 0.56µm.

Low-temperature wafer bonding using sub micron Au particles was performed at temperatures as low as 150°C. Tensile strength measurements using 5mm x 5mm chips revealed that the average bond strength of the samples bonded at 200°C and 100 MPa was 45.8MPa.

The feasibility of hermeticity by wafer bonding using sub-micron Au particles was demonstrated by confirming no leakage of a low-viscosity liquid through the sealing lines. The yield of good sealing showed a maximum value of 91.2% with the sealing line width of 20µm.

In order to improve the bonding quality, or bonding strength and sealing yield, it is important to realize well-filled and smoother surface Au particle patterns.

For practical applications of this bonding technique, a wafer-level pattern transfer method was developed.

[5] Toshiaki Morita, Yusuke Yasuda, Eiichi Ide, Akio Hirose, "Bonding Technique Using Micro-Scaled Silver-Oxide Particles", Journal of Japan Institute of Electronics Packaging, Vol. 12, No. 2, pp. 110–113, 2009, (In Japanese).

[6] T. Nagaoka, Y. Morisada, M. Fukusumi, Y. Kashiwagi, M. Yamamoto, M. Nakamoto, "Low Temperature Bonding Process Using Cu Nanoparticles", Pre-Prints of the National Meeting of JWS, No. 82, pp.138–139, 2008, (In Japanese).

[7] R. F. Wolffenbuttel, K. D. Wise, "Low-temperature silicon wafer-to-wafer bonding using gold at eutectic temperature", Sensors and Actuators A, Vol. 43, pp.223-229, 1994.

[8] M. M. V. Taklo, P. Storås, K. Schjølberg-Henriksen, H. K. Hasting, H. Jakobsen, "Strong, high-yield and low-temperature thermocompression silicon wafer-level bonding with gold", J. Micromech. Microeng., Vol. 14, pp.884-890, 2004.

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His recent experience includes process development of various kinds of wafer bonding such as polymer bonding and metal diffusion bonding.
He received his B.E. and M.E. in Electronic Engineering from Tohoku University.

Toshinori Ogashiwa received B.E. and M.E. degrees from Mining College of Akita University in 1982 and 1984, respectivery, and Dr.E. degree from Tohoku University in 1994.
He has joined Tanaka Kikinzoku Kogyo since 1984, and is a project leader of the Technical Division.
His research interests include low-temperature bonding technology for electronic devices.

FORMATION OF PRECISE 2D AU PARTICLE ARRAYS VIA DEWETTING ON PRE-PATTERNED SUBSTRATES

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An increasing amount of scientific attention is being paid to the ordered arrangement of metallic nanoparticles, due to their wide range of potential applications in plasmonics[1,2], magnetic memories[3], DNA detection[4], and catalysis for nanowire and nanofiber growth[5,6]. A simple method to fabricate the nanoparticle arrays is dewetting of thin films on the pre-patterned substrates. Dewetting of metal films on a substrate is induced by thermal annealing and driven by the reduction of the surface energy of the thin film and of the interface energy between the film and substrate.

Normally, the dewetting of metal films on the flat substrate leads to the broad distribution of particle size and spacing, as shown in Figure 1. Both, mean particle size and the width of particle size distribution increase with increasing film thickness.

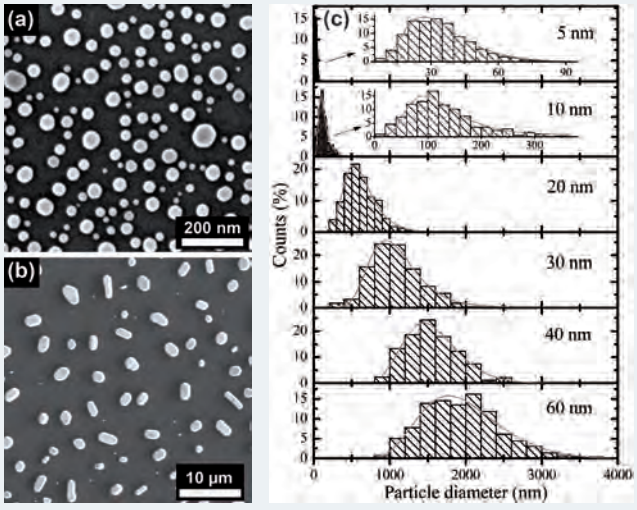

Figure 1:
SEM images of induced particles on the flat SiO2/Si substrate after the dewetting for the 5nm (a) and 60nm (b) thick Au films. (c) Derived histograms of particle size distributions produced by the dewetting of the 5nm, 10nm, 20nm, 30nm, 40nm, and 60nm thick Au films on the flat SiO2/Si substrates. Inset plots in (c) are magnified histograms for better visibility. The fitting curves (fitted with log-normal function) are superimposed in histograms.

However, the morphology of the substrate can influence the mechanisms of dewetting and the ordered nanoparticle arrays can be produced by the dewetting of thin metal films on the pre-patterned substrates[7,8]. Two types of pre-patterned substrates were fabricated using substrate conformal imprint lithography (SCIL)[9] and reactive ion etching (RIE): One with a square array of pyramidal pits (substrate type A), shown in Figure 2a and another with an array of circular holes with square symmetry (substrate type B), shown in Figure 2b. The pits in substrate A have a spatial period of 513 nm and a depth of 150 nm. The holes in the substrate B have the same spatial period of 513 nm, a diameter of about 490 nm and a depth of 120 nm.

20 nm and 40 nm thick Au films were deposited on the pre-patterned substrates and then

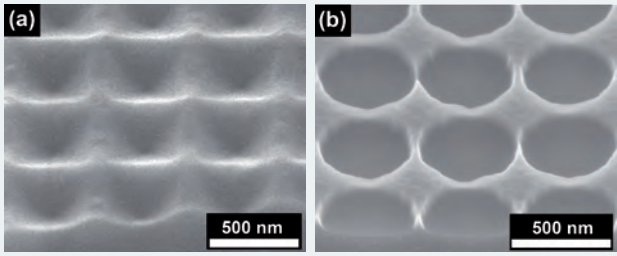

Figure 2: SEM images at 45° tilt of (a) square arrays of pyramidal pits (substrate A) and (b) array of circular holes with square symmetry (substrate B)

annealed in N_2 at 900 °C for 15 min in order to induce the dewetting. Figure 3 shows the SEM images of the 20nm thick as-deposited Au films and the dewetted particles. All particles are located in pits and in every pit there is only one particle. Thus a precise periodic array of particles evolved as seen in Figure 3b. Dewetting of solid films is driven by reducing the surface energy (capillarity driven dewetting mechanism) and results in formation of particles via surface diffusion. Surface curvatures of periodic substrate structures are associated with the chemical potential, introducing an additional driving force for diffusion from the position with positive local curvature (peaks or ridges) to the position with negative local curvature (valleys) and an additional barrier for diffusion at the position with positive local

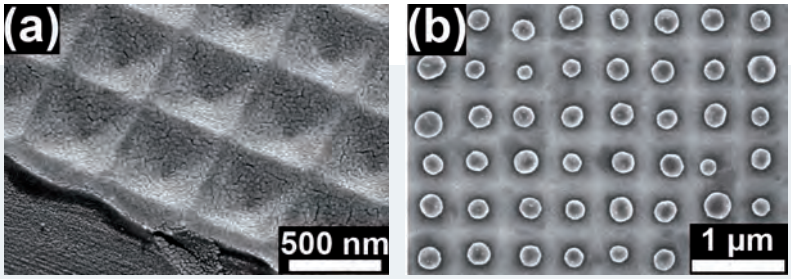

Figure 3: SEM images: (a) the as-deposited 20nm thick Au film, and (b) the dewetted Au particle array on the substrate A (pyramidal pits)

curvature (peaks or ridges)[7,8]. So with the additional diffusion driving force, the ordered particle array is formed on the pre-patterned substrate A.

The influence of the substrate B (circular holes) on dewetting is somewhat different[8]. Figure 4 shows the SEM images of the 40 nm thick as-deposited Au film and the dewetted particle array on the substrate B. There is only one formed particle in every hole and one on every mesa (Figure 4b). The particles in holes are clearly larger than particles on mesas. The interior sidewalls of holes of the substrate B are perpendicular to substrate horizon and normally, the subsequence is the evolution of film discontinuity at the perpendicular interior sidewalls by film deposition (Figure 4a). The film discontinuity is substrate-exposing, separates the film and limits the diffusion pathway within the individual regions (holes and mesas). The Au would retract from the discontinuity regions and one particle is formed in every individual region after annealing, so that the precise particle arrays are evolved (Figure 4b).

The substrate conformal imprint lithography (SCIL) technique enables the production of large areas (6 inch area) of pre-patterned substrates with high uniformity and the corresponding fabrication of large areas of precise 2D particle arrays. The remarkable optical and plasmonic properties of noble metallic particles indicate the potential applicability of this method in fabricating large area of particle arrays for plasmonic devices or in improving the efficiency of photovoltaic devices and light-emitting diodes (LED) by modification of surface optical properties.

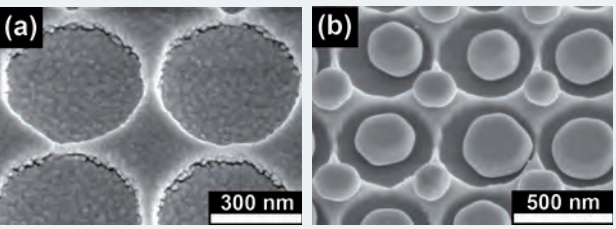

Figure 4: SEM images at 30° tilt: (a) the as-deposited 40 nm thick Au film, and (b) the dewetted Au particle array on the substrate B (circular holes)

Dr. Dong Wang studied chemical engineering at Wuhan University of Technology in China and received his B.Sc. in 2000, and studied materials science further at RWTH Aachen in Germany and received his M.Sc in 2004. Then, he conducted his doctoral research at research Center Karlsruhe. After receiving his Ph.D. in 2007, he moved to Hannover to pursue a post-doc at Hannover University. In 2010, he accepted a staff scientist position at Ilmenau University of Technology (TU Ilmenau). His research interest lies at nanostructured materials.

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References

[1] Maier, S. A.; Brongersma, M. L.; Kik, P. K.; Meltzer, S.; Requicha, A. A. G.; Koel, B. E.; Atwater, H. A. Adv. Mater. 2003, 15, 562.

[2] Fan, J. A.; Wu, C. H.; Bao, K.; Bao, J. M.; Bardhan, R.; Halas, N. J.; Manoharan, V. N.; Nordlander, P.; Shvets, G.; Capasso, F. Science 2010, 328, 1135.

[3] Cheng, J. Y.; Ross, C. A.; Chan, V. Z. H.; Thomas, E. L.; Lammertink, R. G. H.; Vancso, G. J. Adv. Mater. 2001, 13, 1174.

[4] Fritzsche, W.; Taton, T. A. Nanotechnology 2003, 14, R63.

[5] Kodambaka, S.; Tersoff, J.; Reuter, M. C.; Ross, F. M. Science 2007, 316, 729.

[6] Guan, Y. F.; Pearce, R. C.; Melechko, A. V.; Hensley, D. K.; Simpson, M. L.; Rack, P. D. Nanotechnology 2008, 19, 235604.

[7] Giermann, A. L.; Thompson, C. V. Appl. Phys. Lett. 2005, 86, 121903.

[8] Wang, D.; Ji, R.; Schaaf, P. Beilstein J. Nanotechnol. 2011, 2, 318–326.

[9] Ji, R.; Hornung, M.; Verschuuren, M. A.; van de Laar, R.; van Eekelen, J.; Plachetka, U.; Moeller, M.; Moormann, C. Microelectron. Eng. 2010, 87, 963.

POINT-OF-USE WET CHEMICAL SURFACE TREATMENT FOR COPPER BASED WAFER BONDING

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INTRODUCTION

With increasing interconnect densities and rising cost of IC manufacturing in leading edge technology nodes, 3D integration is proving to be the next key building block in the development of future microelectronic devices. Low temperature Cu-Cu, Cu/hybrid and Cu-Sn wafer bonding in addition to emerging TSV technologies are critical to making 3D successful for mainstream microelectronics manufacturing. Many 3D integration schemes are based around copper because this material is used extensively in FEOL, has a well-developed CMP history and high yield through-silicon-vias that have already been proven. But Cu surface suffers from spontaneous and non self-limiting oxidation of its surface. The oxides that form on the Cu surface inhibit rapid diffusion and reduce final conductivity at the metal interface. Cu-Cu bonding processes require the need for contamination free and smooth surfaces, which becomes increasingly important if lower temperature processes (<300°C) are desired[1].

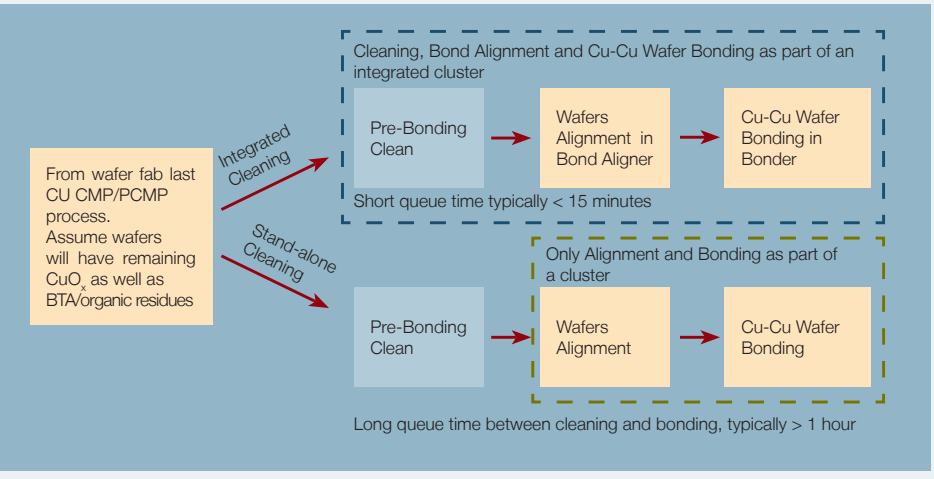


Figure 1: Two approaches to Point of Use Cu cleaning, either as part of an integrated cluster (very short queue time) or as a stand-alone pre-bond cleaning module followed by the bond cluster (relatively long queue time)

COPPER SURFACE CLEANING

Three key requirements for a clean copper surface include (a) excellent surface roughness, (b) complete removal of undesirable copper oxide layers and (c) complete removal of organic contaminants and Cu inhibitors from previous CMP steps. Additionally, it may be advantageous to protect the copper surface with a thin copper oxidation barrier (COB) that can be easily applied and easily removed prior to bonding. This would protect the clean, more reactive Cu surface and prevent further environmental contamination from attaching to the Cu surface, especially in processes where there may be an extended queue time between cleaning and bonding. Close-coupled copper cleaning immediately prior to the bonding step offers an excellent approach for providing process reproducibility while achieving increased electrical yields.

Integration Approach:

The most effective approach for Cu cleaning would be to implement a clean immediately prior to the actual Cu-Cu wafer bonding step. Leading edge wafer bonding tools require clustered modules which include a pre-bonding clean station. Close-coupling the clean with the bonding step through this clustered arrangement allows for better control of the copper surface prior to bonding, as well as a very short queue time, less than 15 minutes in most cases. However, not all bonding equipment will have integrated cleaning modules and it is important to ensure that the cleaning chemistries and process will also be effective in stand-alone cleaning tools as well. The process flow for two approaches to Cu cleaning is described in Figure 1.

In this paper, various Cu pre-bonding cleaning chemistries have been compared for their ability to (1) remove copper oxides, (2) remove BTA films,

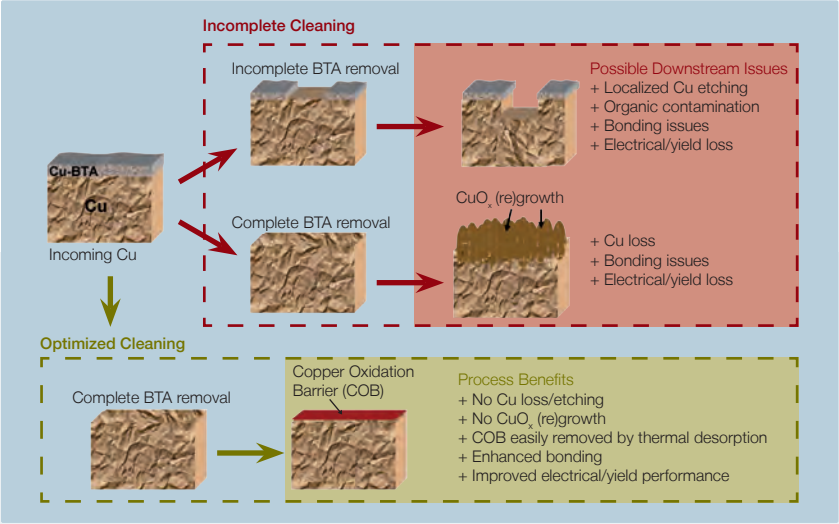


Figure 2: Comparison between incomplete and optimized BTA removal from Cu surface using EKC chemistries[1]

(3) remove a combination of BTA in the presence of thin copper oxides and (4) add copper oxidation barrier (COB) functionality to prevent Cu oxide (re)growth.

Benzotriazole (BTA):

Benzotriazole (BTA) is commonly used to protect Cu surfaces in wafer fab CMP processes. It can be found in the polishing slurries to prevent copper corrosion and static etching during the CMP process. It is also added to interstation rinse steps in the CMP tool to ensure copper protection as the wafers are processed. In wafer fab processing, the BTA needs to be removed prior to subsequent liner deposition steps as part of the copper metallization process. One of the goals of the Cu post-CMP (PCMP) cleaning step is to remove any residual BTA left on the wafer surface. However, not all commercially available PCMP cleaners can completely remove the BTA film. On the other hand, if the Cu PCMP clean step completely removes the BTA film, the copper is very reactive towards the environment and can grow copper oxide rapidly. Therefore, the result would be wafers leaving the wafer fab with significant Cu oxide growth. It therefore becomes critical to protect the Copper surface using a COB (copper oxidation barrier) during the queue time between cleaning and bonding. A direct comparison between incomplete vs. complete/optimized removal of BTA from the Cu surface is shown in Figure 2.

Copper Oxidation Barriers (COB):

Copper oxidation barriers (COB) allow protection of the cleaned copper surface from environmental contamination including copper oxide growth. The previous Figure 2 shows that in a typical Cu cleaning process when BTA is completely removed from the Cu surface, the bare copper can quickly grow undesirable Cu oxides. The optimized cleaning process flow illustrates how DuPont/EKC Technology cleaners solve the technical need of protecting the cleaned copper surface with a COB. The COB forms a thin organic layer that prevents the formation of copper oxide. Typically, the layer is deposited on an oxide free copper surface from the cleaning solution and can keep the Cu surface from oxidizing for more than 24 hours.

BTA AND COPPER OXIDE REMOVAL STUDY

Contact angle measurements and FTIR-RAS Measurements:

In order to see the effect of BTA removal on Cu surface, cleaned Cu wafer pieces were contaminated with a BTA solution (0.1-1.0%) and then cleaned using different EKC chemistries. The Cu surface was then measured using Fourier-Transform Infrared Reflection Absorption Spectroscopy and contact angle. A simple and common way to measure BTA presence and removal from a Cu surface is through contact angle measurements using DI water. Pristine copper typically has a low contact angle in the range of 15-30° and is hydrophilic. When BTA is added to a cleaned copper surface, the surface becomes hydrophobic and the contact angle increases significantly to >60°. Figure 3 shows this effect on contact angle

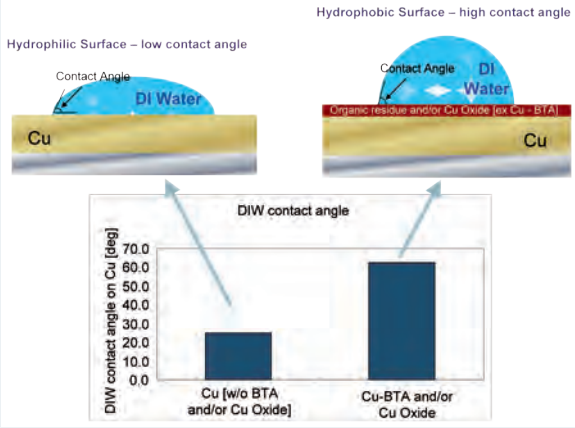


Figure 3: Test for BTA and Cu- oxide removal performance. While pristine Cu has a contact angle < 30°, Cu with a BTA layer has a contact angle in excess of 60°

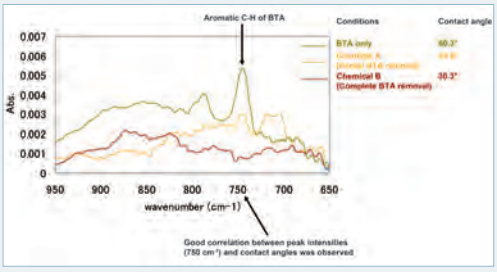


Figure 4: Surface sensitive FT-IR (RAS) data for BTA treated Cu wafer, partially cleaned wafer and wafer with BTA completely removed.

measurements. In addition, FT-IR-RAS can be used to do Cu surface analysis for BTA presence as shown in Figure 4. A good correlation between peak intensities from FT-IR-RAS and contact angle measurements was observed.

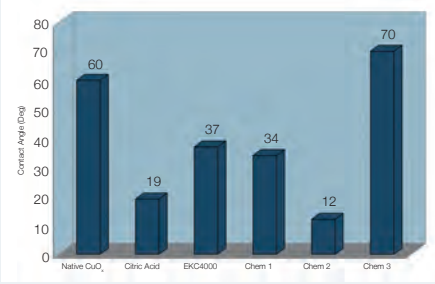


Figure 5: Contact angle measurement comparison for removal of Cu Oxide from Cu Surfaces with different clean treatments.
Chemical Conditions = 30sec @ Room Temperature (Puddle)

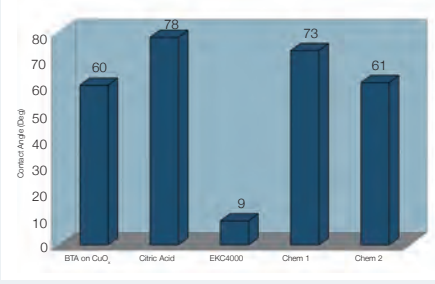


Figure 6: Removal of BTA on Cu Oxide from Cu Surfaces with different clean treatments shown in terms of contact angle measurements

<u>Oxide Removal Comparison:</u>

Prior to any bonding tests, DuPont/ EKC Technology Cu cleaning chemistries were tried at SUSS site and screened for efficiency in removing thin and thick copper oxide films and BTA films on both bare Cu and thin copper oxide. Various other chemistries including existing processes of record (PoR) including citric acid were compared to the EKC chemistries. Contact angle testing was used for this study. All cleaning solutions were run at room temperature for 30 seconds in a static beaker environment and contact angle measurements were taken immediately after the clean step. The electroplated Cu wafers used for this testing simulated the type of oxide that is typical of wafers that would have received Cu depositions a few days to weeks prior to the bonding.

In addition, some Cu substrates were deliberately oxidized by exposure to oxygen at 300ºC for a few minutes. Contact angle measurements were then done to determine the surface energy of the oxidized wafers. Next, wafer sections were immersed in several wet chemistries, rinsed in DI water and dried in N_2.

The contact angle data shows that the untreated Cu oxide has a contact angle of approximately 60°. Figure 5 compares the various chemistries based on oxide removal rates as evident from contact angle measurements. Several chemistries appear to be successful at removing the Cu oxide as evidenced by the contact angle reduction to the 15-30° range. Citric acid provided the lowest contact angle, with EKC4000™ and several other chemistries achieving a lower contact angle.

<u>BTA Removal Comparison:</u>

BTA removal was also tested on both bare Cu and thin Cu oxide films. While BTA is less effective on oxide surfaces compared to bare Cu, it is still useful for simulating BTA and Cu Oxide that can both be present on incoming Cu surfaces due to ineffective PCMP cleaning. The BTA was coated on the surfaces by dipping the samples in a 0.01M BTA solution and rinsing, and the cleaning process was identical to the one used for the Cu oxide removal tests. BTA creates a nearly perfect phobic surface with a contact angle of 80-90 degrees. This prevents other species in the environment from attaching to the surface. Figure 6 shows the contact angle as a function of different cleaning chemistries. The contact angle of untreated BTA on Cu oxide is around 60°. The data indicates that only EKC4000™ was able to clean the BTA and Cu oxide contamination from the Cu surface, resulting in a very low contact angle of 9°. The other cleaning chemicals tested showed little to no improvement to the contact angle, indicating the BTA and/or Cu oxide films were still remaining on the Cu surface.

RUN NO	WAFER 1	WAFER 2	WAFER CONDITION PRIOR TO CLEANING/BONDING	POINT OF USE PRETREATMENT	BONDER IN-SITU TREATMENT	BOND PROCESS
1	Blanket Cu wafer with 200A Ti seed layer/ 1000A PVD Cu/3000 A of ECU Cu	Blanket Cu wafer with 200A Ti seed layer/ 1000A PVD Cu/3000 A of ECU Cu	„Aggressive“ Conditions. Wafers allowed to oxidize in high humidity environment at 80°F for 48 hours prior to cleaning and bonding	None	None	415°C/30min/30kN
2				EKC4000	None	415°C/30min/30kN
3				EKC570	None	415°C/30min/30kN
4				EKC5500	None	415°C/30min/30kN
5			„Standard“ Conditions. Wafers were used as received from vendor	None	Yes. Forming Gas	415°C/30min/30kN
6				EKC570	Yes. Forming Gas	415°C/30min/30kN
7				EKC4000	Yes. Forming Gas	415°C/30min/30kN
8				EKC5500	Yes. Forming Gas	415°C/30min/30kN

Table 1: Process matrix for wafers processed for Cu-oxide removal studies

BTA AND COPPER OXIDE REMOVAL: BONDING STUDIES

Once the screening tests for BTA and Cu oxide removal using contact angle measurements were completed, the most promising chemistries were chosen for the wafer bonding tests. Several candidates from DuPont/EKC Technology including EKC4000™, EKC5500™ and EKC570™ were investigated for Cu surface cleaning capability. 200 mm prime Si wafers with a deposited film stack of 200Å Ti/1KÅ PVD Cu/3KÅ electroplated blanket Cu were used for this study. The cleaning was done using a SUSS CL300 cleaner module (manual puddle dispense) on a XBC300 cluster platform while bonding was performed on a SUSS CB200 Bonder. The wafer was puddled with the selected chemistry for ~30 seconds without agitation followed by megasonics assisted DI water rinse/clean and IR assisted dry. The cleaned wafers were then mounted on a bond fixture and bonded with <30 minutes hold time between cleaning and bonding.

In order to pull a vacuum between the substrates inside the bond chamber prior to bonding, 100µm thick spacers were inserted between the two substrates prior to clamping them on the bond fixture. A total of 8 runs with varying pre-clean and bonding process parameters were made as shown in Table 1. The main cleaning splits had two different process conditions. The bonding was performed at 415°C/30kN with varying bond times for the two splits.
The first split (Runs 1-4) was an “aggressive” condition in which the copper wafers were left

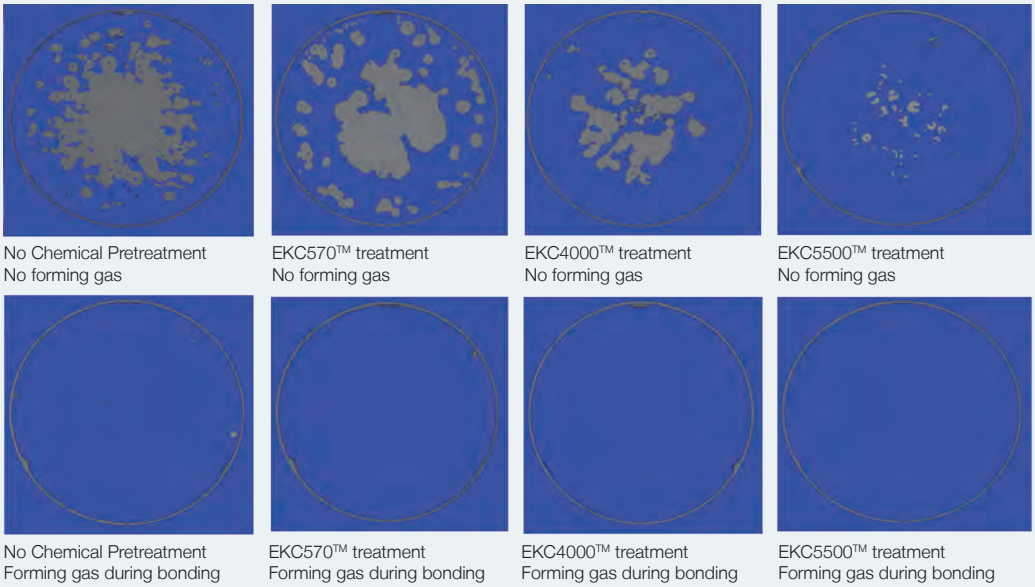
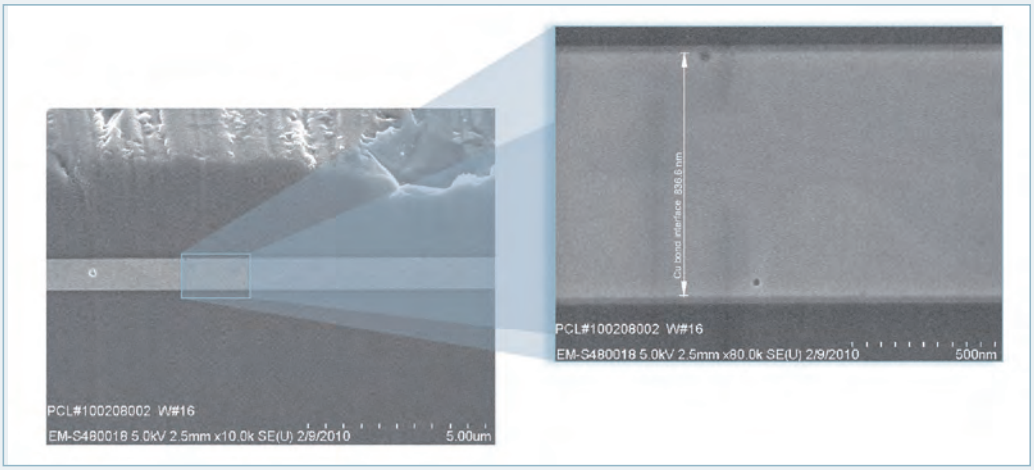


Figure 7: SAM images of Bonded blanket Cu wafers treated with different wet chemistries. The bonded pairs in the top row represent the “aggressive” condition in which the copper wafers were left exposed in a high temperature (80°F) and humidity open environment for 48hrs to enhance oxide growth followed by shortened bond time. The bonded wafers in the bottom row represent the “standard” conditions in which Cu oxide growth was not enhanced and forming gas was used.

Figure 8: SEM Cross-section of a bonded Cu blanket pair pre-cleaned with EKC5500 and bonded at 410°C/30 min. Each wafer has 200A Ti seed layer/ 1000A PVD Cu/3000A of ECU Cu.



exposed in a high temperature (80°F) and open humidity environment for 48hrs to enhance oxide growth; the bonding time was shortened to 15 minutes; and no forming gas was used during bonding. The second split (Runs 5-8) was the "standard" condition in which the wafers were used as-is from the vendor followed by point of use cleaning and bonding steps. Forming gas (95%N_2, 5%H_2) was used as the process/ overpressure gas for the "standard" split to aid with in-situ Cu-O_x reduction.

Scanning Acoustic Microscopy (SAM) was used to evaluate the effectiveness of bonding via focusing the ultrasonic transducer at the bond interface and looking for voids[3]. The SAM results for the bonded pairs from both splits are shown in Figure 7. Looking at the top row of images in Figure 7, the SAM images show a large area around the wafer center where voids were located (shown as white areas on the blue background) on the bonded pair with no wet cleaning treatment as well as with EKC570™ treatment. Improvement was seen when EKC4000™ was used as a pre-cleaning chemistry and the EKC5500™ sample exhibited significant reduction in voids. The bonded wafers in the bottom row represent the "standard" conditions in which Cu oxide growth was not enhanced. The results show that when using the "standard" conditions, the amount of voids seen during the bonding process is significantly reduced, as shown in the image with no wet cleaning treatment. The EKC4000™ and EKC570™ treatment resulted in much lower voiding, especially close to the wafer edge. Following the same trend as the aggressive split, the EKC5500™ exhibited the best performance resulting in a practically void-free surface.

Once it was established that Cu wafer surfaces pretreated with EKC5500™ exhibited void free bond interface, more bonding runs were done with the same chemistry to verify bonding at lower temperatures. The wafers were cleaned with EKC5500™ via puddle dispense, followed by spin rinse dry and forming gas was used as the overpressure gas prior to bonding to scrub any residual oxide inside the SUSS CB200 bond chamber. The bond process conditions were changed to 300°C/30 minutes/30kN. SAM results post bonding showed a void-free bond at 300°C. SEM analysis of the bond interface also showed a clean interface with excellent Cu diffusion as shown in Figure 8.

THE AUTHORS

Sumant Sood is Senior Applications Engineer for Wafer Bonders at SUSS MicroTec. His recent experience includes permanent and temporary wafer bonding process development for MEMS, LEDs and 3-D integration applications. He has authored more than 20 papers in wafer bonding and related areas. He received his B.Tech in Electrical Engineering from India and MS in Microelectronics from University of Central Florida. Sumant is a member of SEMI Standards committees on 3DS-IC and MEMS/NEMS and is a senior member of the IEEE.

Anthony Rardin received his BS in Agricultural Economics from the University of California Davis and his MBA from Golden Gate University. He has been with DuPont for 11 years and currently serves as Marketing Leader for DuPont Wafer Level Packaging Solutions.

Simon Kirk has been with EKC Technology (now DuPont/EKC Technology) for over 20 years, and has close to 30 years of semiconductor industry experience. During his time at EKC he has made contributions through multiple roles including applications engineering, marketing, new business development and new product development. Currently he is responsible for regional marketing and product management for the US and Europe, with an emphasis on advanced copper interconnect cleaning and surface preparation.

Generally the bond interface would still be visible with a low temperature bond, but proper POU treatments as well as insitu oxide reduction allow for proper interface recrystallization. Grain boundaries are visible across the interface at the twin planes in the high resolution SEM image.

The blanket Cu cleaning data seen so far is very promising. Ongoing work is underway to further evaluate the efficiency of the cleaning steps on bonding integrity. It is important to note that the above process runs involved running the CL300 with a manual puddle dispense. With cleaning runs in the automated mode, it is expected that there will be a significant cleaning enhancement due to the mechanical agitation and flow of the chemistry through a spray nozzle. Chemical cleaning capability testing with a fully chemical dispense system as part of the SUSS XBC300 system is ongoing. Studies to better characterize and generate processes of record for various cleaning chemistries are currently underway.

CONCLUSION

Out of all the wet chemistries that were evaluated as part of this study, EKC4000™ and EKC5500™ Cu cleaning materials resulted in very low void Cu-Cu bonds with additional advantage of copper oxidation barrier (COB) functionality to prevent Cu oxide (re)growth. Void-free bonding of blanket Cu-Cu wafers cleaned using EKC5500™ was successfully demonstrated at temperatures as low as 300°C. Further work with Cu-polymer hybrid wafers is ongoing to identify and optimize a complete Cu-Cu bonding solution based on both bond strength as well as electrical data. The electrical yields are above 90% in early R&D lots[3] examined so far. This work was done in collaboration with IMEC and used via last approach from front side of the device wafer using 200mm wafers processed in IMEC 0.13µm CMOS line with W vias and Cu damascene technology. In conclusion, several point of use cleaning options are available for surface cleaning of Cu and hybrid Cu/O_x interfaces before alignment and bonding. These treatments are compatible with both diffusion bonding and hybrid fusion bonding. These processes will become increasingly more widespread as 3D integration and packaging are adopted throughout the industries.

References

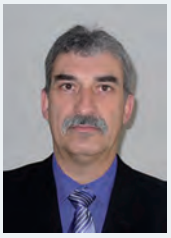
[1] P. Gueguen et al., Copper Direct-Bonding Characterization and Its Interests for 3D Integration, J. Electrochem. Soc. 156, H772 (2009)

[2] A. Rardin et al., "Enabling Thin Wafer Metal to Metal Bonding through Integration of High Temperature Polyimide Adhesives and Effective Copper Surface Cleans" IMAPS, 6th Device Packaging Conf. (2010)

[3] C. Huyghebaert et al., "Cu to Cu Interconnect using 3D-TSV and Wafer to Wafer Thermo-compression Bonding", 13th International Interconnect Technology Conference (2010).

[4] S. Sood et al, , "Metal Surface Preparation for Wafer Bonding with Point of Use Wet Chemistries", ECS Trans. 33, 17 (2010)

ADVANCED MEMS MANUFACTURING TECHNOLOGY



Erwin Hell, Technical Sales Support Manager for Asian Countries, is responsible for manual and automatic equipment (SUSS Bonder, Aligner and Cleaner) and located in Shanghai China.

Erwin Hell has been working with SUSS MicroTec since 1998. He started his career with the company in Engineering and Application for Bonder and Aligner. Erwin planned and carried out to success for SUSS MicroTec the set up of a position of Product Specialist. As a role of Product Specialist, he was responsible for the sales and machine configuration of Bonder in Europe and Asia. In 2007 he moved to Shanghai to take over sales and support activities for all Asian countries.

INTRODUCTION

MEMS technology is facing new challenges since thin wafer handling will be used more and more to archive smaller dies. Packaging the next device on the top of the first and so on called package on package (POP), reduces the wire bonding as the connections will be via through vias that run through the bulk silicon and such, the size of the second (third, fourth …) can have the same size as the first one. This means more space for the die but less additional work to connect the dies to each other.

Perhaps the most significant is the substantially larger market size and the drive toward lower costs. CMOS Image Sensors, Memory, Mixed Signals, FPGA (Flexible Program Gate Array), and Microprocessors are the utilized applications for thinned 3D wafers with interconnections. The bonding method therefore is thermo compression bonding with Cu-Cu bond layer material for the interconnections. Another method is fusion bonding. Both methods require very precise alignment accuracy. This precise alignment is very challenging, as the needed alignment is in the sub micron area.

ADVANCED MEMS BONDING REQUIREMENTS

New MEMS devices are intended for products that require much smaller sizes. This means the pitch to pitch is also getting smaller, resulting in a need for more accurate alignment to match the interconnections. This is a big challenge for the machine manufacturer as it means the machine has to work on submicron accuracy. To develop only new hardware isn't sufficient as the mechanic isn't able to work in that sub micron area. Special software was developed together with special algorithms to handle alignment in the submicron area.

DESIGN OF ALIGNMENT TARGETS

The design of the targets is important as well, as it will have a big influence in the final align and post bond accuracy. Figure 2 illustrates the design used to achieve best accuracy via automatic alignment with the vision system.

The illustrated design was also chosen because of a recommendation from Cognex for their PatMax® system which was used in the SUSS BA300UHP. The design was important for implementing all necessary parameters for the vision recognition system.

Figure 2: Alignment Targets

The MEMS industry will use smaller pitch and therefore need higher alignment accuracy to achieve functional interconnect dies.

ALIGNMENT TECHNIQUES

Different types of alignment techniques were used to test and get the best accuracy out of 300mm wafers. BSI (bottom side microscope) couldn't be used, as the second (lower wafer in the aligner) wafer didn't have alignment targets on the non bond surface. IR cannot be used for all wafers, as the wafer can have thick oxide or can be highly doped, meaning the wafers aren't IR transparent. ISA (inter substrate alignment) was best, as the microscope doesn't need a back side target nor an IR transparent layer. The ISA microscope moves in between the upper and lower wafer after loading them into the aligner. Both targets (upper and lower) are live images and can be seen at all times during alignment. While the upper wafer is fixed on the chuck and the left and right microscope show the targets on the monitor, the lower wafer mounted onto the alignment chuck via vacuum can be moved in all directions like X, Y and theta. SUSS BA300UHP (ultra high precision) was used for the test. To achieve very precise movement, together with very complex software control and last but not least target design for automatic pattern recognition shown in Figure 1. The z movement is a critical part in that the lower wafer has to move up to the cap wafer as it's also covered via software. A self calibrating system is also part of the software and improves the alignment reliability. After the alignment the fixture (Figure 3: wafer carrier) moves with the aligned wafer stack from the aligner into the bonder for final bond (depends on bond type as it is not necessary with fusion bonding because this method needs annealing in a Furness).

Figure 1: SUSS BA300UHP

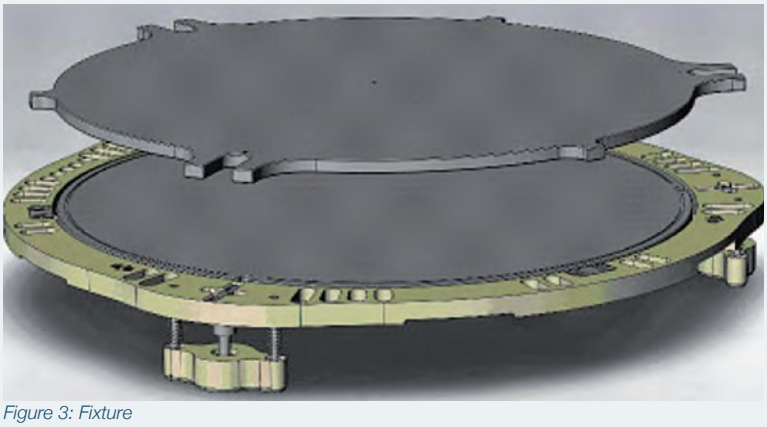


Figure 3: Fixture

ADDITIONAL CONSIDERATIONS

The alignment is one component which has to be taken care of by the machine manufacture. Another is the handling of the wafer, as it can influence the accuracy as well. For fusion test it was not necessary to transport the aligned wafer stack as they were pre bonded right after the alignment. For Cu-Cu bonding it was necessary to transfer the aligned wafer stack from aligner to bonder. Therefore, the fixture (wafer carrier shown Figure 3) must take care of the aligned stack and protect against any movement during transfer. Also, the area where the aligned wafers are held during transport and bonding is important. The fixture shown in figure 3 illustrates a full area for a 300mm wafer stack.

101230 (GCD)					
			3-SIGMA		
X µm	Y µm	T mDeg	X	Y	T
0.149	0.154	0.053	0.174	0.252	0.040
0.076	0.088	0.033			
0.104	0.155	0.038	RANGE		
0.176	0.153	0.034	0.233	0.406	0.048
0.218	0.257	0.051			
0.133	0.083	0.048	MAX / MIN		
0.083	0.068	0.039	0.268	0.240	0.087
0.143	0.049	0.052	0.035	-0.166	0.039

Table 1: Alignment accuracy results

SUMMARY

The MEMS industry will use smaller pitch and therefore needs higher alignment accuracy to achieve functional interconnect dies. At the test with the SUSS BA300UHP alignment for thermo compression bonding in the BA300UHP <350nm, post bond alignment accuracy could be achieved for a Cu-Cu 300mm Si wafer stack and <200nm was achieved for fusion pre bond. This achieved accuracy is even greater than the industries' needs at this time. Looking forward to sometime in 2012-2013 when the achieved accuracy will be needed as shown by several semiconductor forecast magazines like Yole reports.

References

1. Cognex Headquarters
Cognex Corporation
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2. SUSS MicroTec,
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APPLICATION OF THE SUSS ANGULAR EXPOSURE SYSTEM TO FABRICATE TRUE-CHIP-SIZE PACKAGES FOR SAW DEVICES

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EXAMPLES FOR EXPOSURE OF VERTICAL SIDEWALLS

SAW filters are key components for mobile communication. Size reduction of SAW filters allows for further miniaturisation of mobile phones and an extension of their functionality[1-3]. The miniaturisation of the devices demands also a reduction of the package size. To address the packaging requirements EPCOS has developed the Die Sized SAW Package (DSSP), a true chip-size wafer level package for SAW filters. The key for the realization of this package are the 3D-interconnects.

COATING SOLUTION: SPRAY COATING

For high topography wafers, good resist thickness uniformity is necessary for the subsequent process steps, which cannot be achieved with spin coating. Lamination of dry film resist is also not suitable because the topography of the packages is too high and the trenches between the caps are too narrow to allow a good conformal lamination. Spray coating is developed for high topography coatings[4-6] and this method is applied for the customized lithography step, which is described in this paper. Negative tone resists and lift-off resists have been evaluated, but for these resists the coverage of the upper edges is not sufficient. With positive tone photo resist, the coated film uniformity meets the required coating uniformity.

TECHNICAL SOLUTION WITH MASK ALIGNER

The spray coated resist provides a nearly conformal layer that has to be exposed. As the interconnects are running across the sidewalls

the photo resist needs to be exposed and developed completely in these areas. For the standard perpendicular exposure the effective resist film thickness corresponds to the topography depth (Figure 1), that can be easily 10 times the film thickness on the even planes.
For positive tone resist it is essential to expose the complete film layer from top to the wafer surface to make sure that the exposed areas can be developed completely. Chemically amplified resists seem to solve this problem, but even for

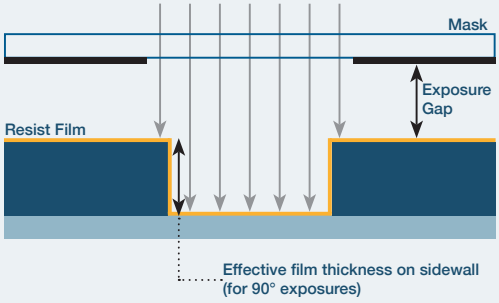


Figure 1: Standard perpendicular exposure of deep trenches and vertical sidewalls

these resists the thickness (corresponding to the sidewall depth) might be too high. If the wafer is exposed with light of an inclination angle of 45° the effective film thickness is nearly uniform across the resist surface. The film thickness on the vertical sidewalls is only 1.4x of the nominal

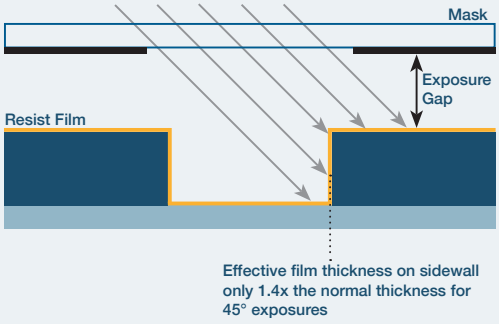


Figure 2: Angular exposure of deep trenches and vertical sidewalls

film thickness (Figure 2).
Due to the inclination angle of the exposure light the shape of the exposed area changes from a circular area for 90° exposure to an ellipsoidal shape for angular exposure. The diameter in y-direction gets larger while the diameter in x-direction decreases. Thus, the angular exposure is possible only for wafers up to 150mm, while the 90° exposure is possible for up to 200mm wafers.
The possibility of angular exposure with inclination angles of 45° and 60°, respectively, is an additional option to the standard perpendicular exposure of wafers. As the optical system itself needed some changes, no upgrade is possible for mask aligners in the field. Additionally, these changes need an increasing of the housing in the front and at the side. Therefore, the footprint of the MA200Compact with angular exposure option is slightly larger then the standard machine.

EXPOSURE EFFECTS: SHADOWS AND REFLECTIONS

As already explained the angular exposure system is used for exposing wafers with high topography structures. The high topography structures are leading to shadow effects due to the inclined light flow and some areas are not exposed. For this reason the wafer needs to be turned by 180° to expose the other side, or 4 times by 90° to expose all sidewalls. Up to 4 exposures will be necessary to structure the interconnects at all sidewalls. For proper exposure of all interconnects accurate alignment is essential.
Reflections from the pattern of the opposite side increases the exposure dose in areas close by the sidewalls of the structures. This has a severe influence on the CD control. The design rules for the mask layout therefore have to compensate this effect.

CHANGES IN ALIGNMENT PROCESS

The alignment process is slightly different from standard proximity printing. With standard perpendicular exposure the position of the exposed structures does not change compared to the mask positions.

For angular exposure, the printed image in the resist is shifted compared to the original position. The shift depends on the exposure gap (Figure 3). It could reliably be predicted by geometrical considerations from the exposure gap and the inclination angle. This has to be noted and can be corrected either by adjusting the mask layout or by using the off-set function in the alignment software.

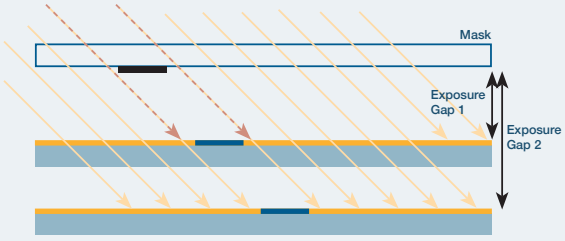


Figure 3: Schematic illustration of pattern printing shift caused by angular exposure

The dependence of the alignment accuracy on the exposure gap requires a precise control of the exposure gap. Due to the strong gap dependency the alignment accuracy is approx. +/-5µm for the angular exposure while it is +/-0.5µm (direct alignment) and +/-1µm (standard alignment), respectively, for perpendicular exposure. Any unevenness or particles between chuck and wafer changes the exposure gap and thus influences the alignment accuracy.

PERFORMANCE OF THE ANGULAR EXPOSURE SYSTEM

The light intensity and the light uniformity across the exposure area are comparable to the standard exposure system. For measurement of the light intensity a special probe holder is used that tilts the probe surface towards the inclination angle to keep the measurement error small.

The resolution results are in the same range for the angular exposure system as for the standard

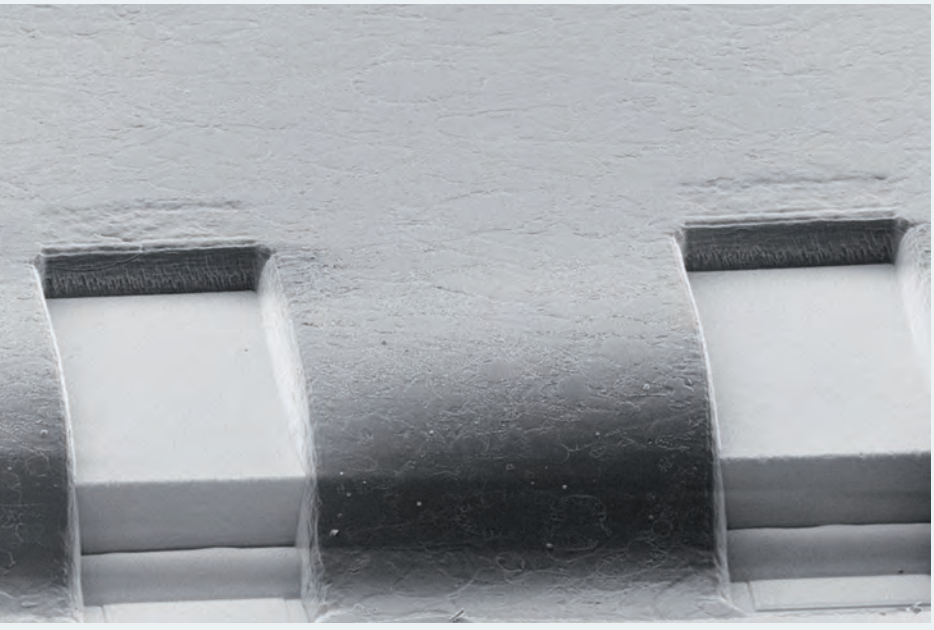


Figure 4: SEM image of spray coated, exposed and developed resist pattern for the metal interconnect

Figure 5: Successfully processed metal connects

perpendicular exposure. The Figures 4 and 5 demonstrate successfully processed interconnects after lithography and after metal patterning for the DSSP package, respectively.

SUMMARY

SAW components require low cost, small size, high reliability and good electrical performance. These requirements do not only relate to the SAW component itself but also to its packaging. True chip size packaging as DSSP meets these reqirements but poses a challenge to the photo-lithographical process due to its packaging caused topography.

For high topography structures like true-chip-size packaged SAW devices 3D-lithography is required. Conformal coating of such high topography wafers is solved by spray coating of positive tone resist.

For the exposure of the interconnect structures on the vertical sidewalls of the package, SUSS MicroTec and EPCOS developed a solution for this challenge with the angular exposure system.

The inclination angle gap exposure causes a shift in the print that can be corrected by the mask layout or by the offset parameters of the alignment software to achieve accurate alignment. As the shift depends on the exposure gap, the correction factor needs to be calculated by geometrical considerations. For exposure of all sidewalls of the structures, up to 4 exposures are necessary.

Realization of the metal connects for high topography structures on the wafers is done successfully with SUSS lithography equipment. Simulations and experimental resuslts proofed the fulfillment of the requirements of the DSSP and the processing technology successfully.

References

[1] P. Selmeier, R. Grünwald, A. Przadka, H. Krüger, G. Feiertag and C. Ruppel, „Recent Advances in SAW Packaging“, Proc. 2001 IEEE Ultrasonic Symp., pp 283-291

[2] Robert D. Koch, Martin Schwab, F. Maximilian Pitschi, J'urgen E. Kiwitt, and Robert Weigel, “Ultra Low-Profile Self-Matched SAW Duplexer with a Flip-Chip HTCC Package for W-CDMA 2100 Mobile Applications” Proc. IEEE Int. Mirow. Symp., 2009

[3] G. Feiertag, H. Kruger, and C. Bauer, “Surface Acoustic Wave Component Packaging,” in European Microelectronics and Packaging Conference, 16th, June 2007, Oulu, Finland

[4] K. Fischer and R. Süss, “Spray Coating – a Solution for Resist Film Deposition across Severe Topography” Proc. Semicon West, July 2004

[5] K. A. Cooper, C. Hamel, B. Whitney, K. Weilermann, K. J. Kramer, Y. Zhao and H. Gentile, “Conformal Photoresist Coatings for High Aspect Ratio Features” Proc. IWLP Sept. 2007

[6] K. Cooper, K. Cook, B. Whitney, D. Toennies, R. Zoberbier, K. J. Kramer, K. Weilermann and M. Jacobs, “Lithographic Challenges and Solutions for 3D Interconnect” Proc. IWLPC 2008

Barbara L'huillier joined SUSS MicroTec as application engineer for mask aligners in October 2006. In 2009 her field of activity was extended by spin coaters. She received her diploma in electrical engineering from Ulm University, Germany, in 2002 and her PhD degree from Ulm University in 2008, working with GaN light-emitting diode structures on semi-polar crystal planes

Michael Jacobs joined SUSS MicroTec Lithography GmbH as an applications engineer for coaters and spray coaters in December 2003. In 2008 he changed his activity to bonder applications, from 2010 he was focusing on fusion bonding and temporary bonding working at SUSS MicroTec Inc., USA. Since September 2010 he has been working for SUSS MicroTec Sternenfels. In Sternenfels his field of activity is working for permanent and temporary bonding. He obtained his degree as an engineer for physical/medical technology in 2003 from the University of Applied Sciences in Aachen, Germany, working on manufacturing and characterization of microelectrodes for the integration in microanalysis systems.

The strategic collaboration agreement with Cornell University's NanoScale Science & Technology Facility (CNF) was signed in late 2010. As part of the agreement SUSS MicroTec installed a SCIL Nano Imprinting toolset and MO Exposure Optics for evaluation on a MA/BA6 as well as a Gamma system including spray coater. Within the collaboration CNF has also the opportunity for process demos with the SUSS MicroTec equipment installed at Cornell.

COLLABORATION AGREEMENT WITH CORNELL NANOSCALE SCIENCE & TECHNOLOGY FACILITY (CNF)

INTERVIEW WITH DONALD TENNANT, DIRECTOR OF OPERATIONS

In 2006 Donald Tennant was named Director of Operations at the Cornell Nanoscale Science and Technology Facility (CNF) after a 27 year technical career at Lucent Bell Labs. At Bell Labs he was a Distinguished Member of Technical Staff where he managed the Advanced Lithography Group. He is an expert in the area of high resolution electron beam lithography and related nanostructure technology. He is a Fellow of the AVS and also the Executive Vice President for the International Conference of Electron, Ion, and Photon Beams and Nanotechnology (EIPBN). His focus at Cornell's CNF is to lead this comprehensive nanofabrication and characterization facility into new and expanded areas of technology in order to offer frontier capabilities to researchers.

What is your role within Cornell and how are you linked to this cooperation?

Tennant: I am Director of Operations for the Cornell NanoScale Science and Technology Facility. I work with Dan Ralph, the Director, to manage all aspects of the facility and staff. In early discussions with SUSS MicroTec we recognized that both our equipment needs and our mutual interest in developing technology solutions would benefit from a broader interaction. So both sides worked hard to bring about this SUSS MicroTec/ Cornell cooperative agreement. Various CNF staff members have taken on responsibility for executing on the different technology developments and applications that were agreed upon.

What benefits does Cornell expect from this cooperation?

Tennant: We see it as a core responsibility at CNF that we seek out equipment and technology solutions for our large user community. The opportunity to work with SUSS MicroTec is a great example of how we are able to connect with a high tech equipment supplier and deliver both high quality "workhorse" systems as well as evaluate and improve on "frontier" technology for a wide variety of applications.

What are the goals (short and long term)?

Tennant: The short term goals of the program are to exercise and evaluate the new technologies such as SCIL, MO Optics, and AltaSpray. We hope to assist in developing processes that are useful for appropriately matched research applications. We also want to expose our large user base to the new possibilities that these tools offer while providing SUSS engineers with valuable data and feedback on their performance and

potential. Long term CNF wants to be prepared for the next decade of nanoscience and technology researchers. Many new initiatives are forming in nanomanufacturing and 3-D structures. University labs must be thinking about solutions to these new challenges.

How does the cooperation look in the daily work?

Tennant: Several CNF staff members have been assigned responsibilities to carry out the various studies that SUSS staff and CNF have prioritized on the various systems. In several instances we have enlisted graduate students as "CNF Fellows". These CNF Fellows have chosen technology projects that are aligned with their own research so they can both learn about technology solutions to their own work, and make steady progress on the experiments designed by staff supervising the work. Noah Clay from CNF is the principal point of contact for the overall project on the CNF side. He has been doing a great job of communicating results and helping to coordinate technical exchanges. Several of our staff recently assisted SUSS MicroTec with customer demonstrations on SCIL and the AltaSpray systems and we have a large group at CNF that assisted with a SUSS MicroTec / CNF Workshop held recently at Cornell to help interested users and potential customers with lectures and hands on demonstrations. The program has really ramped up in the past few months and I am pleased with progress.

How do current trends/developments influence the cooperation?

Tennant: We need to imagine how innovations and inventions made in the research lab can make it into society. Often times we concentrate so much on making one of something that we don't think about how to translate that into a solution to a societal or commercial need. The recent initiatives in the US in the area of nano-manufacturing are a recognition that we need to provide solutions that lower the barrier to commercialization. So working with suppliers who are interested in innovating and pushing the boundaries of fabrication is an activity we want to be part of.

Could you envision more cooperation opportunities coming up in the future?

Tennant: We are always open to cooperative agreements that bring value and good technology solutions to our users. There are advances in wafer bonding that we are learning about this week that might be an interesting area to explore, for example.

Would one of your students working on the project have a comment on their experience?

Tennant: Melina Blees is a graduate student in Professor Paul McEuen's group at Cornell University and one of our CNF Fellows involved the SUSS technology evaluation and she offered this comment: "…we're interested in using single-layer graphene to build three-dimensional "origami" and strong, truly nanoscale hinges. To do this, we need good control over the adhesion of graphene to its substrate, which can be achieved by reducing the contact area using nanopatterned substrates. These patterns should be between 10-100 nm in scale but still inexpensive and easily reproducible, which makes SUSS MicroTec's substrate conformal imprint lithography process an ideal tool for our purposes."

What is your personal conclusion?

Tennant: I really like it when a plan comes together. Working with SUSS personnel on this project has been great. It is clear to me that SUSS MicroTec is very engaged and motivated to make this program a success.

Attendees listening to technology lectures at the joint SUSS MicroTec/CNF Workshop held at Cornell University in Ithaca, NY.

SUSS MICROTEC IN THE NEWS

To read the entire press releases please visit www.suss.com/news

"We are looking forward to using their state-of-the-art research facilities for further developing our technologies. We are happy to offer our North American customers the option to have their application processes set up and tested in this environment."

Frank Averdung,
President and CEO,
SUSS MicroTec

SUSS MICROTEC ANNOUNCES COLLABORATION IN NANO RESEARCH WITH CORNELL UNIVERSITY

January 11, 2011

SUSS MicroTec announced a strategic collaboration with the Cornell NanoScale Science & Technology Facility (CNF), a university nanofab based in North America. As part of the cooperation, Cornell staff will perform research using SUSS lithography equipment, including enhanced contact aligner tool sets and a Gamma spray coater.

SUSS MICROTEC WILL BE INCLUDED IN THE TECDAX

March 7, 2011

SUSS MicroTec will be included in the TecDAX, the leading index for publicly traded German technology companies. The stocks are selected according to market capitalization and trading turnover. SUSS MicroTec has improved in both categories over the last 6 month and now moved up into this important index from Deutsche Boerse in Frankfurt.

FINAL FIGURES FOR 2010 FISCAL YEAR PUBLISHED

March 30, 2011

SUSS MicroTec AG published its consolidated financial statements for the 2010 fiscal year today. The figures show that the company experienced a clear increase in both sales and order entry in the past fiscal year.

PRECAUTIONARY MEASURES FOR MATERIALS SUPPLIED FROM OR THROUGH JAPAN

April 12, 2011

The SUSS MicroTec Group takes its responsibility for the safety of personnel as well as delivered systems very seriously. Our suppliers in Japan are mainly located west and south of Tokyo and signal safe and stable supplies.

SUSS MICROTEC INTRODUCES MASKTRACK PRO INSYNC, A SYSTEM FOR AUTOMATED HANDLING, STORAGE AND INSPECTION OF EUVL RETICLES EXPANDING THE MASK INTEGRITY INFRASTRUCTURE

July 13, 2011

Today SUSS MicroTec, a global supplier of equipment and process solutions for the semiconductor industry and related markets, launched its new MaskTrack Pro InSync - the first holistic in-fab EUVL mask management offering. MTP InSync is a stand-alone or clustered handling system which seamlessly synchronizes mask cleaning, handling, inspection and storage in a single controlled environment.

A WORLD LEADING INTEGRATED DEVICE MANUFACTURER (IDM) SELECTS SUSS MICROTEC AND TMAT FOR 300MM HIGH-VOLUME PRODUCTION OF 3D LOGIC AND MEMORY APPLICATIONS

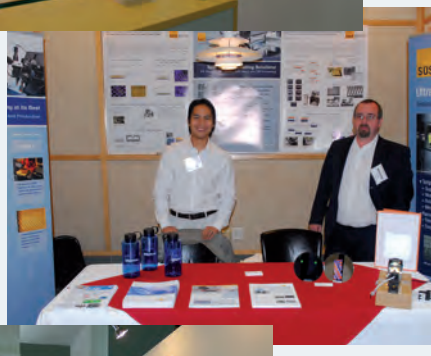
October 18, 2011

SUSS MicroTec and TMAT, a provider of process technology and adhesives for temporary bonding, have received a purchase order for SUSS MicroTec's latest generation of high volume manufacturing temporary bond clusters from a world-leading IDM.

TRADESHOWS AND CONFERENCES

Some of the opportunities to meet with SUSS MicroTec in the upcoming months:

TRADESHOWS/CONFERENCES			
	Tradeshow/Conference	**Location/Country**	**Date**
January			
	Photonics West	San Francisco, USA	Jan 21 - 26
	IEEE MEMS	Paris, France	Jan 29 - Feb 02
	IEEE International 3D System Integration Conference	Osaka, Japan	Jan 31 - Feb 02
February			
	Semicon Korea	Seoul, South Korea	Feb 07 - 09
	Strategies in Light	Santa Clara, USA	Feb 07 - 09
	SPIE Advanced Lithography	San José, USA	Feb 12 - 16
March			
	Optical Fiber Communication Conference and Exposition	Los Angeles, USA	Mar 04 - 08
	IMAPS Device Packaging	Scottsdale, USA	Mar 06 - 08
	MIG MEMS Executive Congress	Zurich, Switzerland	Mar 20
	Semicon China	Shanghai, China	Mar 20 - 22
April			
	Photomask Japan	Yokohama, Japan	Apr 17 - 19
May			
	Semicon Singapore	Singapore, Singapore	May 02 - 04
	IEEE Workshop Low Temperature Bonding for 3D Integration	Tokyo, Japan	May 22 - 23
	Optatec	Frankfurt, Germany	May 22 - 25
	ECTC	San Diego, USA	May 29 - Jun 01
	EIPBN	Waikoloa, USA	May 29 - Jun 01
	DGAO	Ilmenau, Germany	May 29 - Jun 02
June			
	Opto Taiwan	TWTC, Nangan, Taiwan	Jun 19 - 21



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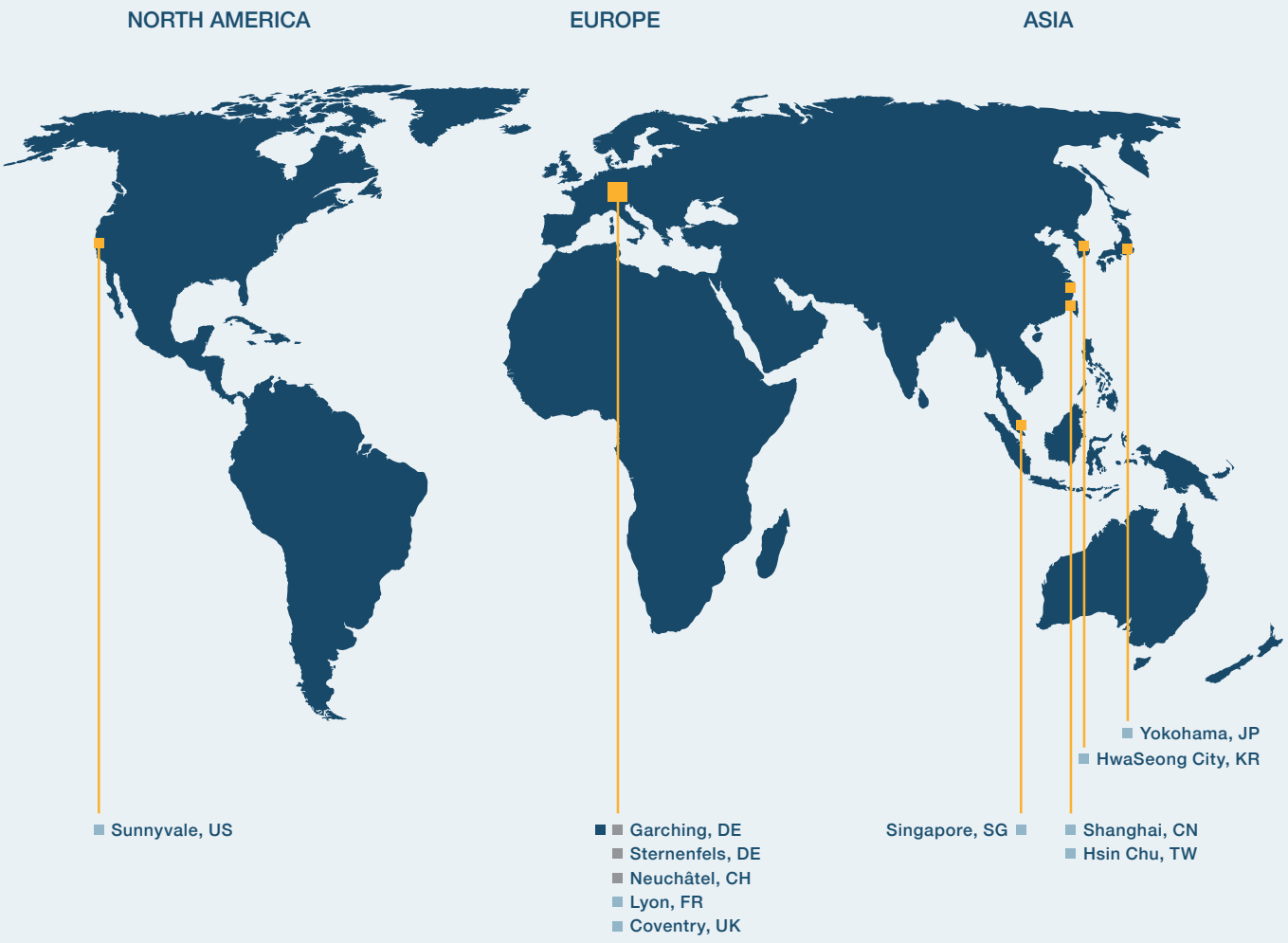

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