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# EDITORIAL

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Dr. Franz Richter, CEO, SÜSS MicroTec SE

"The only constant thing in the universe is change", Heraclitus once said. This quote is more than true for the semiconductor industry, these days maybe more than ever. Megatrends, like the Internet of Things (IoT), Autonomous Driving, Digitization and many more, require new semiconductor solutions. The fifth generation of mobile data communication, 5G, will allow for an extremely high speed of data transfer, allowing real-time connectivity. As a consequence, a huge amount of data will be created and subsequently need to be handled, stored and managed in very powerful, highly integrated smart electronical devices. The whole semiconductor industry as well as adjacent industries (Micro Optics, MEMS, RF, etc.) will grow with the trend towards highspeed connectivity in a digitized world.

We at SUSS MicroTec support those trends by developing and releasing new product solutions for all of our product lines. It is a big challenge, but it is also great fun to develop smart technologies by using our creativity and innovative power to find convincing solutions for our customers. Thus, we are creating and continuously developing valueadded equipment with improved capabilities.

We have just released an improved generation of our DSC300 UV projection scanner, an ideal solution for emerging packaging applications such as copper-pillar bumping and fan-out waferlevel packaging. It is the perfect example of our ability to drive technology to its limits and provide a best-in-class cost-of-ownership solution to our customers.

However, just providing equipment is not enough anymore these days, no matter how fast, customized and powerful the equipment is. There are other important elements to providing a comprehensive solution to our customers. Only with a complete understanding of the processes our customers are using, are we able to arrange for a convincing demonstration. Then, once we receive the order, the after-sales support starts with a successful operator training, closely followed by application and process support during and after installation. Last, but not least, we are offering more and more intelligence built into our tools by creating and managing critical process data in order to optimize the production outcome. In summary, we provide comprehensive solutions by offering a complete package of processsupport services that comes with the tool.

Exemplary in this regard is our Imprint Excellence Center located in Neuchatel – it houses a whole range of imprinting experience, from process development to series production. We are able to offer the complete process development infrastructure along with cutting-edge equipment technology. Nobody knows our machines and their capabilities better than we do, and it is our aim to pass this experience and expertise on to our customers and partners because we want to see them succeed.

The bottom-line is – no matter which disruptive wave the industry is facing – we are ready to manage the changes, to develop dedicated and customized technologies, and to support our customers as a complete solution provider.

With this in mind, I am happy to present the new annual issue of the SUSS Report and hope that the articles in here would be of interest for you.

Enjoy reading.

Richts

Franz Richter

# SUSS DISPENSE SYSTEM – AUTO CALIBRATION/SELF LEARNING

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The SUSS Dispense System (SDS) is a pressure based dispense system, which is used to dispense chemicals for coating and developer processes with a repeatability of  $\pm 1\%$  and an absolute accuracy of  $\pm 2\%$ . The system setup uses standard components and intelligent software algorithms to achieve precise dispense results.

To optimize this a new automated calibration and self-learning/self-optimizing algorithms needed to be evaluated and implemented, to simplify the system setup and maintenance in the field and also to improve the cost of ownership.

Now in the new update, the system intelligence is improved further with the complexity being taken away from the user. The system offers improved intelligence, stability and due to the increased tolerance to errors a significant reduction in time and effort for setup and calibration.

## AUTO CALIBRATION

The system is using a pressure based dispense and a flow sensor for accurate dispenses. These components together with the system behavior need to be calibrated in an optimal way to achieve precise and repeatable results.

The dispense behavior can be separated in three different phases:

#### 1. Start phase

- During the start phase the flow rate is ramping up to the flow set value, depending on system settings also including an overshoot at the beginning
- 2. Stable flow
  - Time in which the flow rate is as stable as possible
- 3. Stop phase
  - After stopping the system (closing valves etc.) the flow rate is ramping down, but there is still some amount which is dispensed even after stopping the system

The next picture shows these three phases with overdrawn start and end phases to better visualize the behavior in general:



Figure 1 Drawing dispense phases

To achieve the most accurate results the software needs to predict the optimal stop time, therefore not only the calibration of the components, but also the calibration of the system behavior is very important.

In the first version of the system, it was necessary to do all required calibration manually; now with the new version the change of parameters is handson. Every needed parameter can be changed in real time from dispense to dispense without any further steps. This dramatically reduces the time taken for the first setup of tools as well as the time to get the process running after any hardware change in the system.

The calibration for all required parameters can be done in an automated process. After starting the auto calibration only a zero offset and three dispenses are required to calibrate the system to a specific resist.

After starting calibration, the real time dispense graphs are shown (Figure 2).

After each performed dispense, the user is requested to provide the real measured amount in weight and density or amount in ml (Figure 3).

After this short procedure, the system is calibrated and ready for production. If the resist needs to be changed, then also by just repeating this procedure, the system can be taken back to production in little time.



Figure 2 Realtime dispense chart



Figure 3 User input for measured amount in calibration mode

# SELF-LEARNING

Caused by the pressure based dispense, the system is sensitive to temperature changes. In the previous version, this was compensated by the system by adjusting the dispense time. Now the software is one step ahead. Any variations in e.g. the clean room temperature will be compensated by self-learning algorithms, which actively adapt the pressure and therefore flow rate rather than the dispense time. Therefore, the system ensures consistent flow rate, resulting in a static dispense time.



Figure 4 Two dispenses without self-learning

#### SELF-LEARNING PRINCIPLE

The new software uses principles from machine learning to optimize itself from previous dispense results. Therefore, the software collects the quality (errors) in former dispenses and starts to train itself to predict better performance for future dispenses.

The optimization for future dispenses is started after at least three dispenses are performed. One issue of this optimization is overfitting (learn noise instead of real errors), this would result in a bad repeatability performance, as shown in the next picture (blue Gaussian distribution vs. red).

A Finite Impulse Response Filter (FIR) and an asymmetric filter is used to omit old recorded errors, which are not relevant anymore. This optimizes the adaption to temperature or viscosity drifts and limits the influence of statistical inaccuracy at the same time.



Figure 5 Second dispense with bad compensation by noise



Figure 6 Blue new worse Gaussian distribution

# EXPERIMENTAL RESULTS

The provided test results are showing the capabilities of the system. The system was calibrated using resist at 21.4 °C (room temperature), afterwards resist was cooled down to 19.5 °C, which is 1.9 °C delta from the temperature during calibration. The corresponding data can be seen in Figures 7-9. These results are presented to demonstrate the error caused by the temperature change and the efficiency of the new software. According to the new update, Self-Learning became effective after three dispenses.

As you can see in Figure 7, once the temperature is changed the previous calibration does not fit anymore. That's the reason for the jump in the 9<sup>th</sup>, 10<sup>th</sup> and 11<sup>th</sup> dispense. As mentioned earlier, the system learns the change in flow rate and error correction is activated after three dispenses (started at the 12<sup>th</sup> dispense). Thus, already after the fourth dispense, the error is just under 5 % and the system keeps close to the set value. In a real world application, a jump in the dispensed amount would not occur, as temperatures typically change slowly and the system continuously adjusts to the changing conditions.

The biggest advantage comes with the time taken for dispense, as shown in the next picture. Even after  $1.9 \,^{\circ}$ C of temperature change, the time taken for dispense is kept constant at +/- 100 ms with no compromise in the system specification.

In addition, a miscalibrated system will optimize itself automatically as shown in Figure 9, where a bad calibration (used on purpose) demonstrates, how the total amount is compensated to match the set value.

As you can see in the above graphs, the temperature has a huge impact on the system performance. Yet, the self-learning takes care of the changes and keeps the system within the specification i.e. 2% accuracy and 1% repeatability.



Figure 7 Stable flow rate









Thus, without any extra effort needed for calibration, the system performs to its specification with almost no change in the dispense time.

# LOGGING

The SUSS dispense system is seamlessly integrated in the optional SUSS data logging concept. In case data logging is available, all dispenses can be reviewed offline using the viewing software. It is possible to see the flow behavior and the dispensed amount for each dispense, which were performed in the past.





#### SUMMARY

The SUSS dispense system is designed with the concept to make it universal and user friendly. Additionally, it supports automatic dummy dispenses in case of detected bubbles. The dispense system can be used between 3 ml to 25 ml with  $\pm 2\%$  accuracy and  $\pm 1\%$  repeatability. The system features great possibilities of monitoring and controlling of dispense in real time. This helps the customer to use various ranges of viscosities and let them optimize the whole dispense for process specific requirements. With the latest addons along with the existing exceptional system performance, the SUSS Dispense System now made a further step forward. The new system not only offers an improved user friendliness and stability against environmental changes, but also significantly reduces the time and effort required for system setup.

Björn Böckle studied Electronics and Information Technology at the University of Heilbronn. He graduated with focus on software development in 2002. After starting his career in the area

of digital image processing, he developed sensors based on optical coherence tomography (OCT) for Metrology applications whereby he collected first experience in the semiconductor industry. He joined SUSS MicroTec in 2011 as Lead Engineer Software Development. Since 2018 he holds the position of Manager R&D Software and is responsible for the software development for the bonder and coater product line.





# ADVANCEMENTS IN PELLICLE GLUE RESIDUE REMOVAL

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A pellicle is employed to protect a photomask from particle contamination. The pellicle is positioned at a distance from the photomask pattern such that particle contaminants are out of focus. To extend the lifetime of a photomask, the pellicle must be replaced when it becomes heavily contaminated or damaged. The replacement process generally consists of the following three steps, 1) removal of the existing pellicle, 2) cleaning of the photomask, and 3) installation of a new pellicle. The cleaning step is primarily required for the removal of pellicle-glue residue unintentionally left behind during the pellicle removal process. This cleaning step has traditionally employed aggressive chemistries, such as a long process cycle, utilizing a Sulfuric Acid and Hydrogen Peroxide mix (SPM). The major drawback from this approach is that it inadvertently exposes the photomask pattern to aggressive chemistries, risking CD shift, damage to sub-resolution assist features (SRAFs), and accelerated haze growth, thus, ultimately reducing a masks lifetime<sup>[1]</sup>. To overcome these shortcomings, this paper presents a localized approach for removal of pellicle-glue residue, which does not require long SPM cycles for post-clean.

#### 1. INTRODUCTION

The use of pellicles to protect photomasks from particle contamination during transport, storage, and use has greatly increased semiconductor device manufacturing yields. Nevertheless, the pellicle membrane must be exchanged after a certain number of scanner exposures (cumulative exposure dose), as airborne molecular contamination and residual ions, left on the mask during mask cleaning, often lead to haze formation on the backside of the mask and underneath the pellicle. Such contamination can adverse impact the optical properties of the mask, and must be removed [2a-e]. The pellicle frame is glued to the mask surface. The glue is often composed of organic polymers, which can have a wide range of polarity, from a-polar aliphatic chains to polar oxidized groups. The adhesion is usually promoted by chemical polarity gradients and threedimensional arrangement of the polymer chains. During exposure to UV radiation, further oxidation and/or cross-linking of these polymer chains can occur. The XPS plot in Figure 1 below shows increased oxidation of an olefin-based adhesive, which has been exposed to UV radiation<sup>[3]</sup>.



Figure 1 XPS image shows oxidation of olefin-based glue upon UV exposure; Oxygen 1 s peak is visible (right image)

In a common workflow, the photomask is exposed to several thousand joules of exposure energy at given wavelengths (i.e. 193i and 248i) before the pellicle frame is removed by means of a mechanical and thermal process, commonly referred to as de-pell, or pull-pell process. During the removal of the pellicle, a polymeric residue (glue residue) is left behind. These residuals must be removed before a new pellicle frame can be mounted.

A long SPM process, followed by physical force cleaning, utilizing megasonic and/or droplet spray technology have been employed over the past years to remove pellicle glue residuals after the de-pell process. Despite its good cleaning performance, elongated exposure of a mask to SPM is reported to lead to major drawbacks such as CD shift and haze generation. In addition, post SPM physical force cleaning may lead to SRAF damage. Both effects are carrying a high risk to shorten the life time of such masks [4]. Alternative wet and dry cleaning methods, such as CO<sub>2</sub> EcoSnow cleaning and laser ablation, have been proposed to overcome these issues [1, 5, 6, 7]. However, these methods come with their own drawbacks and have therefore not found their way into high volume manufacturing.

SUSS MicroTec, in collaboration with Micron Technology, has developed a method of localized pellicle glue removal, which overcomes the limitations of the current SPM based process of record (PoR) and is expected to extend the photomask lifetime. In this paper we present this novel method, resulting in highly efficient removal of the pellicle glue residuals without any impact to the pattern area. This method comprises a well-contained treatment of the glue residue with an organic solvent, while exposing the dissolving glue to a localized physical force. Chemistry selection and feasibility studies will be presented, along with production results, utilizing a fully automated glue removal module.

#### 2. EXPERIMENTAL

#### 2.1 EXPERIMENTAL WORK

Initial data on pellicle glue residue removal, focusing on chemical selection and system design optimization, were performed on a table-top ALPHA system, further described in chapter 3.2. Learnings from those initial studies were then transferred into a fully automated production system, which is further described in chapter 3.3.

Experimental and production data obtained from both systems, utilizing SUSS' novel localized cleaning approach, were compared to baseline data, obtained from today's commonly used PoR for pellicle glue residual removal, which is employing an extensive and aggressive SPM step. A SUSS MaskTrack X cleaning system was used to obtain the baseline data and was also employed for final cleaning of reticles after pellicle glue residual removal.

#### 2.2 CHARACTERIZATION

Visual bright-light (BL) inspection in a dark room was initially performed to judge the performance of the removal process, especially during chemical selection and feasibility test, utilizing the ALPHA module. During qualification of the fully automated production system, a LaserTec particle detection system was employed after visual BL inspection to quantify the difference between the common POR and the newly developed process. High-resolution pattern inspection data were collected to verify the process cleanliness.

# 3. EXPERIMENTAL RESULTS AND DISCUSSION

The development of our novel residual pellicle glue removal technology was divided into the following three main phases:

#### Phase I:

Chemical selection utilizing beaker tests

#### Phase II:

Feasibility studies utilizing an ALPHA test bench **Phase III:** 

Production verification utilizing a fully automated system

## 3.1 CHEMISTRY SELECTION

Beaker tests were performed to select a highly effective chemistry for the removal of pellicle glue residuals. Coupons from officially retired 193i production reticles were prepared, containing residuals of pellicle glue. The composition of specific pellicle glue on hand directed the choice of possible chemicals to non-polar or low polarity solvents. Dissolution normally takes place when the polarity of the solvent and the one of the polymers are similar.

After having tested more than fifty (50) formulations, a narrow group of five (5) solvents were selected as potential candidates. Considering physical properties, such as flash point, but also health and environmental concerns, we further reduced those candidates to only two (2) solvents to be entered into Phase II. Table 1 summarizes the main properties of the five (5) solvents initially selected and our final two (2) choices entered into Phase II.

Solvent	Activity on pellicle glue line	Flash point	Health/Fire/Reactivity
SOLMETA	ок	Below r.t.	-
SODIESTIS	ок	Around r.t.	
SOLVENT C	ОК	50 °C	
SOLVENT D	OK	44 °C	
SOLVERTE	OK	NON FLAMMABLE	

 Table 1
 Chemistry selection according to physical properties

 as well as health and environmental concerns

# 3.2 FEASIBILITY STUDIES

A table-top ALPHA module with the following features was built to study the local glue removal approach. The ALPHA module provided the following critical technology features:

- A nozzle for local dispense and suck-back of "strip" media, containing a wiper tape to support the glue removal
- ii) A nozzle for contact-free local "rinse" media dispense and suck-back to remove residual contamination
- iii) Two media dispense systems (one for each nozzle) with manually adjustable flow
- iv) Media suck-back systems utilizing vacuum with manual controllable pressure

With this setup, the solvent can make contact with the residual pellicle glue, but is contained to the immediate area surrounding the treated area. Such containment is critical as it prevents spreading of media containing dissolved glue into the pattern area, thereby avoiding the need for an aggressive final clean process. The local containment of the media is visible in Figure 2.



Figure 2 ALPHA module set up with rinse head contact-less and a strip head in contact with the reticle surface

Efficient pellicle glue removal was verified on reticles which underwent several thousand UV exposures in production prior to the glue removal process. Figure 3 provides an example of the results obtained.

Within these feasibility tests utilizing our ALPHA module, it was verified that Solvent C was the proper choice for effective pellicle glue removal. In addition, we found that a polar, water-miscible organic solvent could be used as rinse media.

## 3.3 PRODUCTION VERIFICATION

Utilizing the knowledge gained in Phase II (Feasibility Studies), a fully automated high-volume manufacturing pellicle glue removal module was employed for Phase III (Production Verification). This system, named MaskTrack X GlueBuster (GB), is providing the following critical technology features:

- A combined "strip" / "rinse" nozzle for local dispense/suck-back of strip and rinse media, containing a wiper tape to support the glue removal (manufactured utilizing 3-D printing technology)
- ii) A quickly exchangeable tape cassette
- iii) A first linear drive to automatically align the nozzle with pellicle specific glue line positions



Figure 3 ALPHA module results: visual BL inspection showed complete pellicle glue residual removal

- iv) A second linear drive to scan the nozzles along the glue line, proving multiple choices of scanning modes
- v) A surface contact force control system
- vi) A rotation stage with integrated mask-edge alignment system
- vii) A nozzle cleaning station

The tape fabric was carefully selected among a variety of vendors. It was found that intrinsic cleanliness and glue removal capability strongly depend on the material composition and structure of the tape fabric.

## 3.3.1 INTRINSIC CLEANLINESS

It should be noted that visual BL inspection is typically employed to verify the cleanliness of the surface area where the pellicle frame meets the mask surface. In a first pre-screening test, different tapes from several vendors were tested by wiping a Chrome blank (without solvent) and visually inspecting the area of tape contact utilizing BL.

The applied contact force was intentionally high in order to magnify any effect of tape impurities or abrasion. Prior to BL inspection, the Chrome blank has been subjected to a wet clean process. Table 2 summarizes the results.

To further quantify the results of our intrinsic cleanliness studies, we went beyond the normal inspection regime, utilizing LaserTec inspection to judge the performance of various tapes. Manual tests without process media and highcontact force were performed. Figure 4 shows the results of different tapes.

TAPE ID/VENDOR	EYE INSPECTION (BRIGHT LIGHT)
TAPE A, VENDOR 1	Surface highly contaminated
TAPE B, VENDOR 1	Surface highly contaminated
TAPE C, VENDOR 2	Surface looks clean
TAPE D, VENDOR 3	Surface contaminated
TAPE E, VENDOR 3	Surface highly contaminated
TAPE F, VENDOR 3	Surface contaminated
TAPE G, VENDOR 4	Surface highly contaminated

Table 2 BL inspection results of different tapes and vendors

Considering these results, Tape C was selected as the only choice for further testing.

In order to obtain final intrinsic cleanliness results utilizing Tape C in conjunction with the selected strip and rinse solvents, GB was used. The cleaning nozzle was moved along a pre-inspected photomask blank, having the tape in contact with the surface. Strip and rinse media flow rate,



Figure 4 Dry test results on Tapes A-E

contact force, arm speed, and motion modes were studied. High resolution particle inspection was used to visualize the particle distribution. After process optimization, about 90 defects were added to the mask surface per GB scan with tape C. All defects were located within the contact area of the tape and were smaller than  $2 \,\mu$ m. Figure 5 illustrates the defect distribution in relation to the scanned areas.

# 3.3.2 GLUE REMOVAL

The glue removal process was optimized varying the following process parameters:

- i) Arm scan speed
- ii) Type of arm scan mode
- iii) Media flow
- iv) Surface contact force

To perform a full pattern inspection on masks after pellicle glue removal, the localized removal of the glue was followed by a final clean cycle, employing a very short SPM step. In this final clean cycle, the SPM step time is reduced to only 7% of that used in the SPM based pellicle glue removal PoR. De-pelled reticle samples, which underwent tens of thousands to hundreds of thousands scanner exposures, were utilized to test the glue residue removal effectiveness.





For fast verification of glue removal results, visual BL inspection was used before and after glue removal, as well as after the final clean. The images in Figure 6 below illustrate clearly the removal of the pellicle glue utilizing the GB system.



Figure 6 Left image shows post de-pell glue line; middle image shows glue line removal after GB clean, and right image shows mask surface after final clean

To further quantify the glue removal performance, high resolution pattern inspection has been performed on the pellicle frame area to confirm these results. Figure 7 below provides one example of such inspection.

Very low-density, residual contamination was found after local pellicle glue removal, followed



Figure 7 Pattern inspection of 193i Photomask after GB treatment followed by a final clean

by the short final clean cycle outlined above. As mentioned in chapter 3.3.1, this area is usually not inspected at high resolution, hence baseline data for the original PoR (long SPM cleaning) is not available.

#### 3.3.3 PATTERN AREA IMPACT

A key point in the localized cleaning is to demonstrate that the presented method does not impact the photomask pattern area. To verify this, the following sequence was used:

- i) Through pellicle high resolution defect inspection of the mask's pattern area
- ii) Removal of the pellicle from that mask
- iii) Local removal of the pellicle glue, utilizing GB
- iv) Final clean of the mask utilizing the short cleaning cycle as described in chapter 3.3.3
- v) High resolution Die-to-Die (DTD) defect inspection of the mask's pattern area

Figure 8 is providing an example of the high resolution pattern inspection results obtained.



Figure 8 Left image, Defect map prior to pellicle removal. Right image, Defect map after GB followed by final clean

The comparison of both inspections revealed no added defect on the pattern area post de-pell and GB process, followed by the final clean, containing the very short SPM step.

# 3.3.4 FILM PROPERTY IMPACT

Film loss data were collected as well by cleaning the sampled reticles with different processes containing short SPM, long SPM (PoR) and no-SPM steps. Figure 9 shows the normalized data on change of Cr transmission, phase shift and phase shift material transmission in percentage collected on multiple plates. Figure 9 shows these results.

It's clearly visible that GB glue residue removal followed by SPM-free process is comparable to both Long SPM (PoR) and Short SPM processes with respect to film property impact. Minimal change of film properties post pellicle-glue residue removal and clean processes were observed. All results are well within specification.

# 4. CONCLUSIONS

The use of long SPM cycles for 193i pellicle glue residual removal has driven the industry to focus efforts in finding suitable cleaning alternatives. SUSS MicroTec, in collaboration with Micron Technology, has developed and optimized a novel pellicle glue removal technique combining local physical force with well contained media dispense and suck-back features. A single component organic solvent has been identified and qualified for efficient local glue removal. A fully automated pellicle glue removal system, called MaskTrack X GlueBuster, has been characterized in terms of intrinsic cleanliness, glue removal efficiency, pattern and reticle film properties impact. All results obtained meet or exceed current industry standards. Final clean after MaskTrack X GlueBuster process requires 95% less SPM time than the typical SPM based pellicle removal PoR. By eliminating long SPM cycles and incorporating different chemistry with new and innovative glue removal techniques, photomask lifetime can be potentially extended with less risk of haze growth



Figure 9 Film loss measurement for Cr transmission, phase shift change and phase shifting material transmission change

by not adding sulfate ions to the reticle surfaces. Additional development is ongoing to verify the long-time performance of reticles post no-SPM clean under wafer Fab environment and scanner exposures.

Davide Dattilo took his master degree in Chemistry in 2000 and his PhD in Molecular Materials in 2004. He gained experience in Surface Chemistry during his 3 years postdoc at the University of Padova, where he studied the basic reactivity of crystalline substrates such as Silicon and Gold.

He worked for 5 years in the R&D department of Molecular Stamping, a bio tech company where he has been responsible of the development of Surface Chemistry for the immobilization of organic molecules on solid substrates and passivation approaches.

Since 2012 he is Process Scientist at SUSS MicroTec, leading R&D projects for cleaning of optical and EUV photo-masks.



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# A SHARP LOOK INTO RESOLUTION

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Why is the definition of resolution for lithography tools not straight-forward?

Why this article? What is so complicated about resolution, one might ask. Lord Rayleigh published a paper on it already 145 years ago! Resolution is the smallest distance in which two point light sources can be distinguished as being separate. That's it!

But, is that really the truth? Can resolution be defined the same way for the challenges we are meeting in lithography every day as it is defined in microscopy? The answer is – as every Process Engineer knows – no. It gets even more complicated, since what is considered as resolved is dependent on the requirements of the processes which follow and therefore on the level in the resist at which resolution is assessed. Therefore, coming up with a definition of resolution which fulfils the expectations of the different processes from various technologies and which can be applied universally is a delicate task.



**Figure 1** Plot of the intensity of two point-like light sources at a distance equal to the Rayleigh Criterion. The dashed lines represent the intensities of each individual light source and the solid line is the sum of both intensities. The intensity at the center between the distance between two light sources, in order to be resolvable, as such that the maximum intensity of the second light source falls directly over the minimum intensity of the first light sources. Therefore the sum of the light sources together is nowhere higher as the intensity of one of the light sources alone.

# THE OPTICAL DEFINITION

Even if we go back to the optical foundations of resolution, the situation is not as clear as one might think. Lord Rayleigh's traditional physical or optical definition of resolution is focused on imaging with microscopes. His interest was to find a rule when two infinitesimally small, separate light sources can clearly be distinguished from one another. Rayleigh sets this limit at the distance where the diffraction pattern of the light sources interfere such, that the main maximum of the one source falls together with the first minimum of the second. Besides being a relatively arbitrary definition - and there were other, less successful definitions in the past - this definition is not truly fit to describe the situation in lithography.

As can be seen in Figure 1, with the defined distance between two point-like light sources, e.g. contact holes, the intensity in the center between the two points just drops by a little less than 30%. This is hardly enough contrast for a lithography process, which typically requires a contrast of 50% or higher.

In addition to this flaw, for our purpose to define resolution for lithography processes, the Rayleigh Criterion also does not state which features need to be resolved. Lithography resists have a finite thickness. As projection exposure tools and proximity exposure tools likewise have a specific depth of focus, the aerial images on the top and bottom of the resist can differ significantly. This is especially true for thicker resists. Figure 2 shows the lithography result that can be expected on top and on bottom of a 10 µm standard Novolak resist after exposure in a maskaligner at 20 µm gap. As can be seen from the simulation and as is commonly known, a significant difference in feature shape is to be expected between the top and the bottom results. In order to define the features resolved, each of the processes following will require that each individual feature is fully developed until the substrate-resist interface. It will also require that each feature which is isolated in the design is recognizable as an isolated geometry at the substrate-resist interface.

From our discussion so far, we can already define two basic rules for resolution in a lithography process:

- 1. the features are isolated from each other on the resist-substrate interface
- 2. the features are opened until the resistsubstrate interface

But, even when we simply look at the resist-air interface, things become more complicated. While many processes such as the electroplating of RDL traces and some etching processes use only 70 to 80% of the film thickness for the process steps which follow, some other processes such as solder bumping use the full height of the resist. This fact becomes even more important if we take feature sizes or L/S ratios into account.



**Figure 2** Example of a resist image in a  $10 \mu m$  thick positive Novolak resist as predicted by lithography simulation for a  $20 \mu m$  exposure gap. a) feature at resist top b) feature at resist top

#### WHERE TO MEASURE FEATURES

The Ravleigh Criterion itself does not state anything about the size of the resolved features but looks only at infinitesimally small light sources. This situation becomes even more complex if the actual feature size or the ratio between feature and space is taken into account for the definition of resolution. Even though the size of features is not at all part of the definition of physical resolution, it is sometimes requested to be included in the observation. From the point of view of the consecutive processes, features are only resolved if it is possible to create the desired features in the in the processes which follow. As mentioned in the previous paragraph, some processes, such as a consecutive wet metal etching process with high etching rate specificity, may only be interested in the feature dimensions at the substrateresist interface. Feature geometries at the top of the resist film are therefore of minor interest, since the resist is hardly attacked during the short metal etching times. Similar considerations apply for many electroplating processes, especially in bumping applications. Here the plating process is typically followed by a reflow process. Therefore, the dimensional accuracy of the features throughout the film thickness is of lower importance as long as the volume of the features can be kept stable within the plating height. Other processes, such as RDL plating, require a lot higher accuracy in feature fidelity at their respective CD size.



**Figure 3** Schematics of plating into different features. Features a) and b) contain the same volume of solder material. After reflow (c), the ball shape depends only on the volume and geometry of the UBM



**Figure 4** Resolved or not resolved? Schematic drawing of the influence of the resist profile and at which height in the resist the assessment is performed on the decision if the features are resolved

When assessing the feature ratio, the height level at which the sizes are measured is of high importance. Whether the measurement is performed at the top, center or bottom level of the resist film has an important influence on the process parameters and even the feasibility of the process. In combination with a specification about the minimum residual film thickness between resolved features and together with the behavior of the specific resist, a feature size requirement on the film center or even bottom can render a process impossible. This remains true, even if the same process may work when the specific feature would be measured at the resist top.

Figure 4 illustrates how the level in the resist where the resolution is measured influences the smallest achievable resolution if feature size ratios are taken into account for the definition of resolution. Figure 4 illustrates how the level in the resist where the resolution is measured influences the smallest achievable resolution if feature size ratios are taken into account for the definition of resolution. If a feature has a 1:1 ratio at the center level and is just fully developed while at the same time maintaining the full film thickness at the center between two lines, the same line cannot be resolved if the 1:1 criterion is assessed at the top or bottom of the resist. This behavior becomes more apparent when moving away from the perfect resist profile and to more realistic, nonlinear resist profiles.

Since the level where feature sizes are to be assessed depends strongly on the processes which follow, no general rule can be fixed on this metrology requirement. It therefore became common in the equipment industry to define a feature as being resolved if rules 1 and 2 are fulfilled while at the same time

3. the feature size ratio is roughly 1:1 at 50 % of the original resist film thickness.

This rule also found its representation as a recommendation in the SEMI standards. Test features are line-space structures, and the 1:1 requirement is applied only to the innermost 3 lines and the 2 space between these 3 lines. This requirement is based on the fact that resolving dense structures is harder to achieve than sparser feature groups. The crosstalk between the features, which can cause a slight increase of feature size, can be corrected by a slight size bias on the lines in the mask. A change in feature size between dense pattern groups and isolated features is not part of the resolution criterion but is a topic of CD uniformity specification, and will be discussed in a later article.

Additionally, most following processes require that as high a film thickness as possible remains between the developed features. Therefore, we furthermore define the remaining film thickness to be well beyond the specification of the Rayleigh Criterion and allow a resist erosion between developed lines of only 10 % in comparison to the film thickness at positions that are far off from the developed features.

4. Film thickness at spaces is equal to or greater than 90 % of the remaining film thickness after dark erosion

The more vertical the resist profile is, the less influence is expected from the level of the feature size ratio assessment. However, especially for higher film thicknesses, inspection of the feature size on any level but the resist surface can be heavily impacted by the aperture of the microscope used for inspection. Figure 5 shows the influence of the microscope aperture by comparing optical microscopy images from the top and bottom level of a resist film with a SEM inspection. Besides the general issue of recognizing 1 µm-sized features with optical microscopy, it is also obvious that the line opening at the bottom of the resist appears smaller in the microscopic image than at the top of the resist. However, the SEM image of the same structures proves that the sidewalls of the structures are almost vertical.

This effect is caused by the high numerical aperture of the objective. It leads to a misinterpretation of the feature size at the bottom of the resist. In order to avoid such artifacts during the inspection of resolution in a general test or commissioning situation, testing will typically be limited to a feature size inspection at the top of the resist. Assessment of the feature size at the center or bottom of the resist will require a SEM analysis which require significantly higher in effort.

The here discussed effects which influence the definition and inspection of resolution are for sure not complete, but give an understanding why a resolution definition which is applicable for all possible process requirements cannot be achieved. To have a definition which allows for a reliable commissioning and testing of machines despite following processes SUSS MicroTec fixes the resolution definition as follows, respecting the rules introduced so far:

# SUSS MICROTEC DEFINITION OF RESOLU-TION

Resolution is achieved if the following 4 parameters are fulfilled:

 All five lines of the SUSS standard test mask (or similar test structures on another mask) can be identified in the resist image at the resist-air interface



Figure 5 Images of 1 µm lines spaces features in a 1.2 µm thick positive photoresist a) microscopic image taken at the resist-air interface b) microscopic image taken at the substrate-resist interface c) SEM image of the same structures

- 2. All five lines are developed down to the resistsubstrate interface and show no interruptions along the feature length. However, the line width at the resist bottom is not assessed
- 3. The film thickness between the 5 lines is 90% or more of the film thickness in a large dark area. By default, this is assessed by an optical microscopic image. In the microscope image, the grey level in any space area appears at the same contrast level as the surrounding dark area. When in doubt, the film thickness must be assessed by SEM analysis or profilometry. Diffraction lines in the spaces may be present
- 4. The width ratio between the 3 innermost lines and the 2 innermost spaces is roughly 1:1

The following parameters are not part of the definition of resolution. Even though they might be important to qualify the general process capability of the machine, they are typically not part of the resolution criterion itself.

- Feature fidelity and CD uniformity: CD and CD uniformity need to be assessed at features sizes significantly larger than the resolution limit
- 2. Diffraction artifacts at the ends of features
- **3.** Line widths at the bottom and top of the resist as discussed in the article
- Differences between line widths in dense line-space structures versus in isolated lines. Such differences must be expected especially at the resolution limit and can be compensated for by biasing the mask feature sizes

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# CREATING PLANAR EMBEDDED RDL STRUCTURES WITHOUT CMP

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> Packaging technology is increasingly migrating to fan-out architectures, in many cases with multiple chips in a package. Current and projected designs require multiple redistribution layers, in some cases between 5 and 10 layers, with conductor linewidths down to  $2 \mu m$  and via openings below  $10 \mu m$  (Figure 1).



Figure 1 Multiple interconnect layers in µ-out packaging



Figure 2 Conductors patterned with photoresist which is stripped after patterning



Figure 3 Conductors embedded in polyimide

# THE HIGH DENSITY PACKAGING CHALLENGE

Traditional organic flip-chip substrates are encountering challenges to scale to these dimensions. Photosensitive spin-on dielectrics for via formation, together with RDL patterned with photoresist, face serious technical challenges, causing reliability and pattern integrity concerns (Figure 2). Free-standing RDL lines with <= 2/2 µm L/S size may cause electro-migration concerns and removing the seed layer from the narrow trenches is almost impossible or causes severe undercut to the RDL lines. The non-planar surface presents an additional challenge for the next redistribution layer, since it requires a larger depth of focus for the exposure system, which in turns limits its resolution capability. Finally, warpage of the substrate during processing is increasing with additional RDL layers, so careful selection of the material with respect to thermal properties is key.

# DUAL DAMASCENE PROCESS

A viable solution to overcome these challenges is to apply a dual damascene fabrication process to deliver an embedded RDL structure. This process is well known from CMOS fabrication in the front-end. A polyimide is patterned to create RDL trenches, but not stripped after development (Figure 3). A seed layer is deposited on the patterned and fully cured polyimide, followed by Cu electroplating to fill the trenches and vias. Since the seed layer is present everywhere on the polyimide surface, plating also occurs on the top surface as well as the trenches and vias. Once the desired features are filled, it is necessary to remove the excess Cu and seed layer, which is done using chemical-mechanical planarization (CMP) process. This CMP step adds complexity and cost to the process flow, and is a serious impediment for the adoption in advanced packaging.

To overcome these barriers, this article features a cost-saving dual damascene fabrication process to create embedded redistribution layers for fan-out packaging. This process uses mask based excimer laser ablation to pattern trenches and vias, a non-photosensitive dielectric with excellent thermal and resolution properties, and an innovative plating process that achieves planarization without the need for CMP. We report experimental results where RDL trenches were filled with less than 0.5 µm overburden, which is easily removed by a combination of de-plating and either wet etching or excimer laser ablation, with no damage to the embedded conductors.

# EXCIMER LASER ABLATION PATTERNING

One of the key enablers for the improved embedded conductor process is patterning of the dielectric layer by excimer laser ablation tool (Figure 4). This provides several important advantages over the photosensitive polyimide process:

- The dielectric material can be selected for its mechanical properties, thermal and chemical stability. The potential to use nonphotosensitive material gives access to a wider material selection and can help to significantly reduce material cost. The ability to use a wider variety of dielectric material will also provide relief on the wafer warpage
- The dielectric material is patterned after final curing rather than before, minimizing dimensional and profile changes and allowing smaller features
- The development step and the descum process are eliminated along with associated equipment and materials



Figure 4 ELP300 excimer laser stepper (SUSS MicroTec Photonic Systems)

- Vias and trenches can both be formed in one process step, requiring only a reticle change while the wafer is chucked on the tool.
- The technology can also be used to remove thin residual metal layers on top of a polyimide surface. This process step is critical to the successful creating of planar embedded RDL structures without CMP, as described later in this article

Excimer laser ablation patterning provides a unique flexibility not available in other patterning methods, and this flexibility turns out to be critical in making this process successful. This ablation process is available and validated for a variety of substrates, including panels.

# DIELECTRIC FOR EMBEDDED CONDUCTOR LINES

As mentioned above, the use of ablation patterning permits a choice of dielectric that is not restricted to photosensitive materials. For this work, we used FCPi-2100 polyimide from Fujifilm Electronic Materials. It exhibits excellent physical, thermal, electrical and chemical properties for this application, as shown in Table 1. The thermal stability is illustrated in Figure 5, showing negligible change in patterned feature size with baking. The thermal expansion coefficient can be modified to match a variety of substrates, including panels. It has also been shown to be compatible with a wide variety of solvents, acids and bases, including those which are likely to be encountered in the process flow.

CTE, (50-150°C)	28 (filled system) ∼ 56 (unfilled system) ppm/°C
Modulus	3.3 GPa
Poisson's ratio	0.31
Elongation-to-break	60 %
Tg (DMA by storage modulus)	247 °C
Thermal stability	2 % weight loss: 315 °C 5 % weight loss: 390 °C
Moisture uptake (80 % RH / 80 °C)	0.97 %
Dielectric constant / Dielectric loss (1-20 GHz)	3.2 / 0,015
Peel strength	1.3KgF/cm (before HAST) 0.6KghF/cm (after 500 hours HAST)

Table 1 Properties of FCPi-2100 polyimide (Fujifilm Electronic Materials)

#### METALLIZATION

Metallization involves two separate processes: vacuum deposition of a seed layer, and electroplating to fill the vias and trenches.

#### SEED LAYER DEPOSITION

The seed layer provides a current path to a contact at the edge of the wafer or panel during the plating process. However, it serves the equally critical function of providing adhesion between the underlying polyimide surface and the conductors which will be plated. Without good adhesion, delamination of the conducting lines and vias may occur after plating or during downstream process steps.



Figure 5 Thermal stability of FCPi-2100 (Fujifilm Electronic Materials)

For this process, the seed layer was deposited using an ASM NEXX Apollo PVD tool. Adhesion was guaranteed by the use of an Ar based inductively coupled plasma (ICP) etch before deposition to clean and activate the polyimide surface, and by depositing the Ti and Cu in the same chamber with no break in vacuum.

#### ELECTROPLATING

In previous versions of the embedded conductor process, CMP is required to remove excess metal deposited in the electroplating step. So, to eliminate CMP it is necessary to minimize the excess metal to the point where it is possible to remove it by simpler methods.

Using a modified version of a commercial TSV plating chemistry, an efficient bottom-up plating process was developed (Figures 6, 7). This process can fill trenches  $6 \,\mu\text{m}$  deep with overburden less than  $0.5 \,\mu\text{m}$ .

We can begin to understand the mechanism for bottom-up filling in this case in terms of TSV plating, although there are important differences, as we shall see. A TSV plating chemistry includes three organic additives: an accelerator, which catalyzes the deposition reaction; a leveler, which strongly inhibits this reaction; and a suppressor, which moderates the surface kinetics of the two other species. In TSV plating, bottom-up filling



Figure 6 2-3 µm trenches filled using bottom-up plating process

is achieved because the leveler, which is a slower-diffusing molecule, is initially present in much smaller concentration at the bottom of the via than at the top surface. So, the plating deep within the via is dominated by the accelerator, while plating is suppressed on the top surface and the upper parts of the sidewall.

For embedded conductor structures, the diffusion distances are a few microns at most, and aspect ratios are 1:1 or less. So, segregation of the leveler purely due to diffusion does not appear likely. However, the increase in effective surface area presented to the solution, from the sidewalls of the ablated features and the roughness of the ablated surfaces, may cause a modest increase in the initial consumption of leveler in these locations, plus a modest geometric buildup of



Figure 7 Surface evolution during plating showing bottom-up trench fill

accelerator as the Cu surface evolves. Once established, this can become a self-perpetuating process (Figure 8), with leveler-dominated plating at the top surface and accelerator-dominated plating in the ablated features.



Figure 8 Illustration of the "leveler depletion" hypothesis to explain bottom-up plating. (a) initial state, (b) at start of plating, (c) leveler and accelerator concentrations adjust, and (d) steady-state plating condition. The suppressor is not shown here

This plating process exhibits the phenomenon of "momentum plating", i.e. the deposition proceeds at a faster rate on the trench feature even after the trench has been completely filled. This phenomenon is also seen when the plating includes a via to connect two layers (Figure 9).



Figure 9 Cross section SEM of bottom-up plated dual damascene structure

# CHALLENGES FOR A PLANAR PROCESS

There are two critical challenges which must be met in order to provide a practical process. First, while the overburden is very small, it is not zero, and this metal, plus the original seed layer, must be removed before subsequent processing can occur. Second, the efficient bottom-up plating is very sensitive to the size of the ablated features. In our tests, trenches up to  $10 \,\mu$ m in width could be filled with a reasonably small overburden, but for  $15 \,\mu$ m and wider lines the fill was incomplete.

#### RESIDUAL METAL REMOVAL

The first challenge, removal of residual metal without CMP, has been demonstrated in two

different ways. In both cases, the metal removal begins in the plating step itself. Once the ablated features are filled, the plating current can be reversed. Nearly all of the Cu can be removed from the top surface without compromising the plated conductors themselves. This leaves a very small residue of Cu to be removed, along with the Ti adhesion layer. The second step, to complete the residual metal removal, has been demonstrated with two different approaches (Figure 10): either with a brief wet etch, or by excimer laser ablation. Although metal layers of 1 µm or greater thickness serve as an effective etch stop for excimer laser ablation, very thin layers on a polyimide surface can be efficiently removed. Either approach provides the desired savings in equipment and materials cost and process complexity from elimination of CMP.



Figure 10 Residual metal removal without CMP: deplating plus wet etch or ablation

#### FEATURE SIZE DEPENDENCE

In larger features, an efficient bottom-up plating becomes more challenging, since the concentration of the leveler at the bottom of the feature is significantly higher than in smaller features, which leads to a slower plating speed. A potential solution to this problem is to modify the surface texture of these larger features that allows the accelerator to dominate the plating process inside the patterned structures. We are currently investigating suitable methods for surface texturing that will allow preferential bottom-up plating in large features as well as small lines and vias. The plated features should ideally be nearly flush with the surrounding surface, so that, after application of the next layer of dielectric, a sufficiently planar surface is presented for the next sequence of RDL layer formation.

# SUMMARY

Planarization is an essential part of any multilayer RDL stack structure. Embedded conductors are a means to this end, but deposition processes to this point have included significant metal on the top surface, requiring CMP for removal. This not only represents an added expense in equipment and materials, but may be a barrier to panel applications. We have shown that, with the right combination of materials, patterning method, and metallization, an embedded conductor structure can be fabricated with minimal residual metal, which can be removed with simpler and less expensive techniques. One key aspect of this is the use of bottom-up electroplating, adapted from TSV processing.

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