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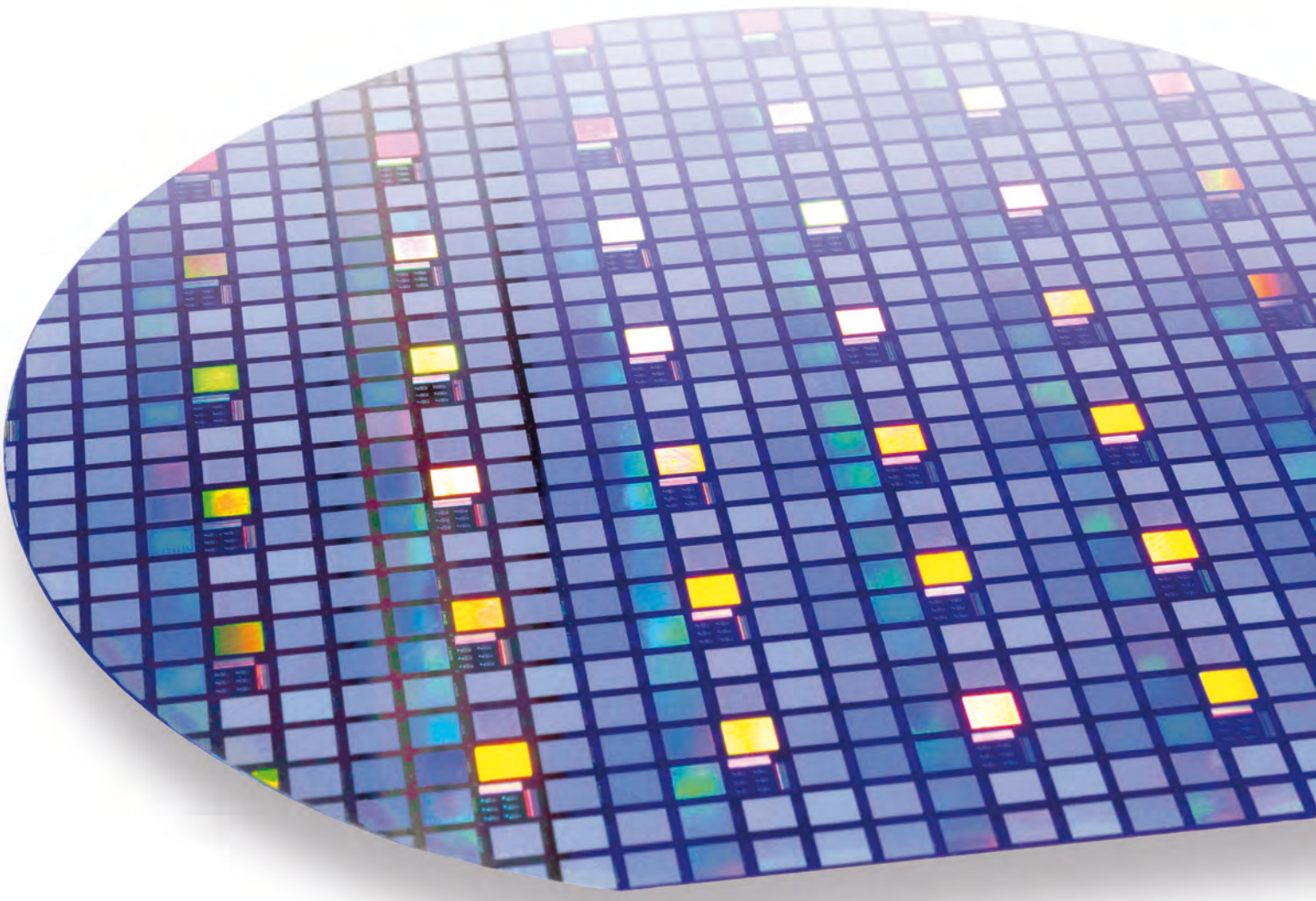
THE CUSTOMER MAGAZINE OF SUSS MICROTEC | ISSUE 2019



SÜSS MicroTec

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+ EDITORIAL

Dr. Franz Richter, CEO, SÜSS MicroTec SE

Dear Reader,

In the first weeks of each new year, we take the time to look back. It is an appropriate moment to reflect on what we have achieved over the last 12 months. 2019 was quite an exciting year for SUSS MicroTec. Driven by ongoing hot topics such as Brexit, China tariff disputes and Fridays-for-Future, world politics has undoubtedly set the course for many changes. Those changes have of course also strongly affected the dynamics and performance of the semiconductor industry – an industry already known for its volatility. A lot of developments also took place at SUSS MicroTec during this time. These dynamics confirm that we are on the right track with our strategy and must continue to orient ourselves accordingly. The top strategic priority for SUSS MicroTec over the next years is to move closer to our customers. It is our mission first and foremost to constantly identify technological trends and latest market requests, and secondly, to be ready to offer needed solutions, whether it is by introducing novel features to already existing and technologically proven SUSS equipment or by pushing boundaries to break new grounds.

With that said, I would like to welcome you to a new edition of our customer magazine, the SUSS Report. We are happy to share more about the new solutions, processes and developments which took place at SUSS MicroTec during the past year. This issue elaborates on the expansion of our product range with high-precision fusion bonding and on integrated metrology for precise process control e.g. in our automated permanent wafer bonders. Our extensive product portfolio contains the capability to serve multiple applications to meet the market's requirements such as increasing commercial interest in augmented reality solutions. Our SUSS MicroTec Imprint Lithography Equipment (SMILE) is a versatile tool to imprint both nano- and microstructures. Its imprint lithography technique is used to obtain high quality binary DOEs which are crucial for augmented reality. Or perhaps you are more interested in processing new materials, with excimer laser ablation of different polymers and their application for wafer and panel level packaging.

I would also like to mention a special occasion that took place in 2019: SUSS MicroTec celebrated its 70th anniversary. With seven decades of experience and maturity, we feel confident and equipped to overcome challenges of the coming decades.

I do not want to keep you from browsing through the articles that hopefully provide new insights and serve as good resource for your daily work.

Enjoy reading!

Franz Richter

HIGH QUALITY DIFFRACTIVE OPTICAL ELEMENTS (DOEs) USING SMILE IMPRINT TECHNIQUE

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Augmented reality (AR) enhancing the existing natural environment by overlaying a virtual world is an emerging and growing market and attracts huge commercial interest into optical devices which can be implemented into head-mounted AR equipment. Diffractive optical elements (DOEs) are considered as the most promising candidate to meet the market's requirements such as compactness, low-cost, and reliability [1] as they replace large display headsets for virtual reality (VR) by light-weight glasses. Their structures can vary from simple optical gratings to binary elements or pyramid-like multilevel structures. While gratings are used as diffractive wave guides for the in- and outcoupling of laser beams in AR glasses [2], binary or multilevel DOEs create three-dimensional projections for holograms [3] or grids for face-recognition. There are many techniques to fabricate DOEs based on, e.g. greyscale lithography, direct writing using laser or electron beams, and direct machining. However, these methods exhibit great weaknesses such as low process variability and surface precision, high equipment costs, and low volumes limiting their suitability for mass production [3]. In contrast, soft lithography replication offers a pathway to the fabrication of large area DOEs with high aspect ratios, multilevel features, and critical dimensions below the diffractive optical limit down to 50 nm. In combination with UV-curable materials, the fabrication time can be drastically reduced in comparison to, e.g. hot embossing replication methods, making it very appealing to industrial applications [3]. Here, we illustrate how the SMILE (SUSS MicroTec Imprint Lithography Equipment) technique can be used to obtain high quality binary DOEs meeting the market's requirements providing a very versatile tool to imprint both nano- and microstructures.

DOEs – BRIDGING THE GAP BETWEEN NANO- AND MICROSTRUCTURES

The rise of imprint lithography in recent years is based on its capability to resolve both nanometer and micrometer scale patterns and on its low cost and high throughput in comparison to conventional optical lithography. As a result, imprint lithography is the technique of choice to fabricate optical gratings, photonic crystals with critical dimensions and structure heights below 1 µm as well as micro lenses and monolithic lenses (see Figure 1). In this context, DOEs can be located in the nanoimprint regime as their typical structure height is around 1 µm and their lateral feature sizes range between hundreds of nm to a few micrometers.

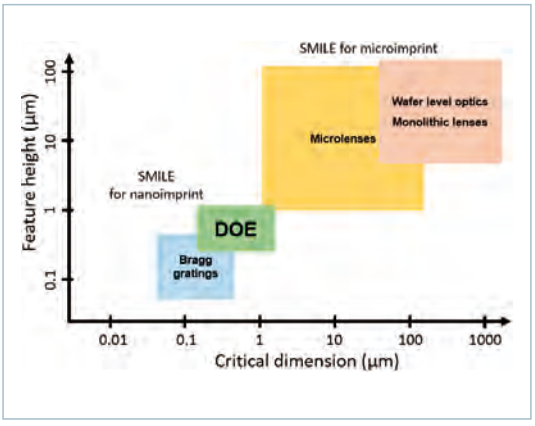

Figure 1 *Typical imprint applications classified according to their feature height and critical dimension. Both nano- and microstructures can be imprinted using the SMILE imprint technology*

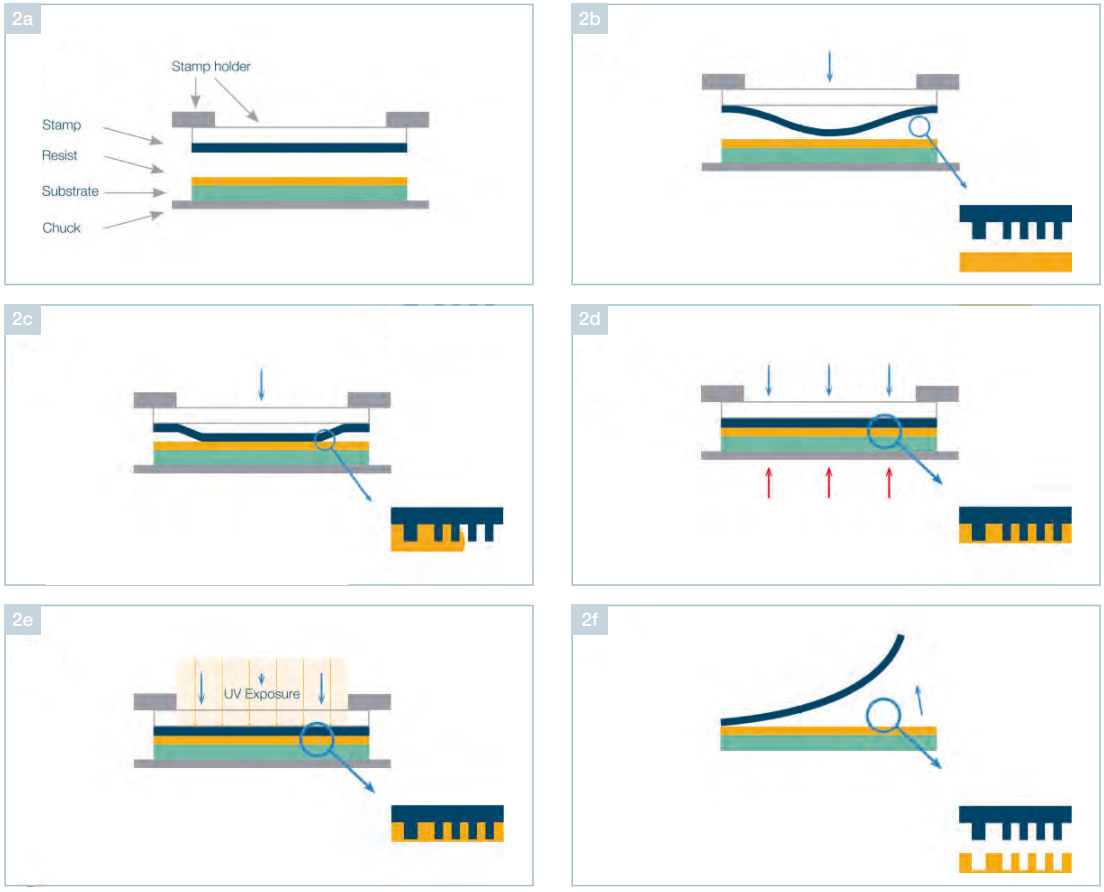

Figure 2 *Schematic illustrating the "SMILE for nanoimprint" process. After the alignment of the stamp to the imprint substrate (a), a small pressure is used to bend the flexible stamp (b) resulting in an imprint wave from the center to the edge of the wafer (c). After an optional force step (d), the imprint resist is cured (e) and the imprint substrate is separated from the stamp inside the machine (f)*

In order to imprint high quality DOEs, SUSS MicroTec has developed the SMILE for nano-imprint technology using flexible stamps (see Storace, SUSS Report 2015). As illustrated in Figure 2, a UV-curable stamp material on a flexible PET foil (Figure 2a) is bent using a small pressure between the stamp and stamp holder (Figure 2b) resulting in a radial imprint wave from the center to the edge of the imprint substrate (Figure 2c). As a result, any enclosure of air is avoided and a full-field imprint can be obtained. After an optional force step (Figure 2d), the imprint resist is cured by UV light (Figure 2e) – typical exposure times are between 30 and 60 seconds – and the imprint substrate is automatically separated from the stamp inside the machine (Figure 2f) enabling high wafer throughputs. As this SMILE imprint technique is based on the same tooling which is used to imprint microstructures (SMILE for microimprint), one SUSS mask aligner equipped with SMILE can imprint both nano- and microstructures covering a huge span of feature sizes.

DOEs – FROM A LASER BEAM TO A PROJECTED THREE-DIMENSIONAL IMAGE

The basic working principle of DOEs is illustrated in Figure 3. In refractive optical elements, an incident light beam undergoes a change in its direction when entering another medium with a different refractive index. Leaving a prism with an apex angle β and the refractive index n_1 (Figure 3a), the original path of a laser beam with the wave length λ is deflected by γ when reaching the second medium with the refractive index n_2. The degree of the refraction depends on the incident angle of the laser beam α_1 and the refractive indices:

$$n_1 \sin\alpha_1 = n_2 \sin\alpha_2 . \qquad \text{(Eq. 1)}$$

Similar to the design of Fresnel lenses as a further development of conventional lenses, the amount of the material needed for the fabrication of these structures can be reduced by using a blazed diffractive structure (Figure 3b). The deflection of the light beam is now determined by the structure height of the blaze and its period d. In order to facilitate the production of these elements, the design can be further simplified using a binary structure (Figure 3c). As a result, the incident beam is now diffracted at the optical grating leading to an interference pattern behind the DOE. The maxima of the interference pattern can be calculated using the following formula:

$$d\,(\sin\theta_i + \sin\theta_m) = m\gamma, \qquad \text{(Eq. 2)}$$

where θ_i is the angle of the incident light beam, θ_m is the angle under which the m-th maximum can be observed and m is an integer which can be attributed to the m-th order. Considering the maxima of the first order, which has the highest intensity among the diffracted light beams (e.g., ~40.5 % of the incident light intensity when using the simplest form of a binary element [4]), one grating constant results in one "pixel" of the projected image. By combining many different grating constants, an incident light beam can be converted into an array of pixels behind the optical element yielding a diffracted pattern (see Figure 3d). As an application, the projection can be used for face recognition cameras using near infrared light in mobile phones allowing an effective identification from different angles (see Figure 3e).

In order to ensure a high efficiency of DOEs, the imprinted structures have to fulfill many requirements. The most crucial feature is the profile fidelity. In general, DOEs are designed for

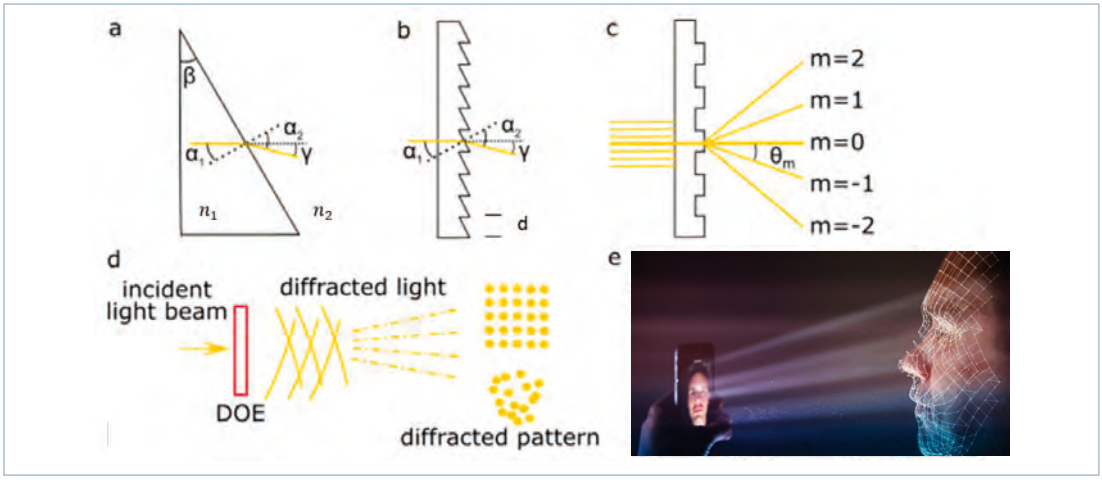

Figure 3 *Deflection of a light beam in a (a) refractive, (b) blazed diffractive, and (c) binary diffractive optical element. (d) Schematic showing the transformation of an incident light beam into a diffracted pattern. (e) Application of a DOE in face ID cameras*

one specific wave length in terms of a certain structure height. Even small deviations within the structure height of a single DOE result in a significant drop of the intensity in the diffracted pattern. Therefore, the uniformity of the structure height should be better than 1 % in order to obtain sharp diffracted patterns. Furthermore, vertical side wall angles especially in binary DOEs are important to obtain a high quality projection. Any transition region between the plateaus and the trenches would lead to misdirected light beams weakening the intensity of the projection behind the DOE. Therefore, a side wall angle larger than 85° is needed to obtain a high performance of the DOE.

Similar to the vertical accuracy, the lateral precision is crucial to get a high quality projection by a DOE. If the critical dimension (CD) in the xy-plane of the DOE imprint varies from the original design, the variation in the grating period *d* would result in alterations of the projected image weakening its intensity. Therefore, any changes, e.g. resulting from material shrinkage, process-based stamp expansions, etc., have to be considered in the master design.
According to Eq. 1, the degree of the refraction of light beams depends on the angle of the incident light beam and on the refractive indices. In some cases, to get the desired projection pattern, high refractive indices are needed which, however, imprint resists might not be able to provide. As a solution, the imprint pattern can be transferred into the underlying substrate with a higher refractive index. Using this approach, the imprint does not serve as the actual DOE but as a barrier for reactive gases (see Förthner et al, SUSS Report 2017). Thin residual layer (RL) thicknesses and a high control on its uniformity in combination with a good etching selectivity between the imprint resist and the imprint substrate are paramount to obtain a good pattern transfer into the substrate [5]. As a result, the etched imprint substrate with a high refractive index can serve as DOE.

MEETING THE MARKET'S REQUIREMENTS

The SMILE imprint technique ensures the fabrication of high quality DOEs with a high efficiency. As discussed above, a high profile fidelity in terms of a uniform structure height and vertical side walls are needed. Any deviation from this angle would lead to misdirected light beams weakening the intensity of the projection behind the DOE. Figure 4a shows a SEM side view image of a typical DOE structure imprinted using SMILE imprint technology. It reveals a complete filling of the DOE structure and a very low height variation. This is also confirmed by the atomic force microscopy (AFM) map in Figure 4b allowing a quantitative analysis of the imprint. In the depicted area of 10 x 10 µm², the total height variation is smaller than 10 nm yielding a structure height uniformity of better than 1 %. Furthermore, a side wall angle close to 90° can be observed

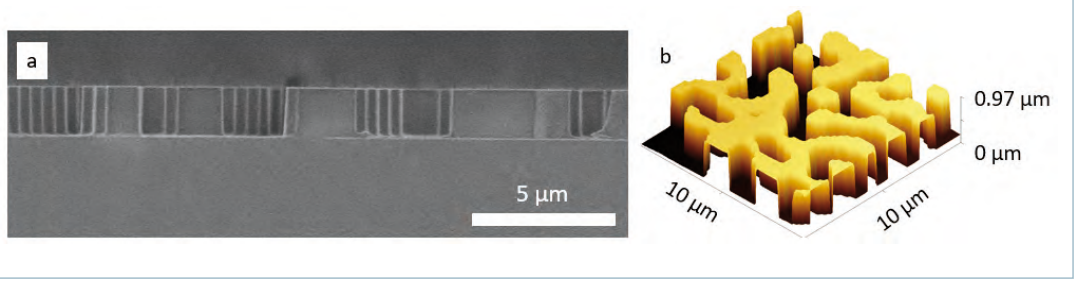

Figure 4 *(a) SEM image (side view) and AFM map (tilted view) of a DOE imprinted using the SMILE technology confirming a very good profile fidelity*

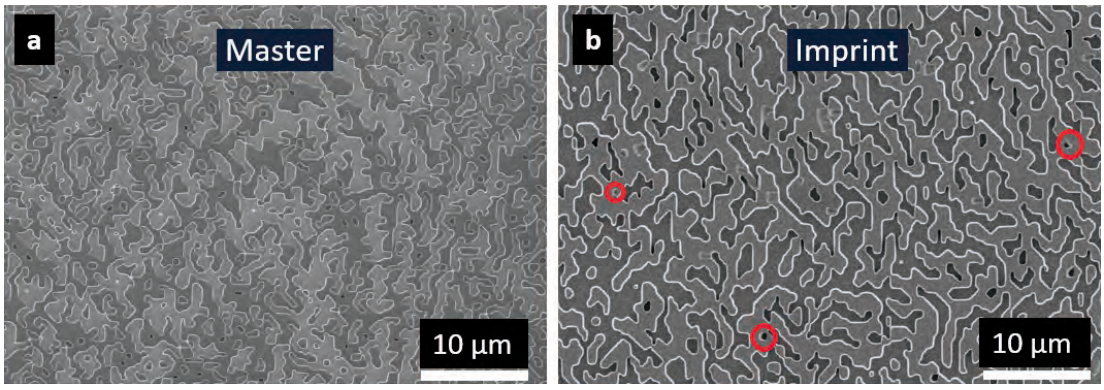

Figure 5 *SEM images comparing the DOE structure of the master wafer (a) to the imprint (b). The red circles in (b) indicate high aspect ratio features*

both in the AFM and the SEM image indicating a very high profile fidelity. The excellent lateral accuracy of the SMILE imprint technique is illustrated in Figure 5. Comparing the imprinted structures (Figure 5b) to the master wafer (Figure 5a) and taking the material shrinkage into account yield a full process-independent agreement in the lateral dimensions. Even high aspect ratio features (see red circles in Figure 5b) can be imprinted. As a result, high efficiency levels and, in turn, a high performance of the DOEs can be expected.

As discussed above, if a pattern transfer into a high refractive index material is necessary, a high control of the RL thickness and its uniformity are crucial to obtain good etching results. The SEM image of a DOE imprint using the SMILE imprint technology in Figure 4a exhibits a RL thickness well below 25 nm. Using additional pressure on the imprint before illumination helps obtain high uniformity level. As indicated in Figure 4, typically achieved uniformity levels are better than 5 %.
Another important requirement for the imprint of DOEs is the alignment accuracy. Especially if multiple fabrication steps are required, e.g. the imprint of DOE structures on top of a micro lens instead of a flat glass substrate, a high alignment precision is needed to ensure the proper diffraction of light beams. To this end, the excellent alignment capabilities of SUSS mask aligners can be used to precisely locate the stamp position with respect to the imprint substrate. The auto-alignment option with automated pattern recognition software (see Hennemeyer et al., SUSS Report 2015), furthermore, allow an operator-independent and fast alignment with a high wafer throughput.

CONCLUSION

In summary, diffractive optical elements (DOEs) are a powerful tool to manipulate the way of light creating high quality projections. They are the basic components for augmented reality devices enhancing the existing surrounding environment by adding virtual elements and, therefore, attract huge commercial interest. Using the SMILE imprint technology, defect-free DOE imprints with a high profile fidelity and lateral accuracy can be obtained. The possibility to employ additional pressure before the cross-linking of the UV-curable imprint resist, ensures a high residual layer control enabling to transfer the DOE pattern into the underlying imprint substrates. Furthermore, the most modern alignment processes of the SUSS mask aligners provide a very high alignment accuracy which is of high importance for multilevel DOE processing.

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[3] *M. T. Gale: "Replication techniques for diffractive optical elements", Microelectronic Engineering (1997), 34 (3-4), p.321-339*

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[5] *Martin Messerschmidt, Andrew Greer, Florian Schlachter, Julian Barnett, Manuel W. Thesen, Nikolaj Gadegaard, Gabi Grützner, and Arne Schleunitz: New Organic Photo-Curable Nanoimprint Resist «mr-NIL210» for High Volume Fabrication Applying Soft PDMS-Based Stamps, Journal of Photopolymer Science and Technology (2017), 30 (5), p. 605-611*

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TM200/TM300 METROLOGY MODULES ENABLE COMPREHENSIVE MANAGEMENT OF COATING PROCESSES

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Process engineers regularly achieve precise process performance with the ACS200 and ACS300 coating systems, but maintaining this process with the real-world situation of a HVM fab is another task completely. Atmospheric, material and mechanical variations contribute to the drifts in resist coating processes, and vary from location to location.

With ever tightening process windows maintaining high yield is already a challenge, especially if sample rates are low and/or there are several process steps after the coat. Precise inspection and CD measurements can be made after development or after etch, but deciding whether drifts or signatures are due to coat, exposure, development or etch equipment can be a challenge. In addition to this challenge, the current metrology portfolio can only alert you to an issue but not the source, let alone suggest how to resolve it.

The current standard tool qualification test of coating an unstructured wafer and measuring thickness is adequate for low frequency inter-wafer thickness drifts, but is blind to intra-wafer excursions. What is needed, is an enhanced method of tool qualification metrology that captures excursions caused by all sources of coating variation. With exposure and development variations removed from the equation, the process engineer has an ideal sample to analyse all variables in the coating process.

The new TM200 and TM300 metrology modules from SUSS MicroTec are the tools that finally reveal a clear picture of the coating process, and fully automate the tool qualification process.

INTRODUCTION

Our process and SUSS application engineers are expected to deliver excellent results on a daily basis, but maintaining this high performance over time is not so straight forward. Variation from equipment, materials and the cleanroom environment cause low frequency drifts and intermittent excursions. Monitoring and controlling such processes to maintain yield is an important task in any production environment, and becomes critical in the back end of line when the substrate value is high, metrology is less frequent and materials are difficult to rework.

Working closely with customers to extend high performance of our ACS coating systems beyond existing capabilities is a gap in metrology that was repeatedly encountered.

- Periodic thickness checks with bare wafers is good for compensating for inter wafer drifts over time, but is blind to intra wafer excursions.
- Post lithography CD and defect inspection tell you there is an issue, but cannot tell you where it is coming from, let alone how to resolve it.

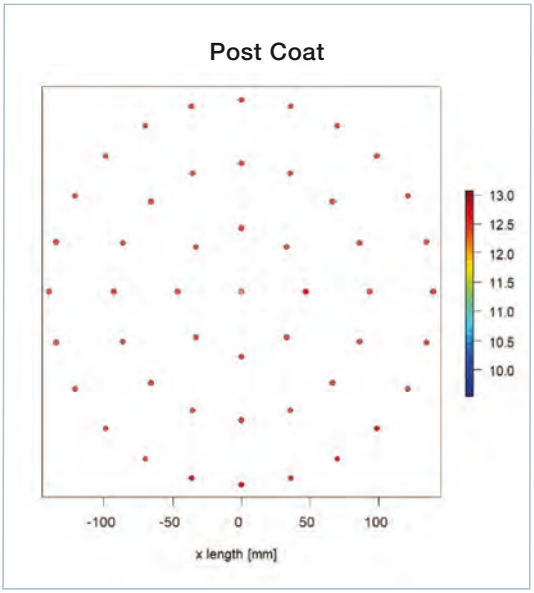

Figure 1 49-point thickness measurement using ellipsometer

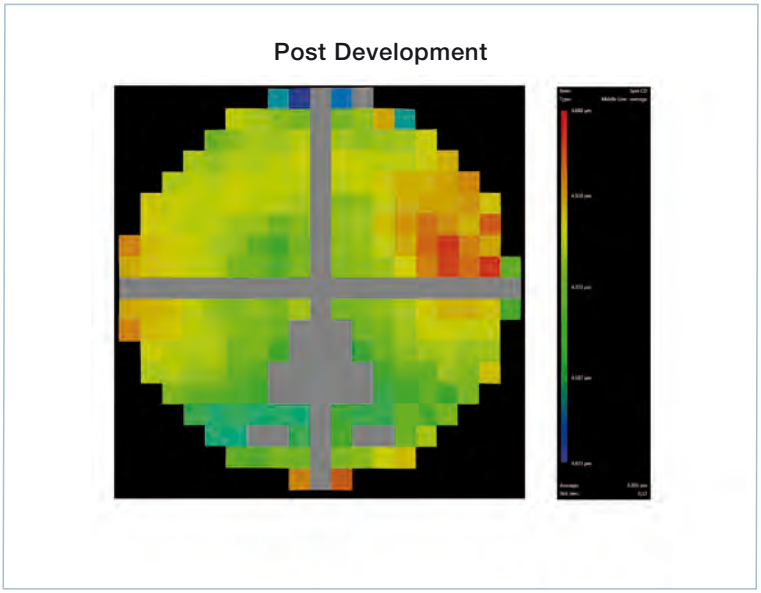

Figure 2 CD measurement

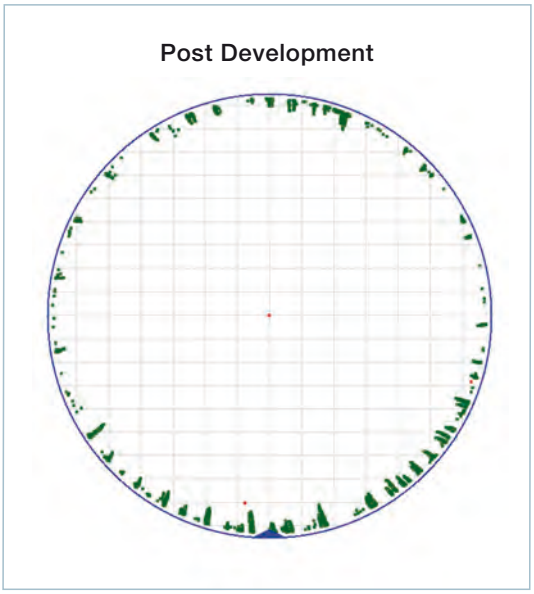

Figure 3 Defect inspection

What we need is to monitor coating process variation, not just react to defects detected later in the process flow. The best method to monitor the coating process would be immediately after a wafer is coated with a high density of measurement points; Ideally with the ability to correlate coating signatures to other sensors throughout the tool. Speeding up this measurement process with automation would enable higher frequency of such measurements to keep a tighter control of the tool.

THE TARGET

SUSS MicroTec set out to develop a comprehensive metrology platform that could quantify all variations that contribute to the coating process. The goal was to go beyond measuring thickness during periodic tool qualification tests and catch everything; once we could measure it, we could then manage it. The additional targets of integrating the module into the coater, automation of the measurement and feedback loop capability would deliver an industry 4.0 ready coating platform.

The key criteria for such a metrology module are:

- Non-destructive measurement method
- High density of measurement locations for thorough analysis of the wafer coat
- Precision to match existing metrology platforms
- Accuracy to give stable results in HVM environment
- Small package and low maintenance for integration inside the coater system
- High measurement speed maintain coating process throughput
- Feedback loop capability to automatically optimize coating parameters
- Fully integrated within tool controller software, sharing the same easy-to-use GUI and allowing offline analysis of collected data

THE RESULT

The principle of the TM200/300 is a high-speed interferometric thickness measurement of a full wafer surface with nanometer accuracy and stability. Using a novel positioning stage, the module is able to measure thousands of points, with a small footprint in less than a minute. This small package allows integration inside a coater, and the high throughput mitigates any throughput impact on processes running in parallel.

To ensure high MTBF (mean time between failure) and measurement stability, an LED-based illumination system was selected. This means maintenance-free operation, and exceptionally stable results are achieved.

A feedback loop was introduced to the ACS coater software to allow recipe modification based on the thickness measurement result. This feedback loop enables:

- Full automation of the current tool qualification procedure
- Flexibility to modify all coating parameters
- Compatibility with signature analysis algorithms

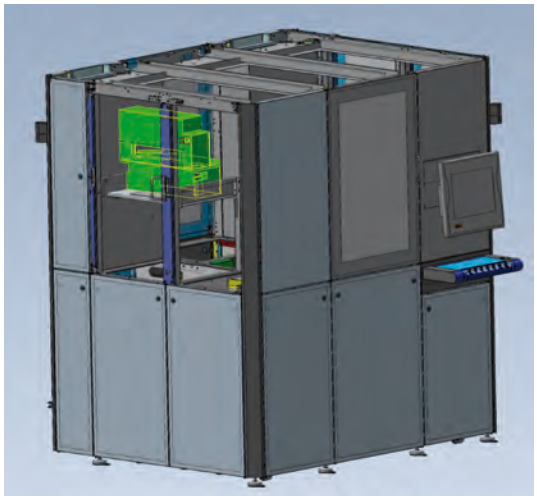

Figure 4 *TM200 module in an ACS200*

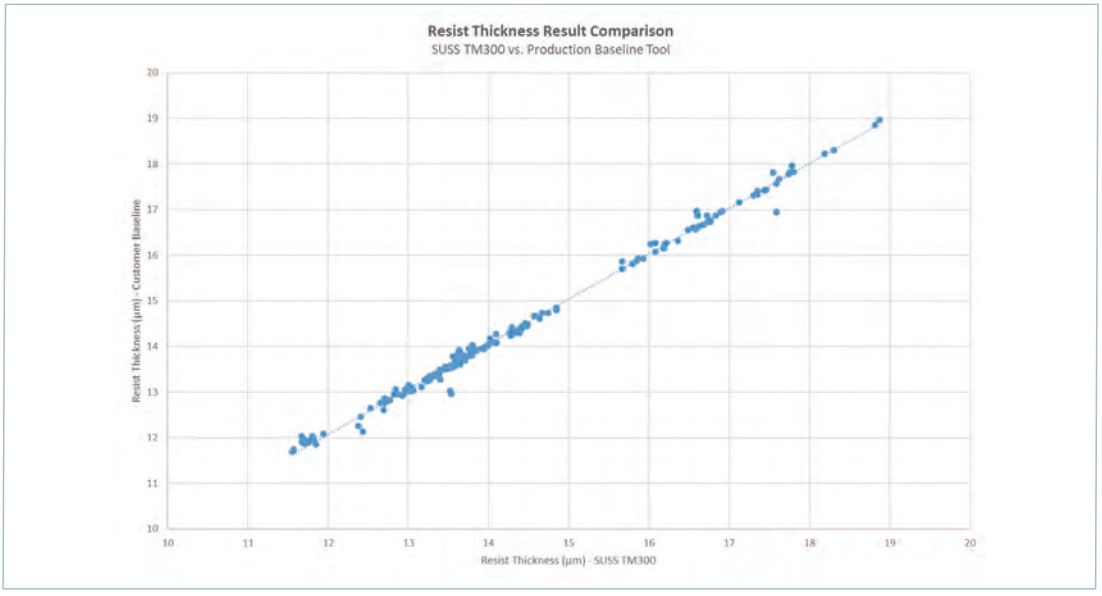

Figure 5 *Validation of TM300 accuracy and stability in production line*

BASELINE VALIDATION

Before exploring the new capabilities of the high density of measurement points, the accuracy and stability of this new metrology unit must be validated. In close collaboration with customers, SUSS MicroTec performed this validation, in a 300 mm HVM environment.

The customer tool qualification process was as follows:

1. Coating of a bare 300 mm Si wafer using the production coating recipe.
2. Manual transportation of the wafers from the ACS300 to their automated ellipsometer, and measurement of the resist thickness at 49 points.
   a. If thickness was out of spec the recipe was adjusted; increase spin speed if thickness is too high, reduce spin speed if it is too thin.
3. The coating and measurement process is repeated until the measured thickness is within SPC limits.
4. This procedure is repeated for each product, meaning multiple recipes with different target thickness.
5. A similar process is performed for polyimide material, but spin time is adjusted to reach the target thickness instead of spin speed.

Once installed, the TM300 measured the tool qualification wafers in parallel to the baseline ellipsometer over a period of 6 months. A comparison of the mean thickness result from the 7500 point measurement of the TM300 vs the 49-point baseline tool is plotted in the graph below. The results are 99.7 % correlation (multiple R) between the TM300 and baseline tool over a range of different thicknesses, and over the course of 6 months.

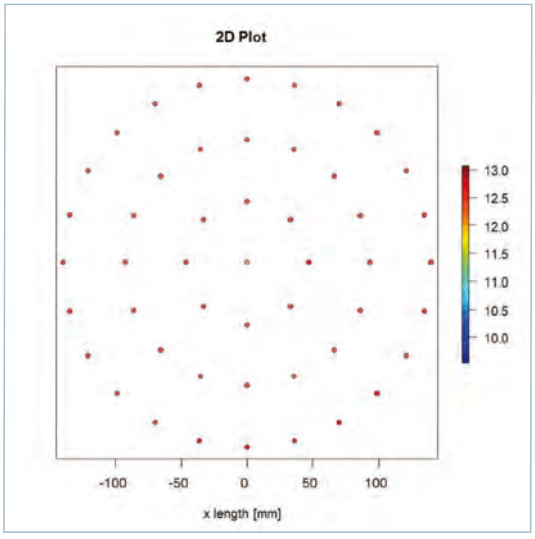

Figure 6 *49-point thickness measurement using ellipsometer*

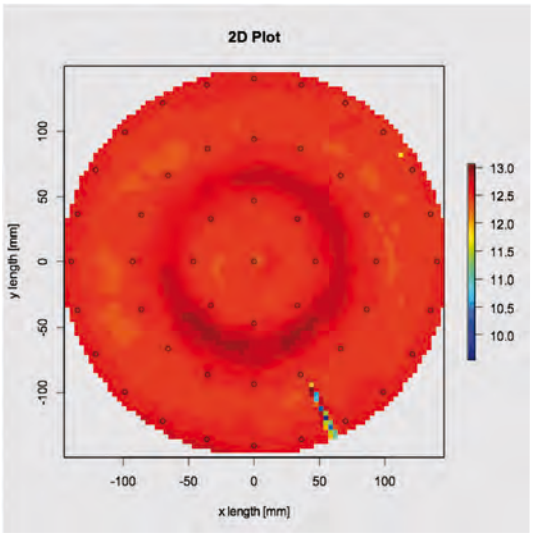

Figure 7 *DI300 comprehensive measurement (with overlay of 49-point locations)*

ENHANCED CAPABILITY OF THE TM300

Now that the TM300 mean thickness results are validated in terms of accuracy and stability we can investigate the benefits of the unique high-density measurement capabilities. The TM300 is capable of measuring thousands of points across the full wafer surface, including the wafer edge, in the same amount of time as the standard 49-point measurement of existing tools. Figure 6 and 7 shows a comparison result of the same wafer with the standard 49-point thickness measurement and a 7500-point measurement with the TM300, both with similar inspection times.

This wafer was in the first batch of tool qualification wafers measured after installation. Not only could we quantify the comet in the lower right corner that was missed by the baseline tool, but a long suspected ring of thicker resist was revealed. This signature was not quantifiable prior to the deployment of the TM300.

Over the course of the evaluation more intra-wafer thickness variation signatures were observed periodically, examples of which are shown in figures 9 - 14. The high quantity of measurement points generated by the TM300 delivers statistical power to identify these intra-wafer excursions. Providing the quantified measure of variation from each wafer in addition to mean thickness via SECS-GEM allows Statistical Process Control (SPC) at the host. Figure 8 shows the variation data collected during the evaluation period with the customer. An upper control limit of 1.25 % was created to identify intra-wafer excursions. Typically the baseline ellipsometer tool did not report these signatures so they were visually inspected to verify that they were true coating defects. Once verified, the data was reviewed by SUSS MicroTec application engineers to identify the root cause and appropriate corrective actions.

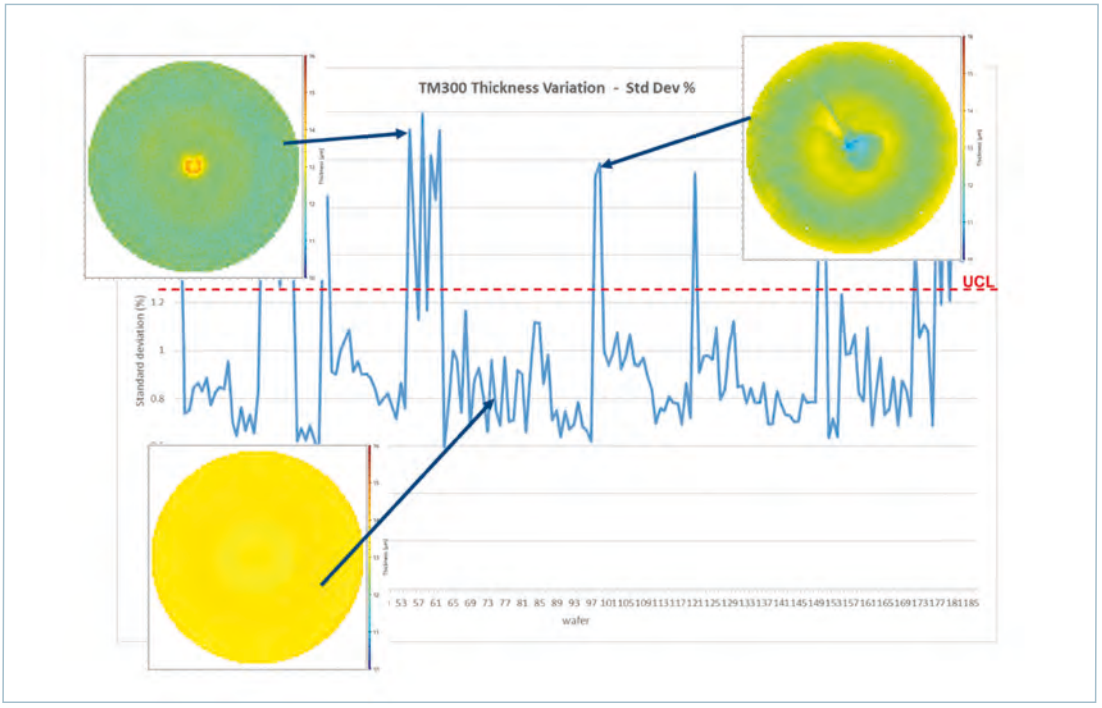

Figure 8 *Thickness variation data per wafer with new UCL to catch excursions*

IMMEDIATE IMPLEMENTATION

1. Manpower required for tool qualification tests is reduced significantly; from what used to take 30 – 40 minutes now takes less than 5. This manpower requirement drops to zero for fabs with automated transport since the ACS can alert the host of a successful result and automatically return to production.
2. Statistical variation data is sent to the host in addition to mean thickness. A control limit of 1.25 % is set for this new data, and an alert is created if this control limit is reached. Such an excursion is a reliable predictor of issues beyond low frequency thickness variations and must be addressed before returning the coating system to production.
3. A troubleshooting guide was created with the customer to enable technicians to quickly identify known excursion signatures and how to resolve the root cause.
   - High-resolution result images are available for process engineers to troubleshoot new excursions, and continually improve the troubleshooting guide.
   - The reduction of coating defects detected post development on production wafers and the resulting yield improvement is currently being calculated.

On the next page are some examples from the TM200/300 troubleshooting guide based on measurements at the HVM site.

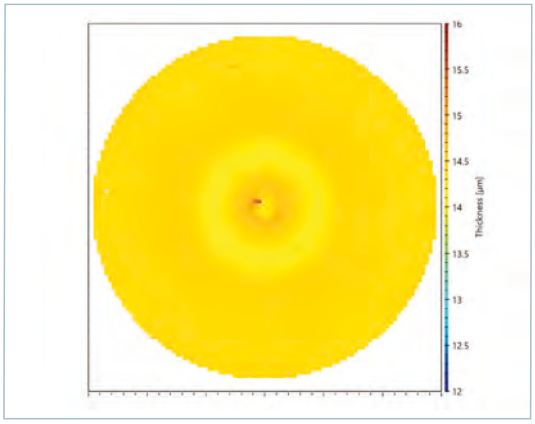

Figure 9 *Clogged nozzle during static dispense*

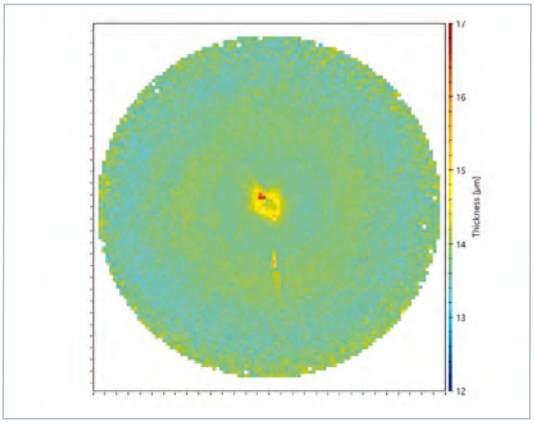

Figure 10 *Incorrect nozzle suck back*

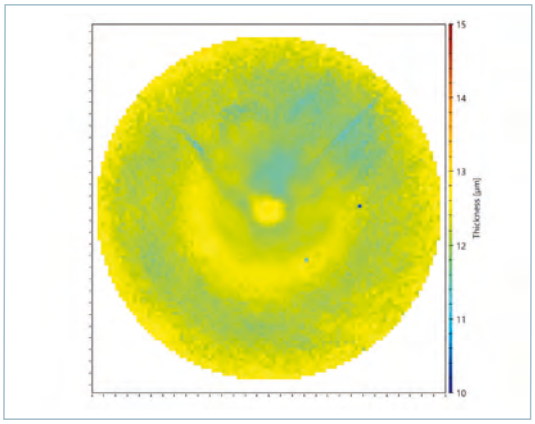

Figure 11 *Static dispense acceleration too high*

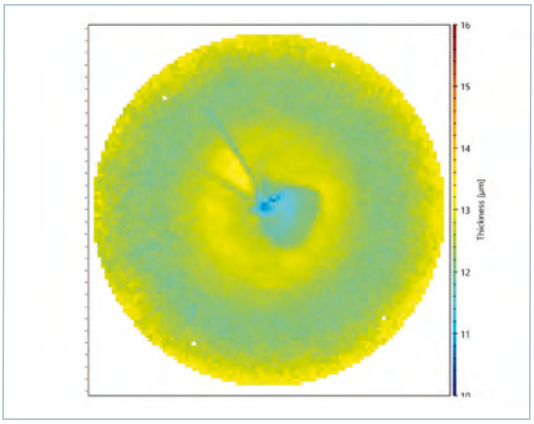

Figure 12 *Dynamic dispense rotation speed too high*

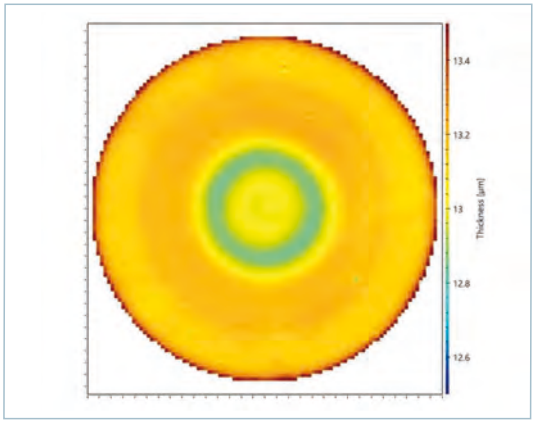

Figure 13 *Spin start too late after static dispense*

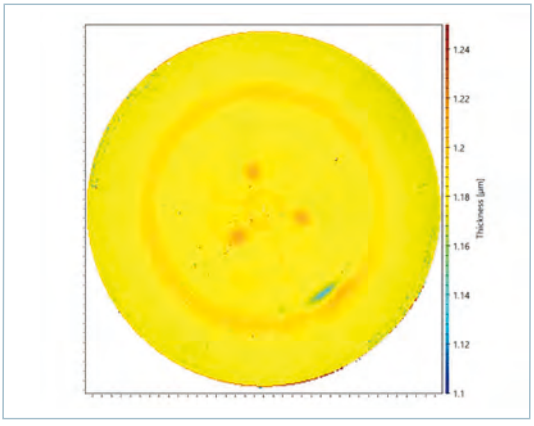

Figure 14 *Temperature variation at vacuum channels*

NEXT STEPS

Learning algorithms are being developed to correlate thickness signatures to coating parameters. Such tool intelligence can then alert the process engineer of specific issues and/or automate corrective measures within the ACS300 coater tool and resume production. A patent is pending for this functionality.

CONCLUSION

The new SUSS TM200/300 module is a game changer that finally enables precise process control of the lithographic coating processes. The key points of the module are:

- Excellent measurement accuracy allows the TM200/300 results to be compatible with existing thickness SPC baselines.
- The high density of the data enables real statistical analysis of each wafer, catch yield limiting excursions before the tool is returned to production.
- Automation and feedback loop capability reduces time required for tool qualification tests. The frequency of qualification tests can therefore be increased if needed for unstable production environments.
- Compact size and high throughput allows integration inside the ACS200/300 coating systems without impact on throughput of processes running in parallel.
- Automatic signature classification is already under development to deliver intelligent industry 4.0 capability.

This unique metrology module is an option for new ACS200 and ACS300 systems, and is available for field upgrades. Both new and upgraded systems have already been installed at HVM sites. The thickness measurement modules are available at SUSS MicroTec in Sternenfels and Garching for demonstration with a broad range of substrates and materials.

Acknowledgements
The author would like to acknowledge Dr. Florian Palitschka for his outstanding technical support at our customer site, and with the subsequent data analysis. A special thanks to Dr.-Ing. Thomas Grund, Margarete Zoberbier, Christof Kronseder and Dr. Marc Hennemeyer for their support.

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He received his B.S. in Electrical Engineering from Northeastern University in Boston.

AN OVERVIEW ABOUT THE EXCIMER LASER ABLATION OF DIFFERENT POLYMERS AND THEIR APPLICATION FOR WAFER AND PANEL LEVEL PACKAGING

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The demands for packaging for either wafer or panel respectively heterogeneous integration in general are rising. New materials and technologies are needed to address the challenges resulting from that demands like better dielectric properties or higher resolution just to name two examples. The excimer laser ablation is able to meet that needs and process the new materials, which are not always photosensitive anymore. The system used for this paper is a combination of a projection stepper platform combined with an excimer laser. The field of application for this system is quite wide. It can be used for laser debonding of supporting substrates or the seed layer removal after galvanic. The main application, however, is the ablation of all types of polymers to generate VIAs for example. In contrast to already known PCB lasers, it is also possible to ablate complex structures in parallel, as it is a mask-based technology. Due to that, it is possible to generate trenches and VIAs within one step. This enables a technology already known from the front end of line (FEOL) to be transferred to the back end of line (BEOL): the dual damascene process.

Within this paper, all the mentioned applications and the experience with a broad variety of polymer materials such as Polyimide, PBO, BCB, ABF, Dry Films are going to be presented. It is going to be shown that the excimer laser system can overcome the limitations of common polymers in terms of resolution and that the laser dual damascene approach can meet the needs for the overall demand towards 2 µm lines and space for packaging. Additionally some reliability data is presented that prove that the laser ablation can replace the today common lithography processes without any drawbacks.

Key words: *Excimer laser; ablation; dual damascene; FOWLP, wafer level packaging.*

INTRODUCTION

Today the demands on wafer as well as panel level packaging are rising due to the overall trend of rising I/O counts and the need of thinner packages for example. One of these demands resulting of the high I/O count is the need of an increasing routing density to avoid a higher number of redistribution layers per package. Besides, the cost aspects of each layer also the technological aspects are rising. The more layers the more stress is generated inside the package, which lowers the reliability. Another aspect is the rising topography added by each layer, which influences the following layers or makes it necessary to integrate cost sensitive planarization steps. Increasing the routing density means to increase the achievable resolution for resist as well as polymer processing. To achieve this, two parts of the process have to be enhanced: the exposure system and the capabilities of the resist resp. polymer system. Both are challenging and sometimes not possible due to chemical limitations of the polymer system for example. Today common polymers allow the photographic realization of 20 to 40 µm VIAs. For some applications, non-photo material like ABF becomes attractive and needs to fulfill the same requirements like mentioned before. However, the common technologies used to structure non-photo polymers like dry etching cannot fulfill these requirements as the under-etching does not allow a high resolution and is in case of filled material like ABF not possible.

The newest exposure systems and resists can already address the demand towards two-µm resolution for the redistribution layers (RDL). However, the semi-additive process, which is commonly used to generate the Cu RDL, faces some new challenges. The adhesion of the Cu

lines is lowered due to the small footprint. The under-etching of the seed layer etching gets a more challenging process too. Both rising the risk of lifting the Cu lines. Bringing the lines close to two µm generates a strong electrical field, which enhances the electrochemical migration between the Cu lines. This sets new demands on the chemistry of the polymer to avoid an electrical short over time due to the electrochemical migration.
In the past years the processing and handling of thinned wafers and modules gets a key technology in 2.5D- and 3D-packaging. The supporting technology needs to withstand harsh influences during the processing like high temperatures while enabling a de-bond process with nearly no impact on the supported wafer resp. module at the same time.
The excimer laser ablation in combination with a projection system and a stepper-based platform can address all these challenges or enable new process flows, which allows solving the mentioned problems.

BACKGROUND

ABLATION PROCESS

The laser ablation or pulsed laser ablation is a process in which material is removed by a short laser pulse with high intensity (which is measured as the fluence). This takes place far from equilibrium, which allows suppressing the excitation energy outside of the ablated volume. According to Bäuerle [1], the process is based on two different main mechanisms – the photothermal and photochemical ablation – and a mixed mode of both. The energy of the photons (the wavelength of the laser) and the fluence are mainly responsible for the mechanism. If the fluence of the laser is below a certain threshold, the energy of the laser is absorbed and transferred into heat. The material starts to melt and gets eventually evaporated. If the fluence of the laser is high enough, the chemical bonds break and gaseous products are formed under an enormous change of volume. This leads to an explosive-like ablation process. The threshold where this happens is defined by the bond energies of the material, which is ablated. For polymers with bonding energies between 3.6 eV and 4.3 eV of C-C and C-H, high-energy ultraviolet photons are able to break most of the interatomic bonds. As a polymer consist of many different interatomic bonds, the mode of ablation is a kind of a mixed mode with the dominance of the photochemical ablation. The threshold of most inorganic materials like metals is different to the threshold of polymers. This allows the structuring of polymers on top of these materials without destroying the material underneath.

The photon energy of excimer lasers of above four eV is sufficient to cause the photochemical ablation process of polymers. Unlike most laser sources, the excimer laser produces a large area beam, which can be widened and formed in optical systems. This allows the usage of excimer laser systems in projection exposure systems for ablation. The light can be directed through a structured mask and projected on a work plane. The glass material has to be transparent to the wavelength. The light blocking material is Al as it has a very high threshold level for ablation. The threshold of the commonly for exposure used Cr is too low. In this work, a laser ablation system from SUSS MicroTec (ELP300) has been used. It combines an excimer laser source with a projection system and a high precision stepper platform. The used laser is a Coherent “LXPpro 305” with an output power of 40 W.

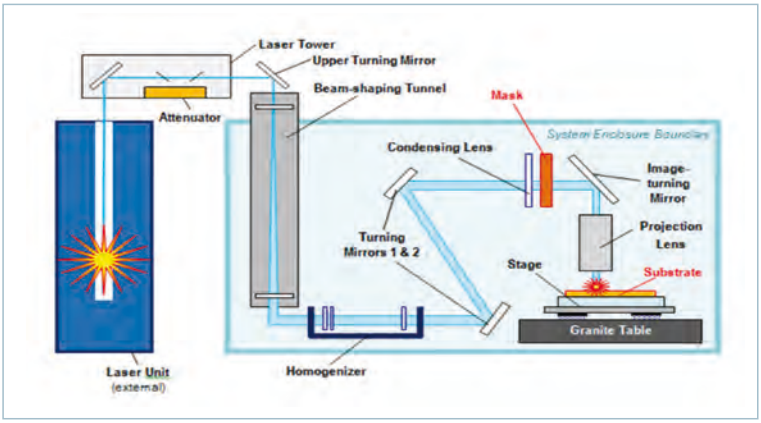

Figure 1 *System schematic of ELP300 [2]*

It is a KrF laser with 248 nm wavelength and 50 Hz repetition rate. The system has a maximum beam spot size of 6.5x6.5 mm² and the fluence can be varied between 70 and 650 mJ/cm². A setup of the system is shown in Figure 1.

The laser light is directed through a mask and projected and focused on the wafer surface. As a result, the pattern in the mask is ablated in the polymer present on the wafer. In principle, the system works like a projection stepper with the big difference that the patterns of the mask are not exposed in the resist or polymer, they are ablated.

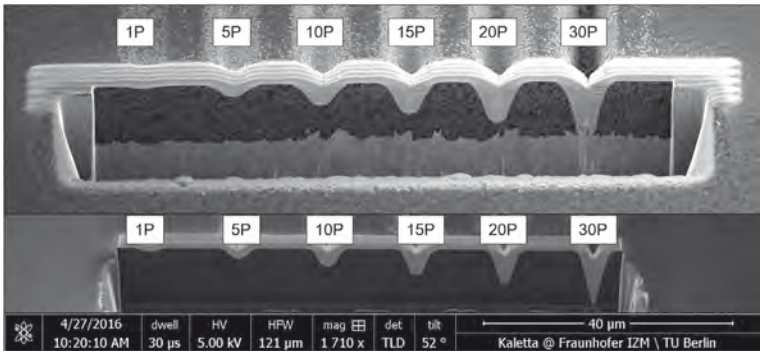

Figure 2 *FIB cross section of ablated ABF (top) and PI (bottom)*

EXPERIMENTAL RESULTS

Different polymers in different applications and projects have been ablated over the last years. The summarized results and key findings are presented in this section.

As already mentioned in the previous paragraph, every polymer can react to the ablation process a bit different. The ablation results depend on fluence, number of pulses, the patterns to be ablated and the ablation characteristic of the material. Besides the ablation rate (ablated material measured in um per pulse), the formation of the pattern resp. the cross section of pattern can differ too. A number of test ablations are performed with different parameters (usually number of pulses, fluence) and the results (depth of ablation, side wall angle etc.) are analyzed like shown in Figure 2.

In general, it can be stated the higher the fluence the higher is the ablation rate like shown in Figure 3.

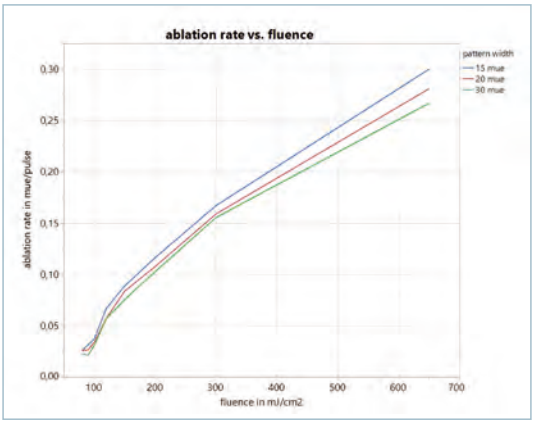

Figure 3 *Ablation rate of BCB*

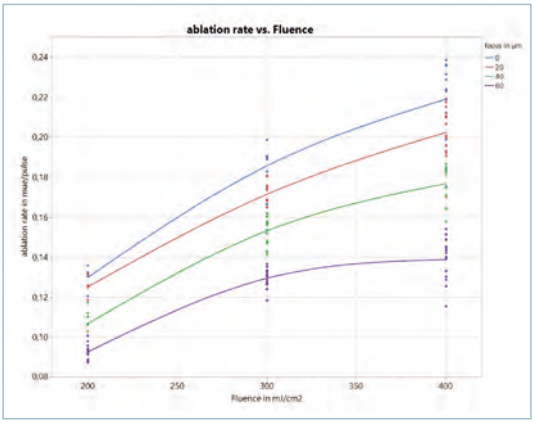

Figure 4 *Focus and fluence variation of ablated PI (CD 5 µm)*

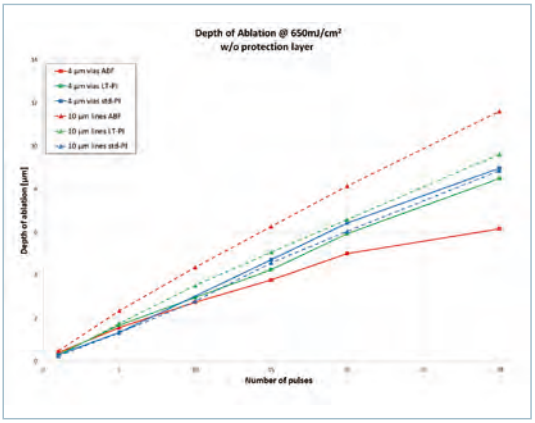

Figure 5 *Ablation depths of different polymers and patterns over number of laser pulses*

At some point, the ablation rate reaches saturation and is not rising anymore [3]. This effect can be observed, if the focus of the laser is intentionally de-focused like shown in Figure 4. The ablation rate is going into saturation for a focus of +60 µm.

In Figure 3 can already be seen that the ablation rate is sensitive for the width of the ablated structure. Besides the opening width, there is also dependency of the form of the ablated structure. The ablation rate of VIAs is in some cases different to the ablation rate of trenches for example. In Figure 5, you can see the ablation depth over the number of pulses of different polymers and patterns. Four µm VIAs and 10 µm trenches have been ablated. The analyzed PI – one low temperature and one conventional PI – show only a slightly difference between VIA and trench ablation. The ABF material shows a significant difference between the ablated patterns. The trenches are ablated much faster than the VIAs. One reason could be the filler particles in the ABF, which may inhibit the material transport out of the ablated structure.

The calculation of the ablation rate shows this more significant (Figure 6). The difference between the ablation rate of 10 µm line and 4 µm VIA ablation of ABF is nearly constant at 150 nm/pulse. The difference for the low temperature PI is only about 40 nm/pulse and the difference for the standard (high cure) PI is neglectable as it is in the range of measurement accuracy.

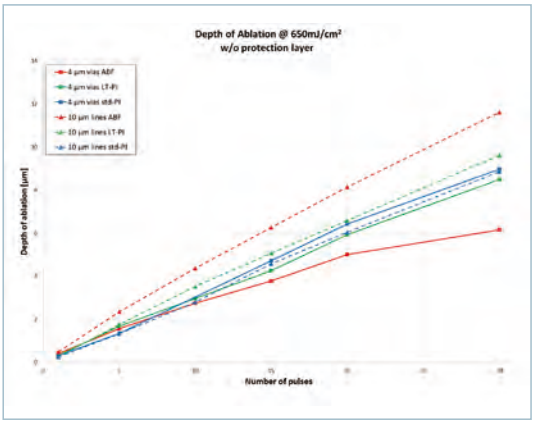

Figure 6 *Ablation rate of different polymers and patterns over number of laser pulses*

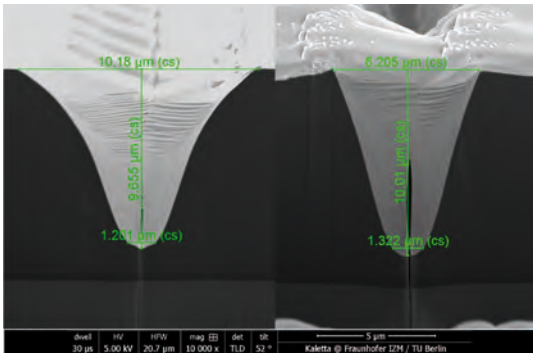

Figure 7 *Ablated trench in PI without (left) and with protection layer (right); 4 µm mask size (trenches filled with Pt during FIB preparation)*

Besides the ablation depth, the sidewall angle of the ablated structures as well as the flaring at the top of the structures are important information to setup a proper ablation process. Both values depend much on the material and the used fluence. A prediction model was presented by Paterson [3]. While the sidewall angle can be controlled with the fluence and wavelength (if possible), the flaring at the top of the structures can be reduced by using a protection layer on top of the ablated material. The protection layer should ideally be a thin film on top of the polymer, which should be easy to ablate with a low number of additional needed pulses and easy to strip after ablation. The flaring on top of the opening is pushed into this protection layer, which results in straighter sidewalls at the top like shown in Figure 7. The ablation parameter in both sample are the same. The resulting depth is nearly the same with about 10 µm but the flaring on top is highly reduced (6.2 µm instead of 10.2 µm).

The protection layer has additionally another benefit. During ablation, residues are generated (material dependent) called debris. Most of them are removed by a high efficient vacuum cell, but some debris is deposit around the ablated structures. There are several possibilities to remove it. With the help of the protection layer, the debris is removed together when the protection layer gets stripped.

APPLICATIONS

VIA GENERATION

One of the benefits of the used laser system is the massive generation of VIAs in parallel due to the use of the mask technology in contrast to sequentially working laser ablation systems known from the printed circuit board technology. The ablation process is setup to the polymer thickness and the under-laying metallization. As already described in the previous section, the ablation process stops on the metal layer if the fluence is adjusted correctly. A cleaning step is performed afterwards to remove the generated debris. In previous works the characteristics of ablated VIAs in different polymers has been studied [4],[5]. Kelvin structures with VIA openings from four µm to 30 µm were realized to measure the contact resistance of a single VIA. The achieved resistances are comparable to lithographic generated VIAs (Figure 8). The resistance rises with smaller VIA diameters. The film thickness was kept constant, which means that the aspect ratio of the VIA is rising with smaller diameters. This could cause that the metallization gets thinner at the bottom of the smaller VIAs and could be one root cause for the rising resistance.

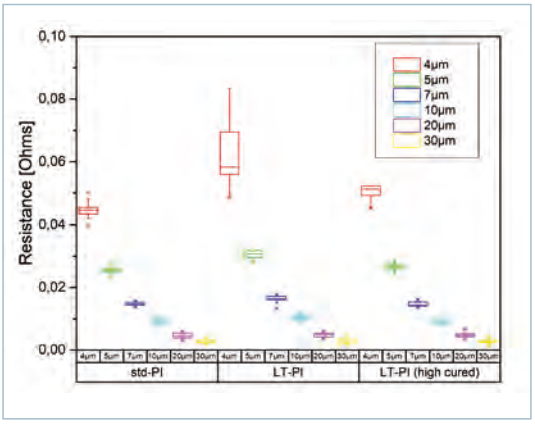

Figure 8 *VIA resistance of different polymers and openings sizes (polymer thickness: 7 µm)*

Nevertheless, the formation of high aspect ratio VIAs allows increasing the routing density without reducing the polymer thickness. Common lithographic generated VIAs below 10 µm are usually limited to a maximum aspect ratio of one [6]. For the ablation technology, high aspect ratio VIAs with VIA depth three times bigger than the opening size could be demonstrated in dry film BCB [5].

The other benefit of the used laser ablation system is the stepper platform. It allows a submicron alignment accuracy, which can be performed global or site-vise. This is a necessary feature for fan-out wafer or panel level packaging to increase the yield resp. to enhance the routing density. One of the bigger issues in fan-out packaging is the shift of the dies during molding. This makes it necessary that the lading pads for the VIAs are 1.5 to three times bigger than the VIA opening to hit the pads of the shifted dies in commonly used mask aligner technology. The ablation tool can perform the alignment site-vise, which is time-consuming. It can also ablate at the real position given in advance by an automated optical inspection (AOI) performed after molding and the use of a global alignment. Both allows to reduce the needed landing pad size to just a few um bigger than the VIA size.

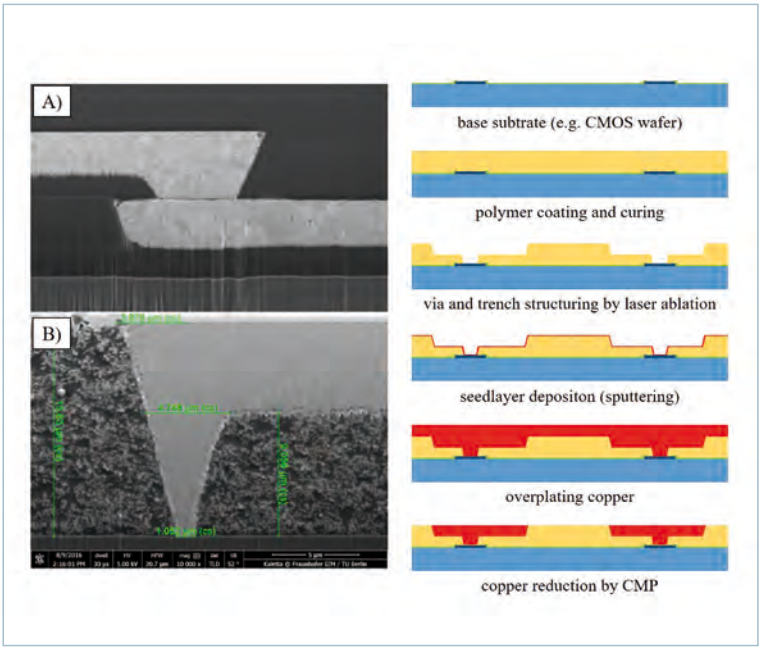

Figure 9 *Left side: cross sections of dual damascene RDL (A: LT-PI / B: ABF); right side: process flow*

DUAL DAMASCENE

As the ablation depth can be controlled by the number of pulses, it is possible to stop inside of the polymer layer. The high alignment accuracy allows ablating trenches and VIAs within the same process step, which enables to bring a front end of line process into the back end of line: the dual damascene process. The trenches are going to be ablated first, followed by the VIA ablation inside of the trenches. The VIA can have the same size as the trench. The created structures are filled with Cu and the overburden on top of the polymer is removed by chemical mechanical planarization (CMP). Some sample pictures of cross sections in low temperature polyimide and ABF and the schematic process flow can be seen in Figure 9. Different test samples were generated to analyze the process capabilities. A daisy chain structure was built-up to analyze the contact between two dual damascene layers with 960 VIAs within one die. These samples had an overall good yield [7]. The second realized test sample was an interdigital finger structure (capacitor IDC).

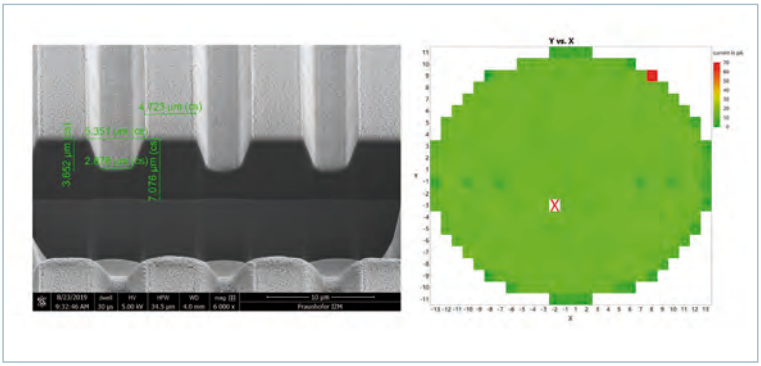

Figure 10 *Left: cross section of the ablated trenches; right: wafer map of leakage current of 5 µm L/S IDC in PI*

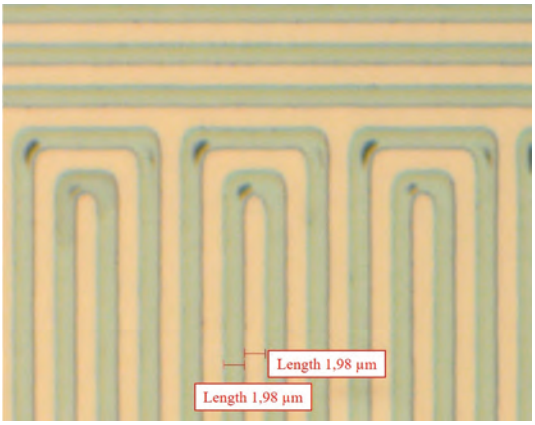

Figure 11 *Two µm L/S Cu lines in LT-PI*

The purpose of the IDC is to check the electro-migration behavior between dense Cu lines and it allows judging the wafer yield by measuring the leakage current between the IDC fingers. A cross section of the ablated trenches and a wafer map of IDC with five µm resolution is shown in Figure 10. Only one die had an electrical short and at one die at the wafer edge the leakage current was marginal higher (70 pA instead of ~10 to 25 pA).
The samples were subjected to a temperature humidity bias test (THB: 85 % relative humidity; 85 °C; 5 V bias) and showed no electro-chemical migration during the test period [8].

A reduction of the resolution down to two µm lines and space can be shown with the laser dual damascene technology (Figure 11). Two-µm Samples, which were generated with mask aligners in semi-additive technology (SAP) to compare both technologies, showed a significant worse yield. The reduction of the Cu line density down to two-µm resolution sets new demands regarding the electro-chemical migration. The damascene approach has the benefit that the seed layer is not only under the Cu lines (like in SAP technology). The seed layer clades the Cu lines and can be used as a diffusion barrier. Investigation regarding that are currently on-going.

SEED LAYER REMOVAL

Another application for the excimer laser can be the seed layer removal on top of polymers. When a laser pulse hits the substrate an energy shock impulse is introduced in the polymer under the seed layer, which results in a lifting of the thin metal film and some amount of polymer. This can be done mask-less with only one laser pulse. The embedded Cu lines are not affected. EDX analysis of the surrounding polymer (Figure 12) showed no presence of metal ions and electrical measurements confirmed the results.
During the sputtering process, metal ions get into the upper nm of the polymer layer resulting

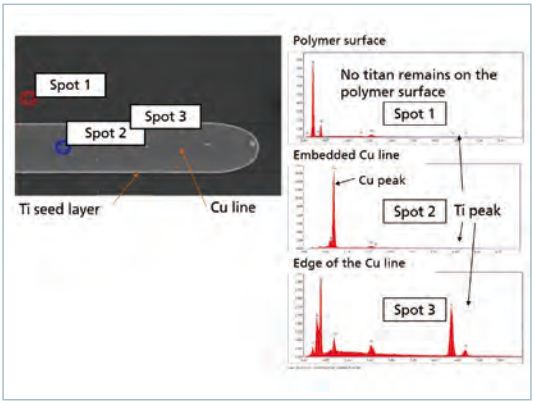

Figure 12 *EDX analysis of laser seed layer removal*

in a higher conductivity at the surface. A plasma de-scum step after wet etching of the seed layer is usually necessary to remove these upper layer. The EDX analysis and the electrical measurement after laser seed layer removal shows that no additional plasma de-scum is needed as the upper nm of the polymer are also removed by the laser pulse.

LASER ASSISTED DE-BONDING

Besides the structuring of dielectric layers, the direct bond breaking effect of the laser ablation can be used for another application: the laser assisted de-bonding. The 2.5D- and 3D-integration demands for thinner and stacked packages. Therefore, a supporting (temporary bonding) technology is needed which is able to handle thinned wafers and withstand the different processing technologies used for wafer processing. Thermoplastic polymers have been used for a long time but they suffer from high temperature processes like the curing of RDL polymers for example. They melt at higher temperatures, which limits their usage. The de-bonding of such supported wafers introduces additional thermal and mechanical stress at the end of the process chain and increases the risk of damaging the devices. The excimer laser enables the usage of other polymers with higher glass transition temperatures. The device wafers are bonded to a glass support carrier. This glass carrier has to have a high transmission at the wavelength of the excimer laser to enable a proper laser assisted de-bonding. The tests have shown that at least 15 % transmission is needed at the wavelength of the used laser system (248 nm) for this work [9]. The de-bonding is performed by exposing the used bond polymer through the backside (glass side) of the wafer stack. The adhesion bonds are broken and after the whole wafer is exposed, the glass carrier can be lifted easily with nearly no need of force. Afterwards, the device wafer needs to be cleaned as most of the polymer remains on it. During the whole laser de-bonding process the wafer is less exposed to thermal and mechanical stress as compared to conventional thermal mechanical de-bonding technologies while the usage of other polymers enables the usage of more aggressive process technologies. The support carrier can even be left on the device during dicing. This allows the flip chip bonding of very thin devices without risking a break and the glass carrier can be de-bonded afterwards [9].

CONCLUSION

The versatile application of excimer laser ablation from VIA generation to fine pitch dual damascene as well as seed layer removal and the usage in support bonding technologies could be shown within this paper. The technology is independent from substrate sizes as the projection principle can be scaled to nearly every substrate size in contrast to mask aligner technology for example. This makes the technology attractive for the use in fan out panel level packaging, where large mask sizes and the lack of flexibility of the mask aligner technology are getting a problem. The dual damascene approach together with the laser seed layer removal enables additionally to skip many wet chemistry process steps like development and wet etching. The usage of other material as the seed layer to use it as a barrier layer in the dual damascene process could be a promising approach to reduce electro-chemical migration between dense Cu lines and is going to be further investigated.

Acknowledgements

The project on which this publication is based was partly funded by the Federal Ministry of Education and Research under the funding codes 16FMD01K, 16FMD02 and 16FMD03.

The author would like to thank the colleagues of Fraunhofer IZM and TU Berlin, which were not mentioned as co-authors. Furthermore the author would like to thank the teams from SUSS MicroTec, Ajinomoto, Fujifilm Electronic Material and Dow for their support.

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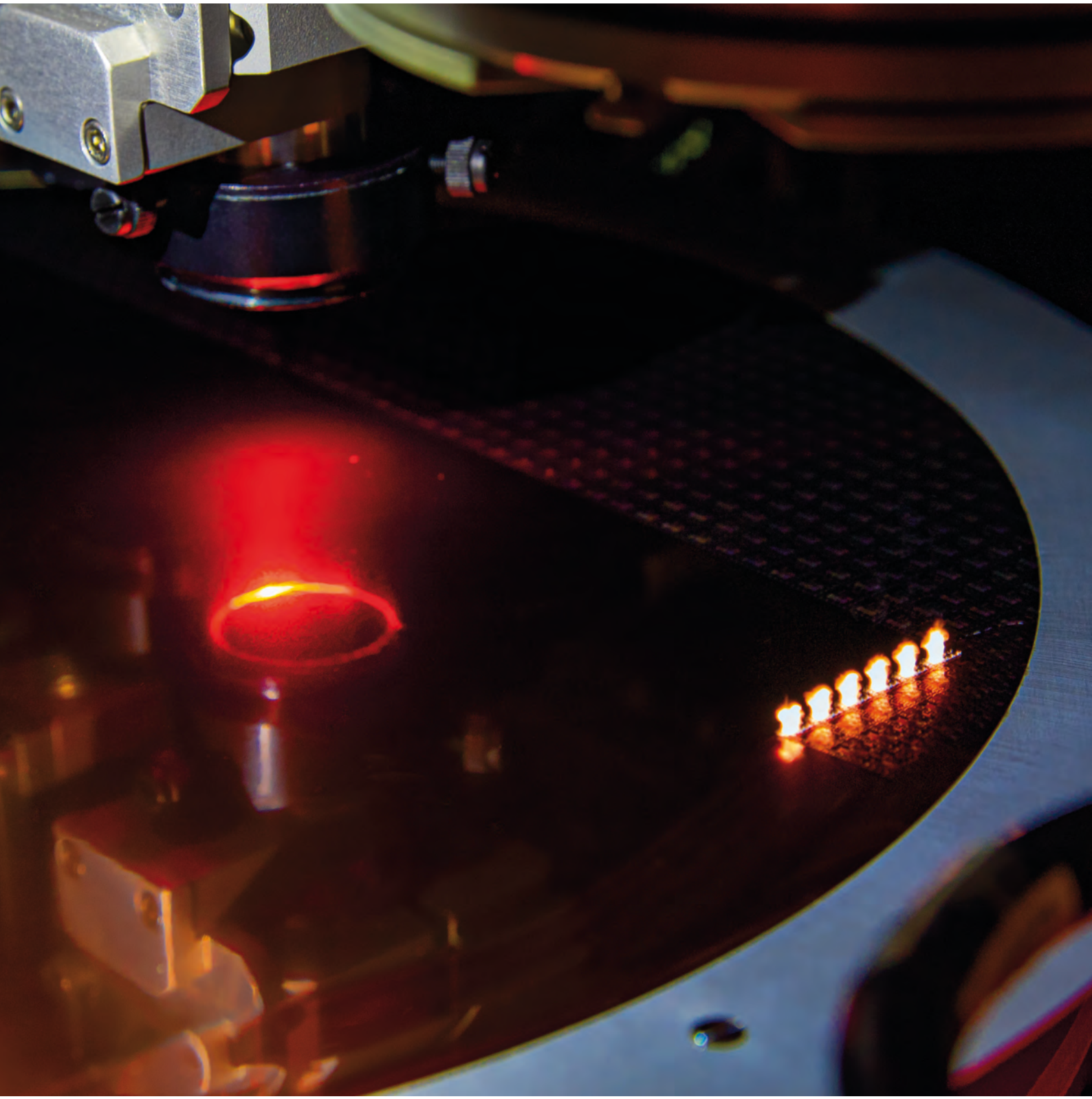
This article was originally published in the proceedings of the IWLPC in October 2019



FUSION BONDING AND INTEGRATED METROLOGY – TECHNOLOGY EXPANSION OF SUSS MICROTEC'S PRODUCT RANGE

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With the introduction of the XBS200 bond cluster platform in 2017, SUSS MicroTec has celebrated its reentry into the automated permanent bonding market. The new cluster for up to 200 mm wafers was developed to target metal bonding applications (mainly eutectic bonding and metal diffusion bonding) within the MEMS market, while also being capable of serving anodic bonding, glass frit bonding or temporary bonding requirements.

Looking back on a long tradition in permanent wafer bonding, SUSS MicroTec not only intended to resume its line of automated bonding platforms from the past, but to break new ground in automated permanent wafer bonding.

Therefore, SUSS MicroTec introduced distinct novel features, which provide a worldwide unique selling proposition, mainly fixture-less wafer handling and laser pre-bond.

The technological trends and numerous market requests however also made clear that low temperature fusion bonding as a mayor bonding technique still plays an important role in the market with the demand even increasing with respect to 2.5D and 3D packaging and the rise of RF MEMS.

SUSS MicroTec has therefore invested a great deal of effort to meet this demand by extending the XBS200 process capability to high-precision fusion bonding.

1. INTRODUCTION

Fusion or direct bonding is a long established bonding technique in the semiconductor and MEMS industry [1]. Joining two silicon wafers without any additional intermediate layer can achieve a weak bond if the surfaces are sufficiently flat and clean. In order to establish a permanent bond a subsequent annealing step is generally carried out to strengthen the bond. Traditionally fusion bonding made use of rather high temperatures (in the case of hydrophilic silicon at >1000 °C).

Especially with the rise of SOI (silicon on insulator) in the late 90s, fusion bonding has gained interest for the semiconductor industry besides MEMS and still remains to be one of the major manufacturing techniques for SOI wafers.

However, with respect to other semiconductor applications high temperatures can cause doping broadening by diffusion, metal degradation, thermal stress, defect introduction and even contamination. Post-metallization bonding or the presence of CMOS circuitry in particular therefore require significantly reduced annealing temperature profiles that can be achieved by wafer surface activation (either by exposing the wafer to specific wet-chemical solutions (e.g. RCA) [2] or by treating the wafers with a dedicated plasma process) [3].

Figure 1 *XBS200 permanent wafer bonding platform*

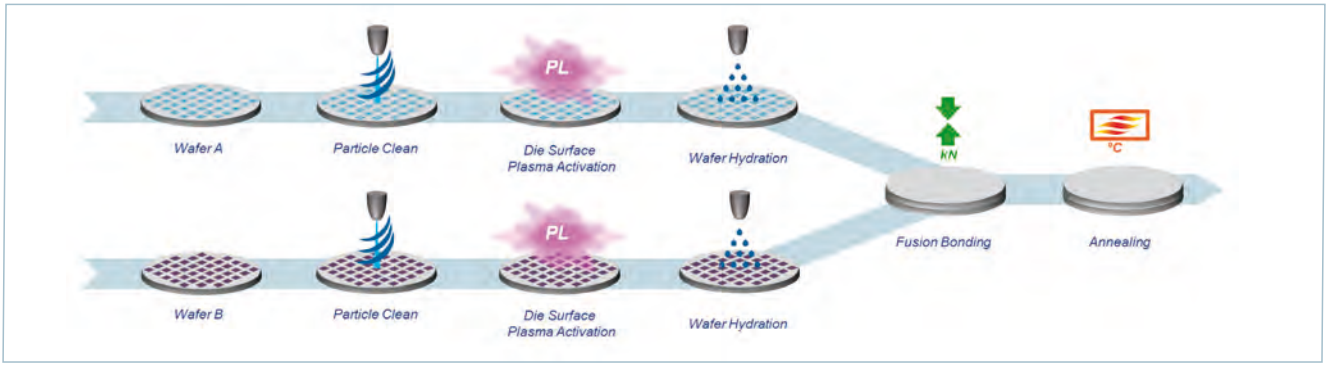

Figure 2 *Typical process flow for low temperature wafer fusion bonding (with plasma activation)*

Wafer surface activation has since allowed for a dramatic drop of the annealing temperatures at fusion bonding down to <450 °C, typically the max. thermal budget for CMOS wafers, while still achieving high bond strengths, sometimes even exceeding the bulk fracture strength of silicon (2.47 J/m²).
A typical process flow for fusion bonding is depicted in figure 2. The incoming bond partners (wafers A and B) are particle-cleaned via megasonic DIW cleaning in an initial step (which is optional, depending on the cleanliness of the wafers). This step is followed by plasma activation and subsequently hydration of the wafer surface via DIW rinse in order to provide OH-groups to form silanol groups at the wafer surface. The pre-treated wafers are then typically aligned to each other using a bond aligner, followed by bonding either in vacuum or at room temperature by bringing the wafer surfaces into contact (using very little or no force at all).

2. NEW MODULES

In order to enable this process flow the XBS200 cluster modules had to be extended by three dedicated process modules: AC200 for wafer cleaning, PL200 for plasma activation and MM200 for integrated in-line metrology. While cleaning and plasma modules in general have been part of previous bond clusters from SUSS MicroTec, the MM200 is an entirely new dedicated metrology platform.

2.1 AQUEOUS CLEANING MODULE AC200

The new cleaning module AC200 builds up on the experience gained at SUSS MicroTec from existing semi-automated and automated wet-processing systems. It offers single wafer cleaning with puddle and megasonic DIW rinsing.
The cleaning module allows for diluted chemistries (e.g. < 2 % NH_4OH). Organic removal functionality (SC1) is available on request.
The module also allows for optional backside rinsing and N_2 assisted spin-drying.
Different wafer chucks (e.g. edge-handling capability for perforated wafers) are optionally available.

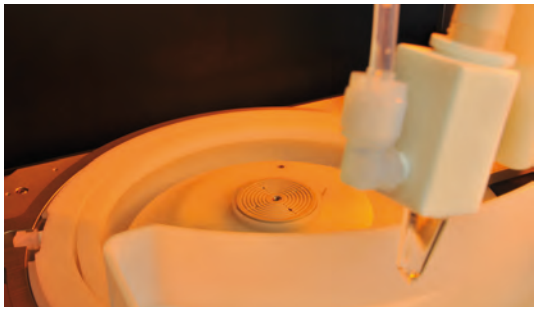

Figure 3 *Aqueous cleaning module AC200*

2.2 PLASMA MODULE PL200

The plasma module PL200 offers controlled and efficient plasma treatment and provides highest process flexibility/repeatability for plasma-based wafer surface activation.
Various process gases such as Ar, O_2, N_2 etc. and mixed chemistries can be used and are controlled via mass flow controllers (MFCs). Gate-valve loading of the PL200 is key for high-throughput handling. In general, the PL200 can also be used for plasma cleaning of polymer residues and for effective metal oxide reduction.

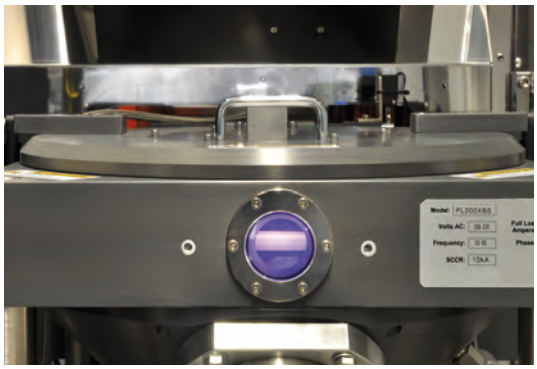

Figure 4 *Plasma module PL200*

2.3 METROLOGY MODULE MM200

Integrated in-line metrology functionality allows for fast process feedback and therefore short intervention times. The novel MM200 module therefore can play an essential role for increased process control and yield improvement.
With the absence of intermediate layers at the fusion bonding surface, particle cleanliness is crucial to obtain void-free bond interfaces. In addition to this, the verification of the post-bond alignment quality (overlay) requires quick response times in high-volume manufacturing. This is in particular the case when the overlay requirements are sub-micrometer (e.g. for wafer-to-wafer (W2W) hybrid bonding).
For this reason the MM200 module can be configured for full-field infrared (IR) void inspection and/or high precision IR overlay measurement (reflective and transmissive modes are available) including multi-site measurement capability.
The throughput- and footprint-optimized MM200 can detect voids down to 0.5 mm size and offers automatic classification and localization logging. In case of overlay measurement, the metrology system provides both high repeatability (figure 7) and high measurement resolution to serve demanding overlay requirements of <50 nm.

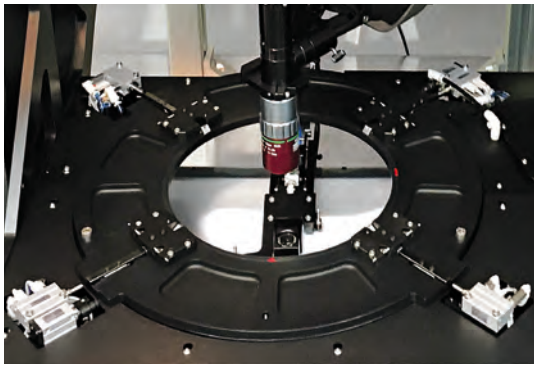

Figure 5 *Integrated metrology module MM200*

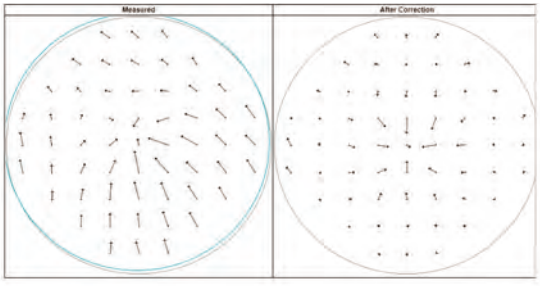

Figure 6 *Vector plot of overlay results showing the MM200 measurement results (left) and calculated bond (right) using correction values derived from the measurement.*

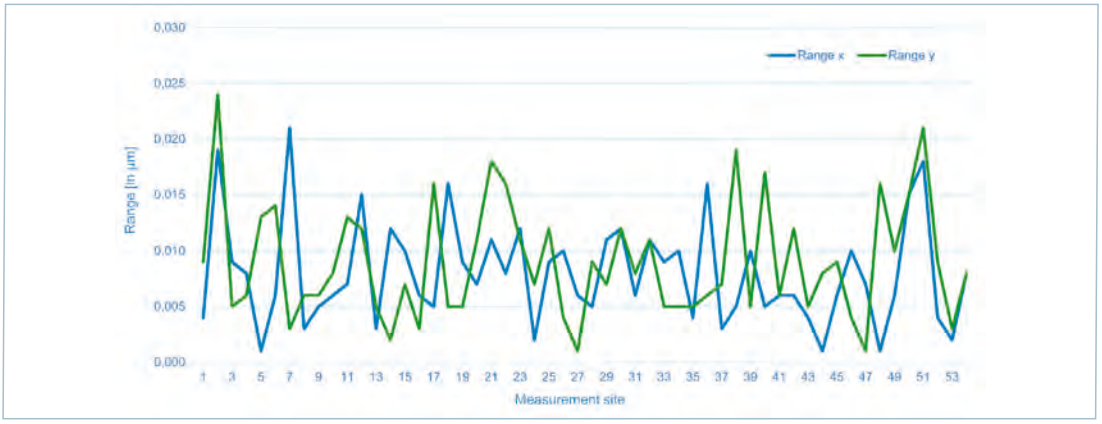

Figure 7 *Repeatability of overlay results of 53 measurement sites over 10 cycles*

In case the XBS200 is used for temporary bonding or other applications comprising adhesive layers (e.g. collective die-to-wafer bonding (D2W)[5]), the MM200 can be extended with total thickness variation (TTV) measurement functionality. Here the adhesive thickness underneath populated dies can be measured with high precision. Such data can provide valuable process information on the die-height variation on populated wafers.
Since alignment verification and defect inspection are essential for all bonding schemes, the MM200 will thus also play an important role for non-fusion bond configurations of the XBS200 in the future.
In order to improve and optimize the wafer alignment results, the MM200 provides a closed-loop feedback to the bond aligner for offset calibration and wafer run-out compensation.

Last but not least, it should be noted that due to the flexibility of the wafer handling system (6-axis handling robot) of the XBS200 platform the MM200 could be effectively designed to not occupy valuable process module footprint. The new metrology station can also be field-upgraded into existing XBS200 systems.

3. UPGRADE OF EXISTING MODULES

Since the available process modules of the current XBS200 platform had to be adapted in order to enable the fusion bonding concept, they will also be mentioned in the following.

3.1 HIGH-FORCE BOND CHAMBER XB200

The XB200 bond chamber is the cluster process module version of the stand-alone XB8 bonder. It offers a wide parameter window and is therefore ideal for all kinds of bonding schemes including metal-diffusion, eutectic, glass-frit, adhesive, anodic and fusion bonding processes.

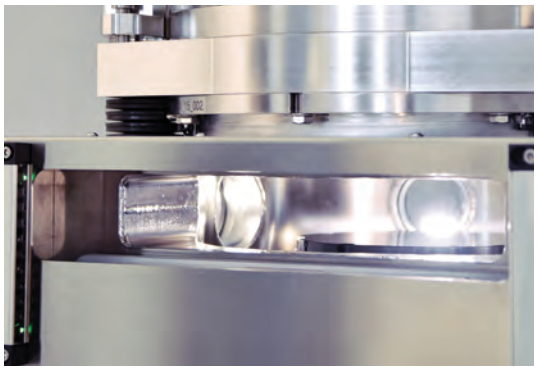

Figure 8 *XB200 high-force bond chamber*

Reproducible bonding results from wafer to wafer are essential for achieving consistently high product quality. The XB200 bond chamber consists of a closed process chamber with a gate valve for loading and unloading. During wafer transfer, the chamber is purged with nitrogen to ensure optimum cleanliness.

An external force column, consisting of a rigid three-post structure takes up the bond force applied during bonding.

This design offers maximum stiffness to avoid mechanical stress on the actual vacuum chamber, heaters and pressure plates, resulting in minimal post-bond wafer bow. Excellent temperature accuracy and reproducibility are achieved by a thermal decoupling of the heaters from the actual bond chamber. An optionally available multi-zone heater setup furthermore enables advanced temperature uniformity control across the wafer.
Active top and bottom heater cooling ensures symmetric temperature profiles as well as short process cycle-times. Water-based chiller units are used to dissipate the heat from the chamber. The innovative mechanical and thermal design concept used in the XB200 bond chamber enables optimal bonding force and temperature distribution across the wafer to ensure higher yields.

For fusion bonding under defined pressure conditions, a new wafer clamping system was developed for the XB200 bond chamber to enable transfer of aligned wafers from the handling robot without use of a center pin.

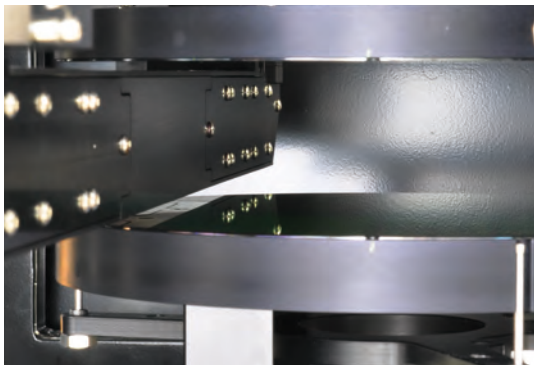

Figure 9 *XBA bond aligner*

3.2 BOND ALIGNER XBA

The high precision XBA bond aligner delivers consistent deep-submicron alignment accuracy for transparent or non-transparent wafers by using SUSS MicroTec's proprietary Inter-Substrate Alignment (ISA) technology. Built-in fixed reference targets, global calibration and overlay verification ensure optimum repeatability. Global calibration wafers (GCD) are an integral part of the aligner system and make automated calibration and overlay verification simple and quick.

To allow for highest possible alignment accuracy of aligned wafer pairs independent from potential mechanical distortions of the wafer transfer from bond aligner to bond chamber, the XBA can be provided with a unique laser pre-bond system [4] on request. Inside the bond aligner the aligned wafers can therefore be physically "tacked" at a dedicated location prior to wafer transfer to the XB200 bond chamber.

To meet even the highest requirements in W2W bonding (e.g. for small pitch W2W hybrid bonding of BSI sensors) the alignment capabilities of the XBA have been greatly enhanced. Special attention has been paid to the control of the environmental conditions at the time of bonding, enhanced wafer stage servo system, and the characterization/enhancement of all critical attributes involved in the alignment and bonding process.

The deliberate development process has lately enabled SUSS MicroTec to make a significant leap from <400 nm (3σ) to <100 nm (3σ) alignment accuracy (see figure 10), even allowing for <100 nm overlay results (see figure 11).

The enhanced <100 nm alignment functionality is optionally available and can be integrated in all existing XBS200 platforms.

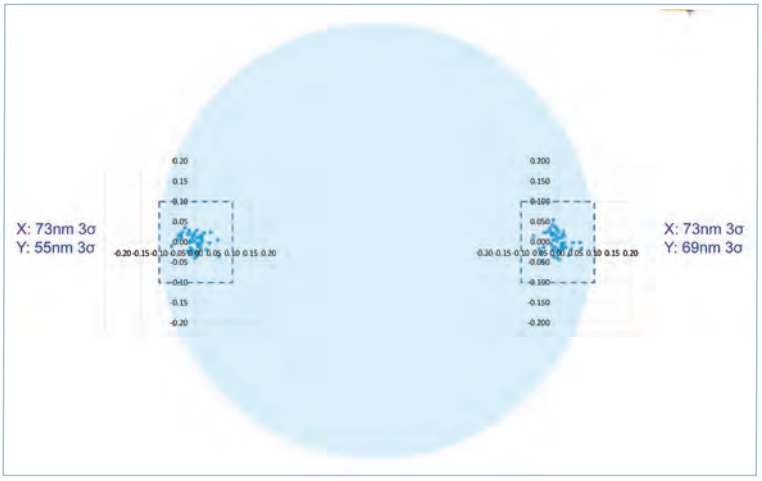

Figure 10 *XBA alignment accuracy over 55 alignment cycles (based on GCD wafers)*

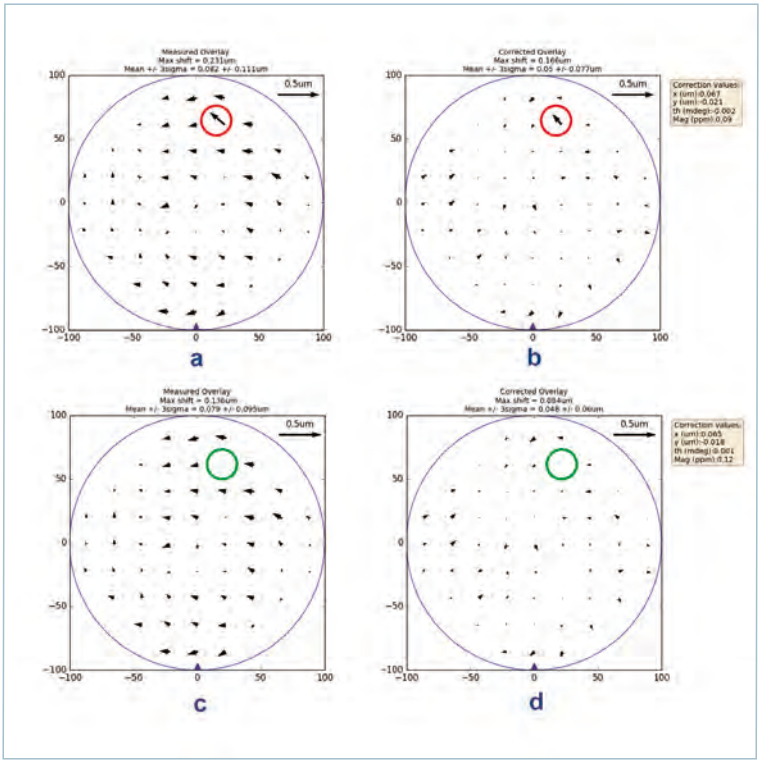

Figure 11 *Vector plot of overlay results from a 200 mm fusion bond, showing the MM200 measurement results (left) and calculated bond (right) using correction values derived from the measurement. The used wafer had a defect at one of the measurement sites, showing its influence on the vector plot*

a) Overlay results:
~80 nm mean alignment, max. overlay error: ~230 nm
b) Calculated overlay:
~50 nm mean alignment, max. overlay error: ~170 nm
c) Overlay results:
~80 nm mean alignment, max. overlay error: ~140 nm
d) Calculated overlay:
<50 nm mean alignment, max. overlay error: ~85 nm

4. CONCLUSIONS

With the new XBS200 permanent bond cluster dedicated for fusion wafer bonding SUSS MicroTec is offering a modular and highly competitive bonding platform with integrated in-line metrology functionality for high-throughput and improved yield requirements.
The system was designed to target MEMS & sensor applications that require fusion bonding (e.g. microfluidics and RF-MEMS). Additionally the greatly enhanced alignment capability can be used to address even more demanding semiconductor application such as CIS, 3D stacked memory and 3D SoC.

The next SUSS Report will therefore cover the extension of the adapted process modules towards 300 mm and highlight results obtained on a dedicated platform for W2W and collective D2W hybrid bonding on 300 mm wafers at SUSS MicroTec.

Thomas Schmidt studied Microsystems Technology at the University of Applied Sciences Kaiserslautern in 2001. In the following years he has held various positions in MEMS/semiconductor processing and has also lectured on advanced lithography as well as on MEMS and CMOS fabrication.

Since 2017 he is Product Manager at SUSS MicroTec with responsibility for the product line "Permanent Wafer Bonding" focusing on automated cluster platforms. This platforms address established bonding techniques for the MEMS/semiconductor industry as well as advanced packaging.

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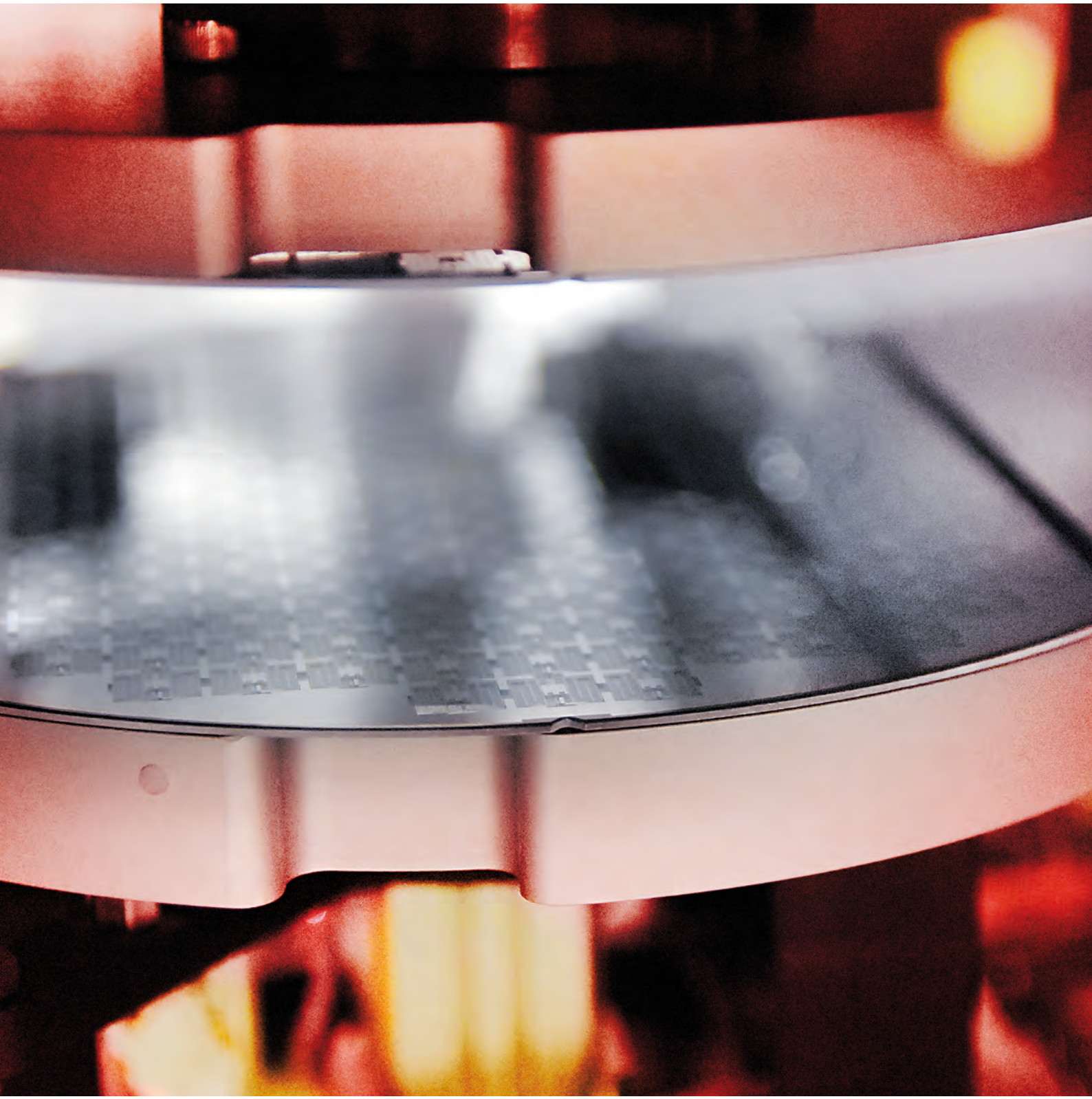

SMART RECOVERY AFTER ROBOT HANDLING FAILURE

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Björn Böckle, Dr.-Ing. Thomas Grund SUSS MicroTec Lithography GmbH, Sternenfels, Germany

In our industry, an increasing number of substrates are deviating from the SEMI standard for silicon wafers. For example, reconstituted wafers for fan-out wafer-level-packaging applications show high warpages, and materials for the RF-MEMS area like lithium niobate ($LiNbO_3$) or lithium tantalate ($LiTaO_3$) are very brittle and tend to break easily. These new challenges are being addressed by novel handling solutions where robot end effectors or vacuum chucks are designed to tolerate higher substrate warpage. Nevertheless, especially with these non-standard materials, handling failures cannot be entirely avoided. Until now, typically the tool will stop any substrate transfers upon a handling error and the intervention of an operator is required to resolve the issue. Not only does this require highly trained and experienced personnel, it also leads to a loss of throughput. Even worse, scrap rates can also increase since during a complete handling stop substrates might stay in process stations for too long and become damaged. A typical example is overbaking in a hotplate with coatings that cannot be stripped afterwards.

SUSS tools are capable of using two different scheduling strategies. Depending on process requirements, either a fixed deterministic pattern can be used to ensure stable process timings (cyclic dispatcher mode), or a powerful and optimized scheduling algorithm can be chosen which adapts itself to the current status of the machine (Decision On the Fly dispatcher mode) and which provides the ability to run different sequences in parallel.

SUSS MicroTec has now further developed its leading Decision On the Fly scheduling algorithm by adding advanced error recovery functionalities. A handling error is typically detected by missing vacuum. Either after putting the wafer to e.g. a coater chuck (PUT), or after getting the wafer out of a module (GET) the vacuum on the chuck or end effector cannot be built up to a high enough level to be detected. The machine software interprets this as a lost substrate. Since the substrate might be still there but is just not detectable by vacuum (e.g. due to a high bow of the substrate and therefore a vacuum leak), the robot will perform a couple of safe moves with the new algorithms, and then continue processing the rest of the wafers currently in process.

First consider a single arm robot machine. In case of a PUT failure, the robot will then perform a PUT to a buffer station, just in case the wafer is still actually on the robot end effector. The same error handling will happen on a GET fail. The machine will assume that there is still a substrate on the end effector and transfer it to a buffer station. The machine will stop transferring any new substrates into the machine but as the end effector is available again, it can finish the substrates already started processing. The process module that was involved in the handling error is not used for finishing the substrates left and can be inspected afterwards.

Figure 1 *ACS200 Gen3*

In the case of a machine with a dual arm robot, the algorithm takes it even one-step further. First, the robot end effector involved in the handling error is cleared as described before. Then not only the process module is paused but also the involved robot arm is blocked for further use. As the second arm is still fully available the machine keeps on finishing substrates as with a single arm robot. After all wafers in the process chain are finished, an operator or equipment engineer can check the tool status and bring it up into full production.

With the new advanced error recovery features, SUSS MicroTec takes its Decision On the Fly scheduling algorithms to the next level. The machines behave more intelligently and help to mitigate any effects from handling errors. Less operator intervention, reduced scrap rate and increased throughput are the benefits for every customer.

The new features are available during Q1 2020 on most SUSS machines using the MMC software platform. Various customized recovery scenarios can be easily configured.

Michael Brennen received a degree in Computer Science from the University of Vermont in 1987. After graduating he worked at several companies on technologies ranging from telecommunications to financial trading systems. He joined SUSS Microtec in 1997 as a Senior Software Engineer and has worked on numerous projects for the bonder and coater product lines since then, including being the software lead for the company's first automated bonding system.

ENABLING HETEROGENEOUS INTEGRATION FOR NEXT GENERATION FAN-OUT APPLICATIONS USING FULL-FIELD PROJECTION SCANNING

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The demand for higher functionality devices drives integration technologies in the third dimension to overcome limitations in Moore's Law. One popular example for 3D Integration is Package-on-Package (PoP), where memory stacks are mounted above the processor. Heterogeneous Integration (HI) is one of the key technologies to meet future fan-out (FO) application standards using higher bandwidths and higher chip-to-chip interconnection density or IO density. However, HI brings new challenges like large-area panel production and design limitations. Fast increasing package size in combination with insufficient increase in stepper reticle size is inhibiting designs for large packages and HI applications.

A solution which provides limitless design and fine resolution patterning capabilities is a full-field projection scanner. For next generation FO applications, a projection scanner provides superior performance compared to a stepper by enabling limitless design, allowing dies of any size and patterning of non-repeated features at higher throughput and lower cost.

This paper presents technical challenges and provides solutions for future HI FO applications, using a full-field exposure system for large package integration, eliminating low yielding stitching steps. High accuracy overlay, fine resolution for RDL routing and large depth of focus (DOF) for thick resist applications with high aspect ratio is demonstrated. The extendibility to large panel packaging integration is discussed.

Key words: *Advanced Packaging, Package-on-Package (PoP), 2.5D, 3D, Projection Lithography, High Aspect Ratio, Heterogeneous Integration (HI), Fan-Out (FO), RDL, FO WLP, FO PLP.*

1. INTRODUCTION

The increasing demand for higher functionality and bandwidth is not only pushing the boundaries of Moore's Law but already reaching the limits of physics [1]. To overcome the limitation of ever decreasing transistor size, new FO integration technologies have been developed.

Moore pursues the increase in performance by further miniaturization of CMOS technology incorporating new materials and applying new transistor concepts [2].

The increasing density of transistors by continuous physical scaling correlates with the increase in device performance in particular with functionality and bandwidth. However, for the past decade, while I/O density is increasing and shorter communication paths are created, the operation frequency is saturating as seen in Figure 1.

Advanced mobile devices, wearables and the Internet of Things (IoT) require increased miniaturization and integration in advanced packaging.

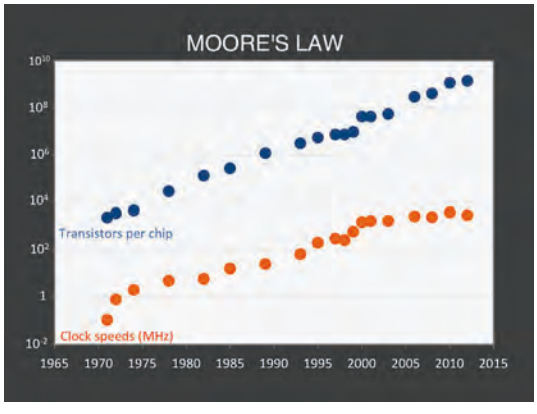


Figure 1 *Moore's Law (Source: Intel)*

One approach to address the heterogeneous integration of multi-functional systems in one package is System-in-Package (SiP). HI will close the gap between integration and functionality density [3]. This will create new system-level design innovations leading to large packages > 400 mm² and very large packages > 2500 mm² for FO SiP, FO PoP with TMV and FO on substrate [4].

Challenges in HI FO applications can be addressed with a full-field projection scanner enabled by limitless design without stitching for next generation system-level design innovations. Overlay accuracy below +/- 0.7 µm for 3D Integration, large DOF for thick resist applications with aspect ratio greater than 6 for tall Cu pillars and fine resolution down to 1.5 µm for RDL routing were demonstrated while maintaining higher throughput and lower costs than stepper alternatives.

2. HETEROGENEOUS INTEGRATION

High IO density applications have started to use packages with FO solutions. Future applications will be more complex including FPGA, high level processors and high demanding CPU/GPU and the memories associated. Such high performance heterogeneous systems, especially those with embedded large dies will result in very large package sizes, > 50 x 50 mm² or even bigger [4]. Using steppers with large reticle size is very cost intensive, while the scanning technology is able to significantly reduce costs.

Traditionally, steppers are used for exposing the vias and RDL for the electrical interconnect, but the package sizes now exceed the reticle exposure field. Stitching is the technology used to fit smaller exposure fields back together. Unfortunately, stitching involves further process steps and increases yield loss, due to reticle shifts in x, y and theta. In total more than 28 error combinations during stitching are possible. Both factors, additional processing and yield loss increase the production costs incurred.

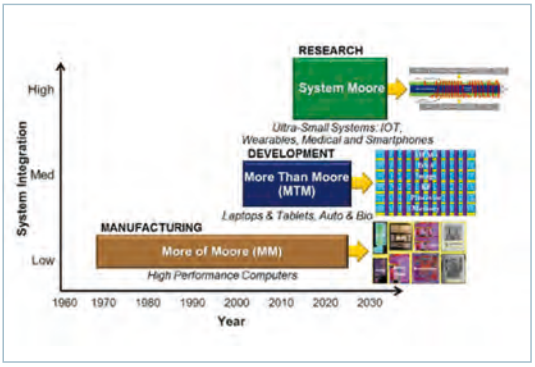


Figure 2 *System integration roadmap*

Furthermore, stepping technology does not allow for limitless design and patterning capabilities. Figure 3 is showing a combination of various dies on one wafer which can be exposed with a full-field projection system, but has no stepper solution. Full-field projection scanning enables for heterogeneous layout of dies and patterning of non-repeated features necessary for next generation HI FO applications.

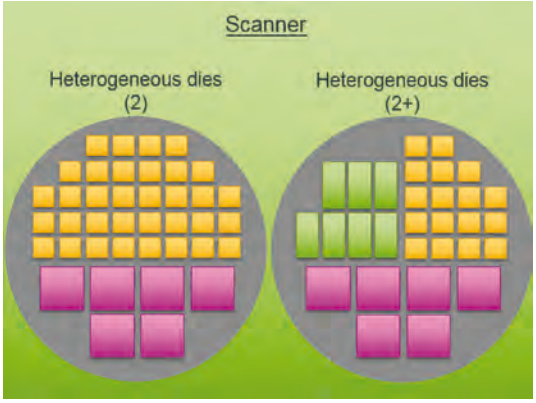


Figure 3 *Heterogeneous Die Layout*

To overcome challenges for future HI FO applications, a system providing large die scalability and production of non-repeated, heterogeneous patterns by maintaining large DOF, fine resolution and accurate overlay capabilities at high throughput and low cost of ownership is needed.

The full-field projection scanner provides the technology enabling future heterogeneous systems, FO SiP and FO PoP. Along with a reduction in total cost of ownership, the full-field projection scanning technology eliminates design limitations and makes place for new heterogeneous system designs and applications.

3. PHOTOLITHOGRAPHIC TECHNOLOGY FOR HI FO APPLICATIONS

Projection scanning systems are the best suitable lithographic choice, that enable next generation HI FO applications by providing limitless design at high performance.

The projection scanning involves aligning a full-field mask to the substrate and then projection the mask pattern onto the substrate by means of scanning. This approach provides high throughput up to 100 wph at 400 mJ/cm² dose. With similar optics, the stepper has to step and repeat whereas the scanner can continuously expose. As a result, higher throughputs are achieved, which in turn provides lower cost of ownership (CoO) [5].

With lower imaging numerical aperture (NA) projection systems in back-end-of-line (BEOL) have higher DOF than their front-end counterparts. The relationship between DOF and NA is expressed by

$$DOF = \pm k_2 \lambda / (NA)^2 \qquad (1).$$

Where λ is the wavelength of the light source and k_2 is a material/process constant. The UV projection scanner has the perfect balance of DOF and resolution (R), for both, fine resolution below 3 µm and large DOF for thick resist applications, with an integrated variable σ expressed by

$$\sigma = \frac{NA_{illumination}}{NA_{image}} \qquad (2).$$

The ability of automated variable σ provides the projection scanner with a unique feature, enabling resist specific optimizations for fine resolution down to 2 µm and large DOF achieving high aspect ratio. Furthermore, side wall angle variation can be achieved by alternating the edge intensity using σ shown in Figure 4.

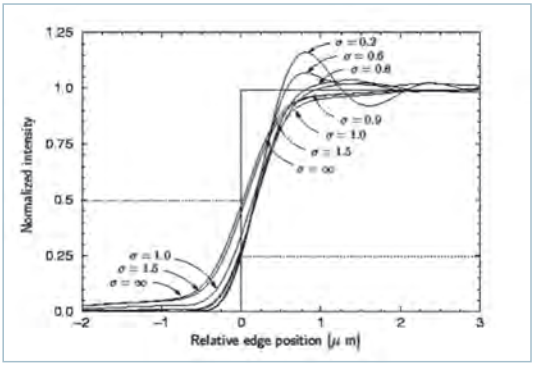


Figure 4 *Alternating edge intensity using various σ [6]*

The adapted Rayleigh's criterion for resolution in relationship with image *NA* and σ is expressed by

$$R = \frac{k_1 \lambda}{NA\,(1 + \sigma)} \qquad (3).$$

Where k_1 is a material/process constant, *NA* the image *NA* and σ expressed by formula (2) [6].

A schematic setup of the projection scanner technology for 300 mm wafers is demonstrated

in Figure 5. Next to the variable σ selection in the Wynne-Dyson projection optics, the full field continuous serpentine exposure path is shown. Die-shifts can be compensated by beam steering and mag correction achieving higher through-put than die-by-die solution.

4. PHOTOSENSITIVE MATERIALS

To showcase the full-field projection scanner's capabilities, a comprehensive selection of photosensitive materials was chosen, providing unique performance in their application for resolution, DOF and overlay.

Resist	Film Thickness	Target Features
TOK PW1000T	7 µm	2/2 µm L/S
PXi-105J12US	6 µm and 9 µm	2/2 µm L/S
TOK's CV1000	20 µm	2/2 µm L/S
AZ-SLD2530	3 µm	Overlay

Table 1 *Resist choice*

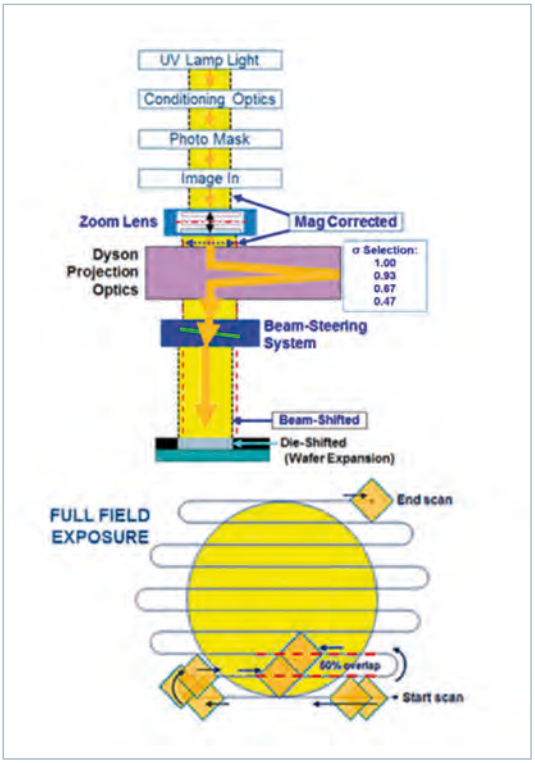


Figure 5 *Principal of projection scanning technology*

TOK's PW-1000T is widely used in the semiconductor industry mostly used for Cu-RDL and was chosen to represent a standard resist for base line evaluation. A film thickness of 7 µm was targeted to achieve 2/2 µm line and space features.

Sumitomo's PXi-105J12US is a positive-tone, chemically amplified (CA), i-line resist. CA photoresists are superior to their older and cheaper Diazonaphthoquinone (DNQ) counterparts for high aspect ratio applications. CA photoresist have high photo speeds and high contrast enabling near vertical sidewalls. In this paper PXi-105J12US is used to showcase lithographic performance in 6 µm and 9 µm thick resist. Due to its high contrast and enabling near vertical sidewalls, this material is particular well suited for fine line RDL structures.

TOK's CV1000 is a positive-tone, chemically amplified resist chosen. The resist provides fine resolution and aspect ratios for thicknesses up to 20 µm.

Lastly, EMD's AZ-SLD2530 was chosen at a film thickness of 3 µm, to demonstrate overlay performance. AZ-SLD2530 is a g-line and broad-band, positive-tone, DNQ-resist.

All of the materials were developed with AZ 726 MIF (metal ion free), an aqueous developer with 2.38 % TMAH and a surfactant for improved wetting. Scumming was reduced in the develop step by using a pressurized fan spray. Removal during the develop step is preferable to the descum step because the plasma process generates undesirable roughness in the via sidewall and requires a separate tool.

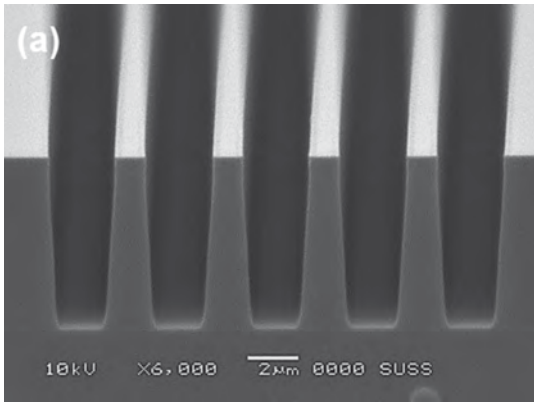
5. EXPERIMENTAL RESULTS

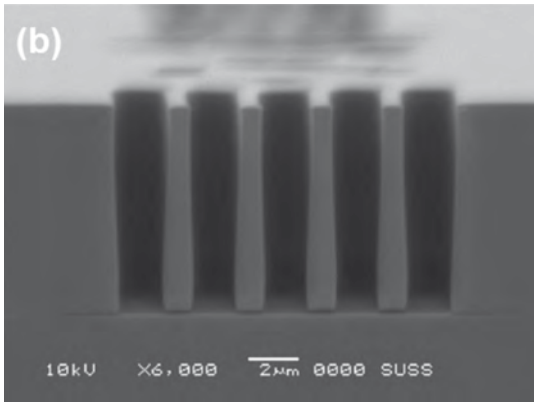
All resists were coated using a manual 300 mm spin coater.

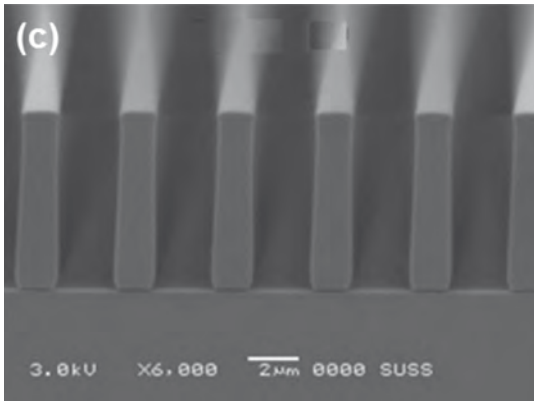
TOK's 1000T (a)
Target film thickness of TOK PW-1000T was 7 µm with a resolution of 2/2 µm line and space with a side wall angle of 88°. An aspect ratio of more than 3:1 was achieved. For the substrate a bare silicon wafer was used.

Sumitomo's PXi-105J12US (b)
An aspect ratio of 6:1 was demonstrated in Sumitomo's PXi-105J12US. For the substrate, silicon wafers with sputtered Ti/Cu seed layer were used to match realistic reflection conditions for typical RDL plating applications. Target thickness of 9 µm with resolution of 1.5/1.5 µm line and space was achieved.
The exposure parameters were optimized using a Focus-Exposure Matrix (FEM). The best profile was achieved using 360 mJ/cm² with a focus offset into the resist. Furthermore, an illumination NA of 0.07 was selected which transforms into a partial coherence σ = 0.48. With lower Sigma higher edge intensities for pattern improvement could be achieved.

Sumitomo's PXi-105J12US (c)
The second process with PXi-105J12US was targeting a film thickness of 6 µm with a 1:1 resolution of 2/2 µm line and space. A sidewall angle of 90° ± 1° was demonstrated. The best exposure condition was achieved with 330 mJ/cm² and 6 µm focus offset into the resist. As in the previous result a PEB step was introduced.
To determine the optimum process conditions, an FEM matrix was generated on the projection scanner system using multi-scan stepping mask enabling over 25 exposure conditions on one wafer. This yielded a dose latitude of 30 % ± 2 % and a focus window of 12 µm ± 2 µm.

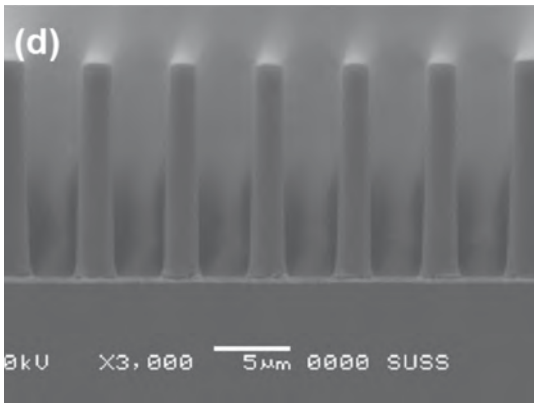






TOK's CV1000 (d)

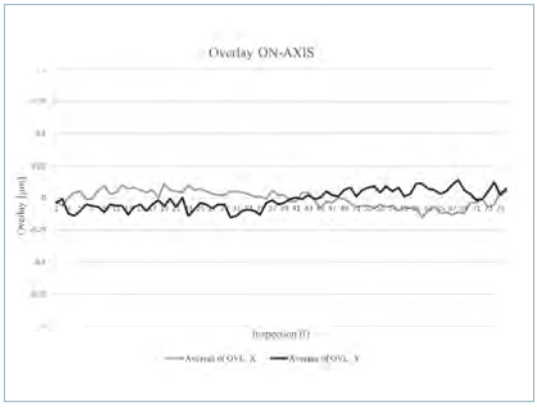
Target thickness of TOK CV 1000 was 14 µm with a resolution of 2/2 µm line and space, to achieve an aspect ratio of 7:1. For the substrate, a Silicon Wafer sputtered with Ti/Cu as seed layer was used. The following best exposure parameters were chosen: dose of 450 mJ/cm², broadband (ghi-line) focus at zero.



EMD's AZ-SLD2530

EMD's AZ-SLD2530 resist was chosen to determine the overlay capability of the full-field exposure scanner. Target thickness of 3 µm was coated. In the first step, the wafer was aligned and exposed. After development, the same wafer is used for a second iteration. This time the pattern of the developed wafer was aligned to the mask pattern followed by an exposure and development.

To verify overlay capability, the relative position of the first and second layer was measured. We used the alignment cameras of the projection scanner as an on board metrology system with an accuracy of 100 nm was used. For each wafer, 25 evenly distributed measurement points across the wafer were taken. An accuracy error of less than ± 0.7 µm for 3 σ was detected.



6. CONCLUSION

Resolution down to 1.5 µm, aspect ratio of 7:1, large process windows (focus and dose latitude) for 2/2 µm line and space as well as high overlay accuracy below ±0.7 µm were successfully demonstrated. These achievements suggest the superior tool performance of the fill-field projection scanner for a wide range of processes from fine resolution RDL to thick resist application and tall copper pillars, which enables to make full use of the unique capabilities, such as limitless design with no stitching, enabling next generation fan-out heterogeneous integration applications.

Acknowledgements

The authors would like to thank Sumitomo, EMD, TOK, and MicroChem for providing their materials for testing. They would also like to thank Jose Martinez for his support in coating and developing.

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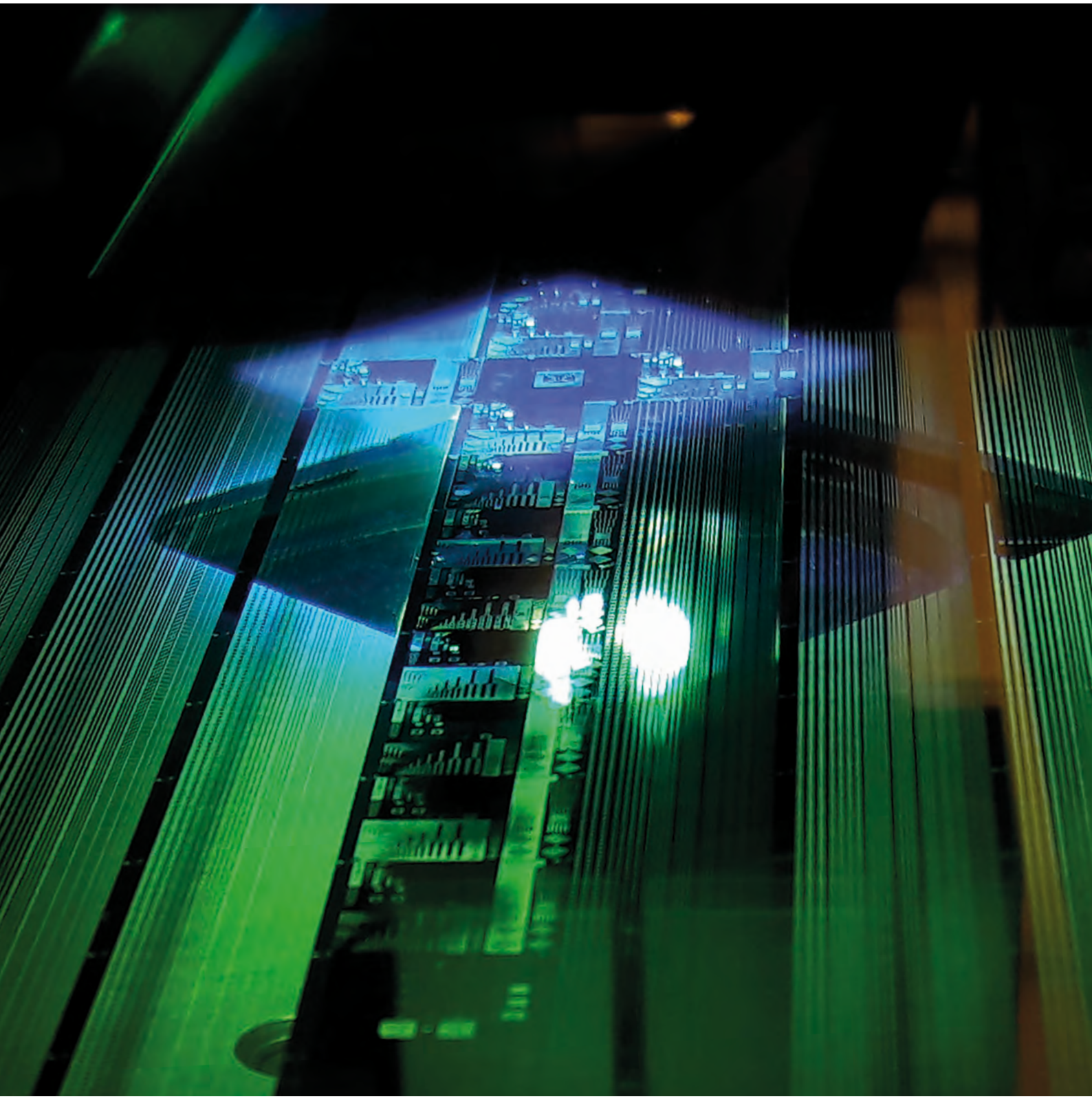

Imprint

Publisher:
SÜSS MicroTec SE
Schleissheimer Str. 90
85748 Garching, Germany
info@suss.com

Register Court Munich
HRB Nr. 235132

Value added tax identification number:
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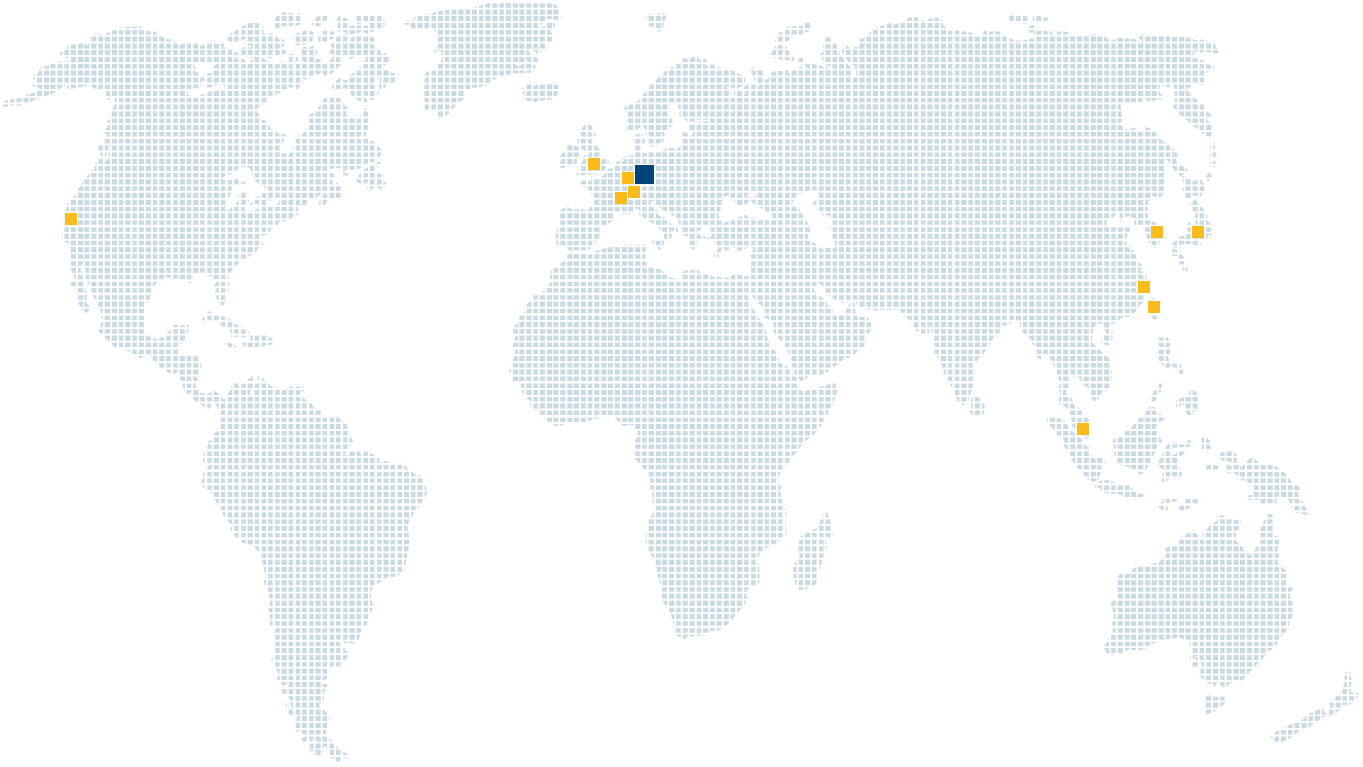

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