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Strong Partners for Technology Leadership:

Panasonic's Plasma Dicing Technology

The plasma dicing technology offers many advantages over conventional mechanical (blade) dicing.

Local Plasma Treatment in a Mask Aligner

Plasma pre-treatment for low-temperature direct wafer bonding is used worldwide in many different applications. An article by Fraunhofer IST and SUSS MicroTec.

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Frank Averdung, SUSS MicroTec

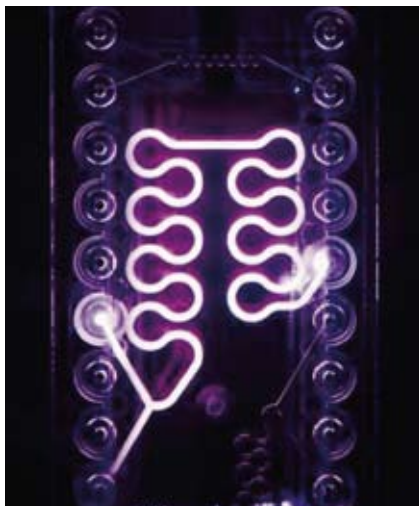
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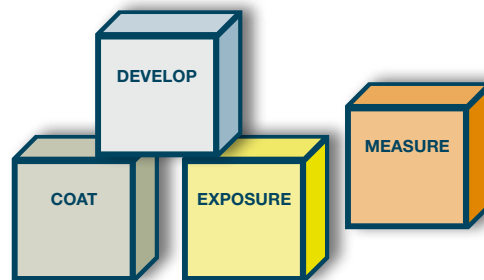
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Full View

Strong Partners for Technology Leadership

When two or more organizations combine their technological knowledge to create new, innovative products and technologies the output is bound to be so much stronger. Strategic alliances are powerful tools on the way to new insights and smarter, better connected solutions. As Bill Gates once admitted: "Our success has really been based on partnership from the very beginning." Motivations behind each alliance range from influencing industry standards to extending product portfolios and reaching into new markets. The globally intertwined airline business today provides an excellent example of the importance of alliances.

SUSS MicroTec has experience in joint research and development with leading semiconductor companies and institutes. As a supplier for state-of-the-art technologies, these types of exchanges have been vital for SUSS MicroTec and are key to today's success. First, being approached with individual research needs helps to meet general market requirements and to design product roadmaps. Second, knowledge and expertise grow with each technology development. The venture pays off as the output generates skilled staff for process technologies of multiple applications. Finally, a third benefit lies within the economic nature of a joint venture. Aligning efforts and pooling resources means reducing necessary expenses for research and development while achieving competitive advantage.

Our recent technology partnerships in the field of 3D integration places us

as one of the key players in the global game. Due to joint development efforts with 3M and Thin Materials, SUSS MicroTec so far is the only equipment supplier that can offer various technologies for the critical temporary bonding and debonding processes. With participation in ITRI's AdStack demo line and imec's 3D research program, SUSS equipment is being deployed in the "Hot Spots" of 3D integration technology innovation. The outcome is yet to be seen as installation is in process. It is to be expected that our customers will strongly benefit from those experiences.

The two plasma-based research projects introduced in the following pages are examples of other fruitful alliance. The cooperation between SUSS MicroTec and Fraunhofer IST goes back to 2002 and has resulted in a joint patent for selective plasma treatment. This process offers a wide range of possibilities for MEMS applications. Furthermore, we have developed a plasma-based method for wafer dicing on SUSS lithography equipment together with Panasonic Factory Solutions which replaces conventional dicing methods with a cost-efficient alternative.

With the majority of our efforts focused on minimizing production time, increasing yield and throughput and reducing overall costs, we share many common goals with other companies in the industry. We are looking forward to working with partners to develop innovative and intelligent solutions.



Frank Averdung

President & CEO, SUSS MicroTec AG

Strong Partners for Technology Leadership

Panasonic's Plasma Dicing Technology

Kiyoshi Arita, Plasma Process Development Group, Development Center Panasonic Factory Solutions Co., Ltd.



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In a joint project Panasonic Factory Solutions and SUSS MicroTec are developing a plasma dicing process that involves photolithography and plasma etching. Plasma dicing offers cost advantages over other dicing technologies for wafers with small dies and yields an exceptional ultra-fine dicing result without chipping effects. The lithography process has been developed on SUSS MicroTec's integrated Litho-Pack300 cluster. The plasma dicing step is performed on a PSX800 from Pasasonic Factory Solutions.

ABSTRACT INTRODUCTION

We have developed plasma dicing technology as an alternative dicing technology of conventional mechanical (blade) dicing. The main advantages of plasma dicing over the conventional dicing are "damage free", "chipping free", "particle free", "water free" and "heat free". We will introduce the features of plasma dicing process and its applications.

PLASMA DICING PROCESS

Currently the most common dicing process is mechanical dicing which uses diamond blades. However as the wafer thickness has been thinner-less than 50 μ m and fragile low-k material has been pretty common recently, the mechanical dicing is no longer the only one solution because it could give physical damage to the chip.

We have come up with the plasma dicing technology in order to solve these problems. Figure 1 shows the schematic comparison between mechanical blade and plasma dicing process. In the case of mechanical blade dicing, a diamond blade is used to cut the wafer

so physical damage to the chip cannot be eliminated. Especially if the chip thickness is very thin such as less than 50 μ m, this physical damage to the chip could be the crucial problem. However plasma dicing would never cause any physical damage to the chip

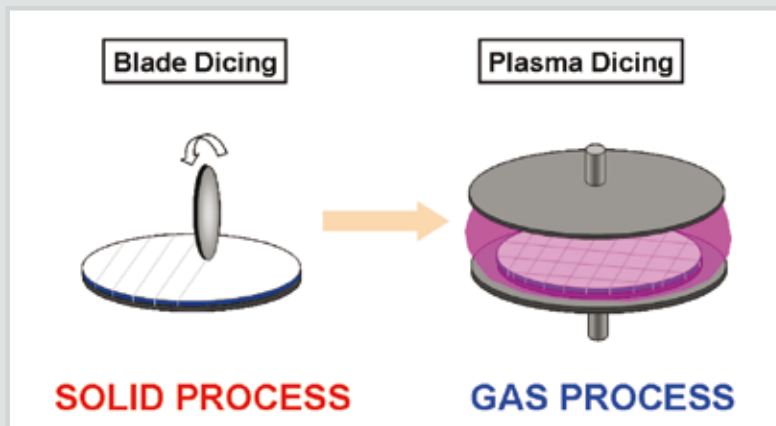


Figure 1:
Schematic comparison
between blade and
plasma dicing

regardless of the thickness of wafer. Of course we know that plasma etching speed is lower than one of the mechanical dicing, but there is no distinction between the two when the wafer thickness becomes thinner and thinner. Therefore plasma dicing technology is considered as one of the ideal dicing technologies in the future.

Figure 2 shows the fundamental plasma dicing process flow. First of all, back grinding (BG) tape is covered on the top surface of the wafer in order to protect active devices.

Secondly, the back grinding process is implemented from the back side of the wafer to thin the wafer. Since the damaged layer is generated by the back grinding process, the plasma stress relief process which uses SF6 gas is carried out in order to remove the damaged layer. After the plasma stress relief process, the spin coating of the photo resist and photolithography process are conducted for the patterning. Then the wafer is cut by plasma dicing process which uses SF6 and O2 mixed gas. After the plasma dicing process, the photo resist is removed by O2 plasma ashing process.

After the photo resist removal, the dicing tape for chip bonding is placed on the back side of the wafer. Finally the back grinding tape is removed with test element groups (TEG). All three plasma processes, which are plasma stress relief, plasma dicing and O2 plasma ashing process, can be carried out by only one equipment.

STRONG WORKING RELATIONSHIP WITH SUSS MICROTEC

Figure 3 shows the process step of plasma dicing, the SUSS MicroTec and Panasonic systems and the wafer surface photographs before and after plasma dicing process. SUSS and Panasonic have developed the new photolithography technology for plasma dicing process. Spin coating process, baking process and exposure process for the very thin wafer are difficult, because it has warpage. In order to correct the warpage of very thin wafer, SUSS MicroTec has developed new wafer transfer systems and new wafer stage in their photolithography system.

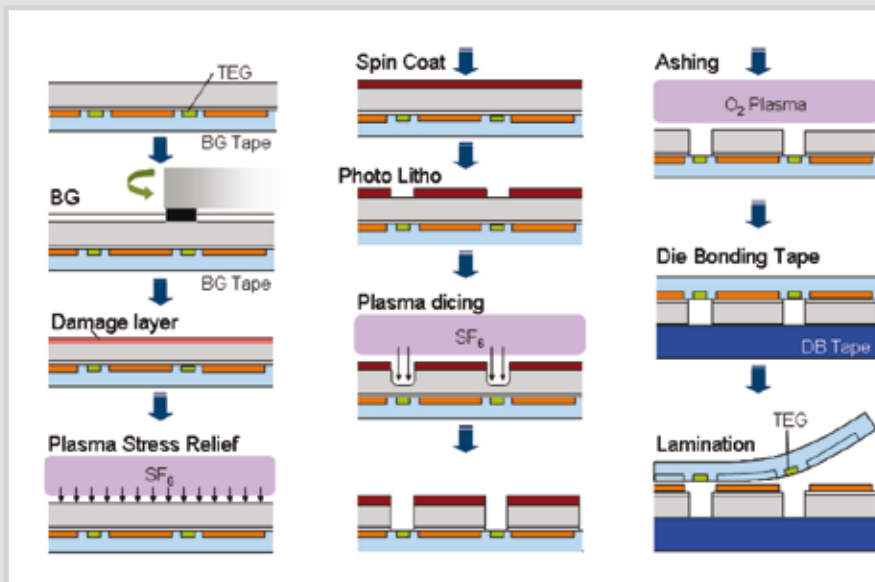


Figure 2: Fundamental plasma dicing process flow


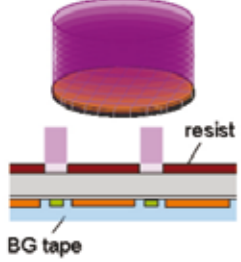


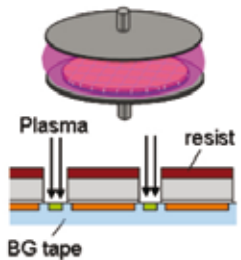

Step	System	Process	Photos of wafer surface
Step 1 Photo Lithography Process	 LithoPack300 (SUSS)	 resist BG tape	 Back side of the wafer after photo-litho process
Step 2 Plasma Dicing Process	 Plasma Dicer PSX800 (PFSC)	 Plasma resist BG tape	 Back side of the wafer after plasma dicing process

Figure 3: Collaboration between SUSS MicroTec and Panasonic for plasma dicing process

THE ETCHING MECHANISM OF PLASMA DICING

In the case of plasma dicing technology, the anisotropic etching is required to cut the wafer and we use SF6 and O2 mixed gas plasma in order to realize it. Figure 4 shows the mechanism of anisotropic etching when using SF6 and O2 gas. Fluorine including ions such as SF5+ move toward the Si bottom surface and react with Si and produce volatile SiF4. At the same time, fluorine radicals and oxygen radicals react with Si surface and make the Si_xO_yF_z film deposition on the sidewall. Then the etching to lateral direction stops. That's how the anisotropic etching can be achieved.

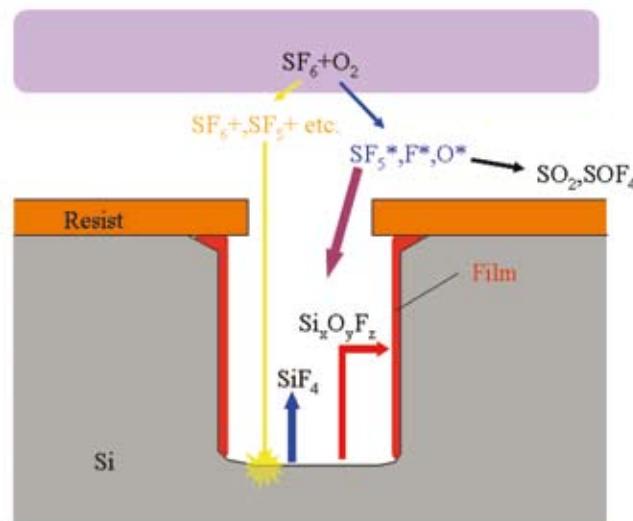

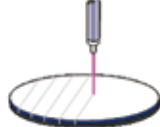
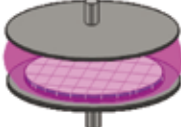


Figure 4: Mechanism of anisotropic etching

Figure 6:
Comparison of various dicing technologies

Process	Blade dicing	Laser dicing	Plasma dicing
Figure			
Dicing method	Dicing blade	Laser	Fluorine plasma
Dicing speed	×	△	⊙ (small chip)
Die strength	×	△	⊙ (damage free)
Low-k	×	○	⊙ (dry & low-temp)
Running cost	○	○	△ (mask cost etc.)

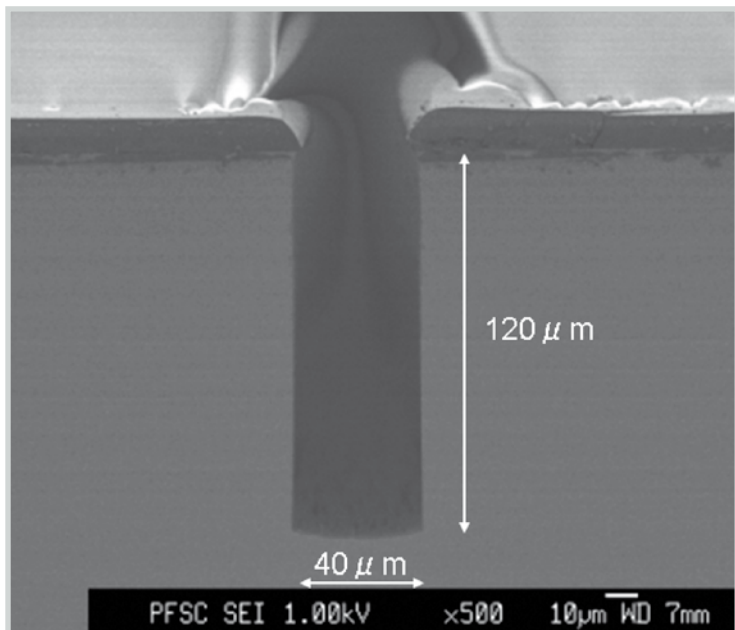


Figure 5:
Cross section SEM micrograph of etching profile after plasma dicing

Figure 5 shows the actual scanning electron microscope (SEM) cross section micrograph of the etching profile by plasma dicing. The etching rate is about 10μm/min.

THE ADVANTAGES OF PLASMA DICING PROCESS

One of the great advantages of plasma dicing is the capability of damage free dicing. Since it doesn't require the mechanical blade, it doesn't cause any physical damage to the chip.

Figure 6 shows the comparison of various dicing technologies. The laser dicing process may be effective as well in terms of mechanical damage free but it still could give heat damage to the chip resulting in low chip strength. Next great advantage of plasma dicing is

Figure 7:
Productivities as a function of chip size for mechanical and plasma dicing

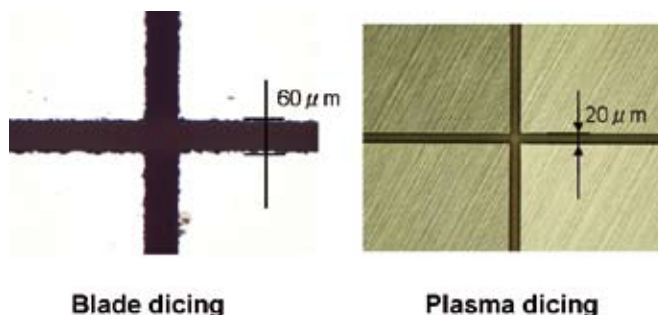
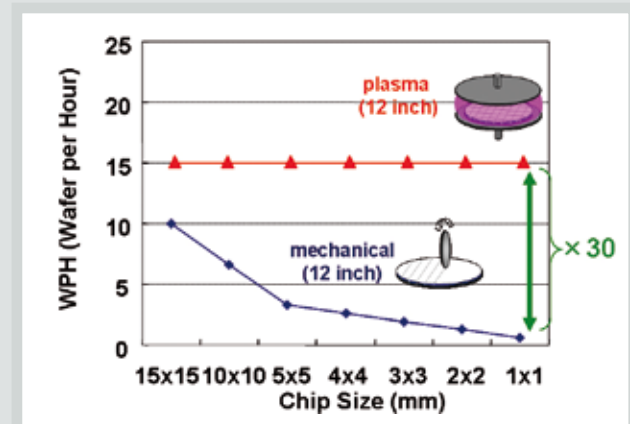


Figure 8: Dicing line comparison between blade and plasma dicing

high productivity. Especially the smaller the chip size becomes such as RFID (radio frequency identification) devices, the higher the productivity of plasma dicing process can be.

Figure 7 shows the relationship between the productivity and the chip size for both mechanical and plasma dicing processes. The productivity of mechanical dicing extremely depends on chip size while that of plasma dicing is always constant regardless of chip size. In case of 1mm×1mm chip size, the productivity of plasma dicing is 30 times higher than that of mechanical dicing. So we can conclude that the plasma dicing process is very effective for small chip size devices such as RFID in terms of high productivity.

Figure 8 shows the dicing line comparison between mechanical blade dicing and plasma dicing process. In case of plasma dicing, there is no chipping observed and the dicing width can be reduced as low as 20μm. On the other

hand in case of mechanical blade dicing, the chipping issue is observed and the dicing width is much wider than the case of plasma dicing.

Figure 9 shows the cross section views of the chip after mechanical blade dicing and plasma dicing. As shown in this figure there is a about 500nm thick damaged layer after mechanical blade dicing but in case of plasma dicing there is no damaged layer at all. This damage free feature of plasma dicing can lead to higher chip strength as well.

The chip strength measurement results of both mechanical blade dicing and plasma dicing are shown in Figure 10. In case of mechanical blade dicing, all about 200 measurement data are below 1000MPa on the other hand the average chip strength is more than 3000MPa in case of plasma dicing. This high chip strength data is one of the evidence of damage free feature of plasma dicing process. The high chip strength is especially important when it comes to

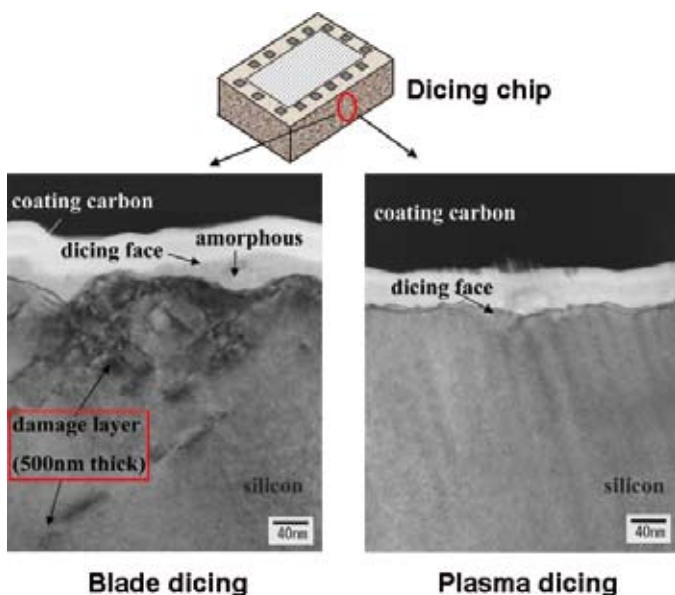


Figure 9: Cross section transmission electron microscope (TEM) micrographs of chip after blade dicing and plasma dicing

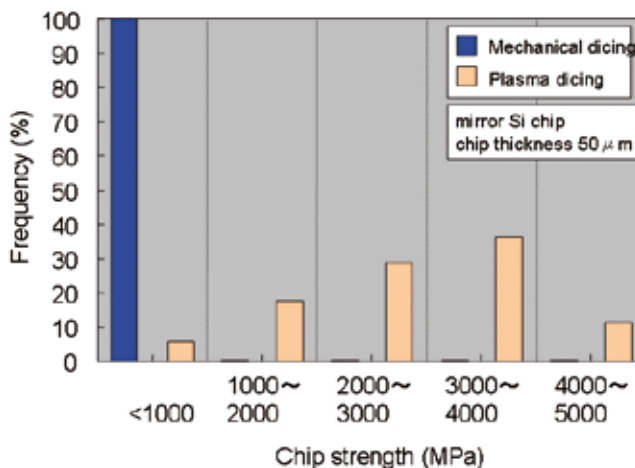


Figure 10: Chip strength measurement results of mechanical dicing and plasma dicing

very thin wafers because they are extremely fragile.

Another unique advantage of plasma dicing is the flexibility in diced shape. Since it doesn't need mechanical blade, you can create free chip shape such as circular chip and hexagonal chip. Actual circular chips and hexagonal chips we have made are shown in Figure 11. We are currently looking for the possibility if this free shape dicing capability can be used for micro electro mechanical system (MEMS) manufacturing.

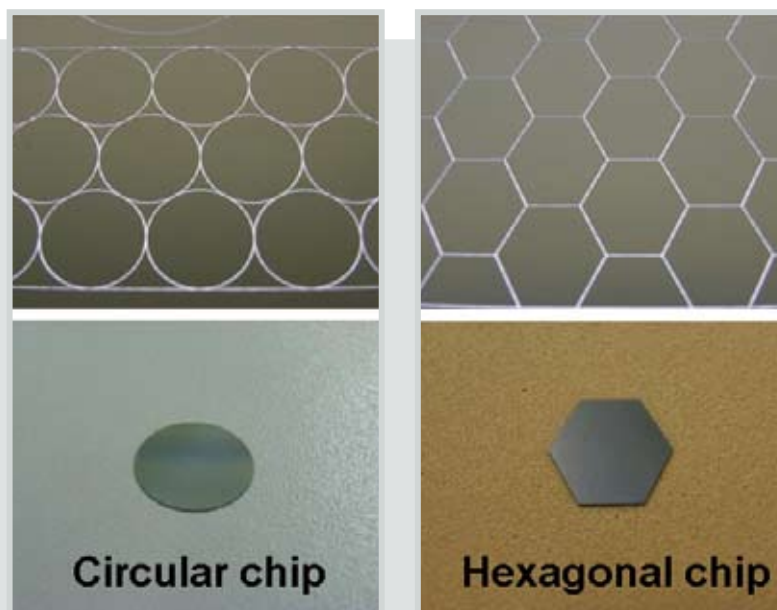


Figure 11: Various chip shapes realized by plasma dicing

PANASONIC'S PLASMA DICING EQUIPMENT

The plasma dicing equipment that Panasonic has developed is the PSX800. This equipment can not only be used for the plasma dicing process but also for plasma stress relief, O₂ plasma resist removal and plasma cleaning for wafer. Both 8 inch and 12 inch wafers are available and we have developed electrostatic chuck (ESC) electrode in order to lower the wafer surface temperature and avoid the heat damage to protective tape for back grinding. We have adopted inductively coupled plasma (ICP) source power to realize high density plasma for high speed etching.

CONCLUSION

The plasma dicing process has the advantages of "damage free", "chipping free", "particle free", "water free" and "heat free" over the conventional dicing processes. Therefore it can not only be applied for thin wafer dicing process but also for MEMS manufacturing process because MEMS has very fragile structures in it.

Mechanical blade dicing process has been most common and has an advantage in running cost. But it would not be the best solution for thin wafer.

Laser dicing may be a good alternative process in terms of physical dam-

age free to the low-k material. But it still could give heat damage to the chip resulting in low chip strength just like mechanical blade dicing.

The plasma dicing technology can realize highest chip strength and highest productivity especially for small chip. In addition it can be applied for thin wafer and make the chip shape freely and the dicing line width narrower.

The plasma dicing technology would be useful for 3D packages, brittle MEMS fabrication, the devices which include low-k material and RFID.

Strong Partners for Technology Leadership

Local Plasma Treatment in a Mask Aligner for Selective Wafer Surface Modification

Marko Eichler, Fraunhofer Institute for Surface Engineering and Thin Films IST

Markus Gabriel, SÜSS MicroTec

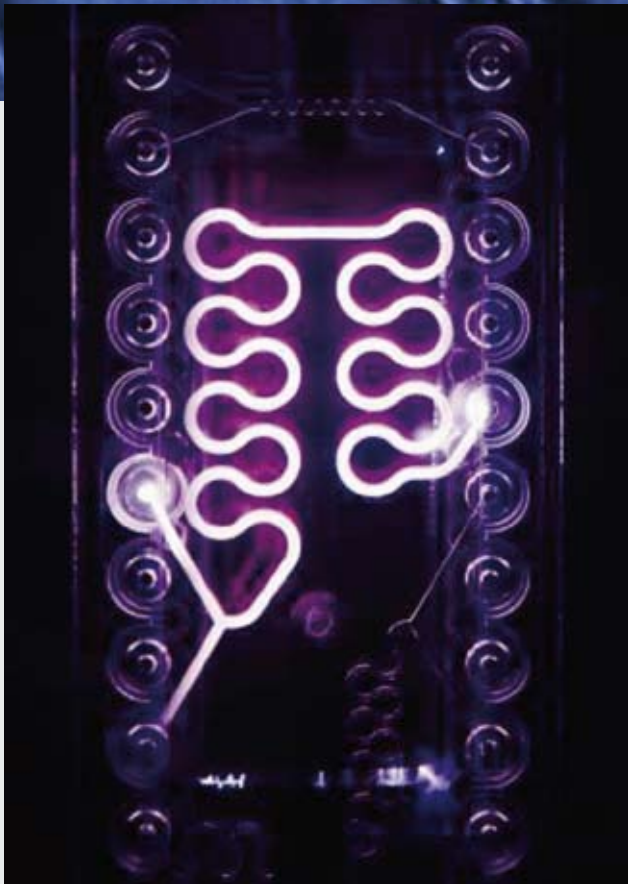


Figure 1: Microplasma in a microfluidic mixer channel structure [by courtesy of thinXXS Microtechnology AG]. Channel cross section is $640\ \mu\text{m} \times 640\ \mu\text{m}$. The discharge is seen through a transparent electrode.

The cooperation between SÜSS MicroTec and the Fraunhofer Institute for Surface Engineering and Thin Films (IST, located at Braunschweig in Lower Saxony, Northern Germany) on atmospheric-pressure plasma processes goes back to the end of 2002, when the first negotiations about details of future collaboration took place. A major series of experiments on low-temperature direct bonding of silicon wafers which beforehand had received a surface treatment by a so-called dielectric

barrier discharge (DBD) – i.e. a “cold” plasma discharge which can be run at atmospheric pressure - was conducted in early 2003. This study was so successful, that a few months later already concepts of an implementation of the DBD method into a commercial bonder were discussed in the Garching head-quarter of SÜSS.

IST is a Fraunhofer research institute specializing in R&D of thin film deposition and surface treatment processes utilizing plasmas. Generally these processes have to be performed at low pressures, typically 1 Pa, and require vacuum equipment. At IST many different kinds of thin films and deposition processes are available, together with an extensive infrastructure for thin film analysis and characterization. For about a decade a team of scientists and engineers at IST has also been evaluating the opportunities offered by applying DBD plasmas at ambient pressure to surface-technological processes such as coating, functionalization, cleaning, and etching - processes which are also of interest for MST applications.

One driving force behind these efforts is the desire or requirement to reduce process costs by making expensive vacuum equipment dispensable. In fact it was shown in many studies that atmospheric-pressure plasmas could be

applied to surface-technological purposes with similar or even better technical performance than low-pressure plasmas - activation of wafer surfaces prior to bonding is a good example.

For physical reasons there are some areas of applications where in the foreseeable future atmospheric-pressure plasmas will probably not be applicable, such as deposition of hard coatings – diamond-like carbon or cubic boron nitride - requiring energetic ion bombardment to attain the necessary properties. On the other hand this handicap is largely outweighed by the possibility of generating so called microplasmas, discharges in very small volumes, owing to the strongly reduced mean free path length; typically only 100 nm at 1 bar, compared with 1 cm at 1 Pa!

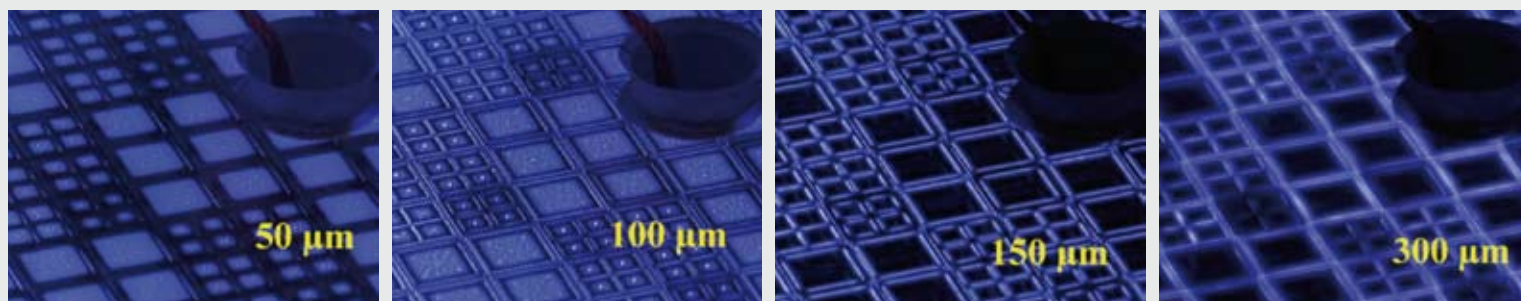
At IST the chances offered by this special property of atmospheric-pressure plasmas for several novel surface-technological processes were recognized quite early: Microplasmas open the ways to new surface patterning methods – plasma printing – which may be used, e.g., for polymer electronics, biochip manufacturing, and medical or solar applications. Roll-to-roll micropatterned plasma-pretreatment of polymer sheets prior to a fully-additive metallization process is presently the topic of a government-funded collaboration of IST with several industrial partners. Microplasmas can also be used for in-

side coating or surface modification of microfluidic channels used in labs-on-chips, see the microplasma in a microfluidic mixer channel in Figure 1 as an example. For MST applications, local plasma treatment (LPT) utilizing microplasmas is of special interest – the process was patented jointly by SUSS MicroTech and Fraunhofer IST and is presently being implemented in a novel mask aligner. Figure 2 shows localized discharges on the surface of a structured Si wafer.

With its focus on atmospheric-pressure plasma-based surface pretreatment for bonding of various materials and on utilization of microplasmas for surface technology the IST group – presently 13 scientists and engineers – has a unique position among R&D groups active on plasma technology. This research capacity is reinforced by several scientists at the neighbouring Institut für Oberflächentechnik (IOT) of the Technische Universität Braunschweig, working on fundamental aspects of plasma-based microproduction technologies.

Taken together, the IST and IOT research groups form a very potent R&D resource both for application-oriented as well as fundamental surface-technological problems to be solved by atmospheric-pressure plasmas and microplasmas.

Figure 2: Local plasma treatment (LPT) of a structured silicon wafer surface. The photographs were taken with different distances between the Si wafer and a transparent counter electrode (ITO on glass), as indicated on the photographs. At low distances, the discharge is limited to the recessed areas of the wafer, at large distances it is concentrated on the protruding ridges of the structure.



Plasma pre-treatment for low-temperature direct wafer bonding is used worldwide in many different applications. In this process the full wafer surface is exposed to the plasma. Recently, a new process for selective plasma treatment has been developed by the Fraunhofer IST and SUSS MicroTec. Micrometer-scale selective area activation and functional layer deposition are the advantages of the process which provide new design and manufacturing options for MEMS/MST applications. The technical realisation is solved by a thin planar electrode in a mask aligner assembly. The plasma process takes less than one minute for all wafer sizes and all relevant mechanical precision parameters of an aligner appear. SUSS MicroTec is about to develop the patented process to industrial maturity and to integrate »Plasma Tooling« into new and used aligners of SUSS as an upgrade kit. The process and the equipment are presented in this paper.

1. Unstructured Plasma Treatment, State of Technology

Plasma treatments are standard applications that are used in the semiconductor industry in many different ways, e.g. for layer deposition, cleaning or etching. Just recently, plasma treatments were more and more employed for plasma surface activation in various MEMS applications. Most of these technologies are based on high frequency low-pressure plasma processes. As an alternative, the ambient pressure plasma treatment can be used. It requires lower investment costs and offers shorter processing times^[1,2,4]. SUSS MicroTec offers plasma systems for both treatments.

Typically silicon or other semiconductor wafers, as well as glass wafers are treated with plasma in order to activate the surface. This step prepares for the subsequent direct wafer bonding, in order to accelerate the con-

densation of silanol groups in the bond interface during annealing at moderate and CMOS compatible temperatures. Without plasma pre-treatment bonded silicon wafers would typically need to be annealed at 1100 °C. When activated with plasma the temperature can be lowered down to 400 °C, without compromising the stability of the bond.

In commonly known plasma activation processes the whole wafer area is exposed to the plasma. That is not always necessary. In some cases it can even affect or damage the functionality of the micro components or the electronics.

Figure 3: Different methods of plasma activation
a) full area, b) selective via structured electrode, c) selective on upper level of substrate, d) selective in cavities / trenches of the substrate.

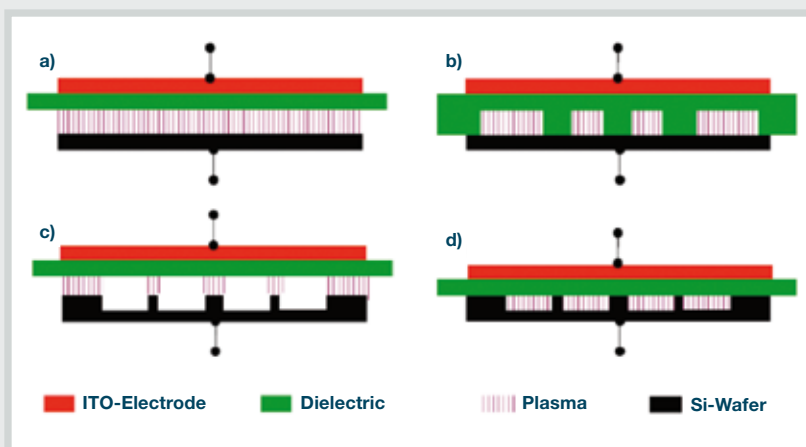


Figure 4: Selective plasma discharge leads to local modification of the surface properties.

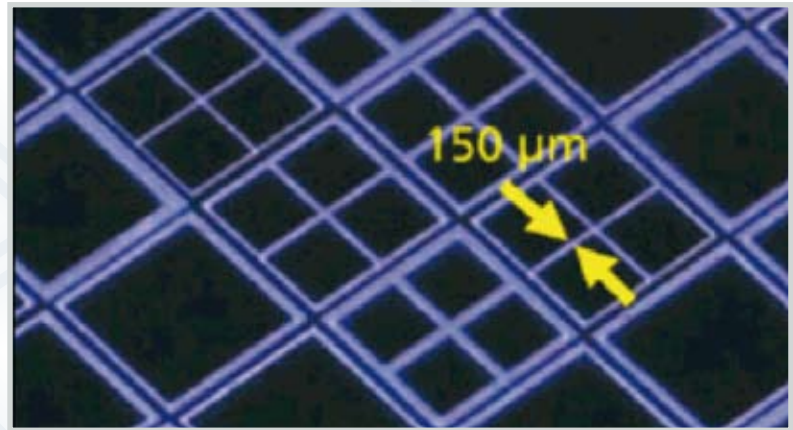
2. Local Plasma Treatment for Selective Wafer Surface Modification

2.1. Goal of Selective Wafer Surface Modification

In order to enable a selective surface treatment in addition to the full area (unstructured) approach, Fraunhofer IST has now developed a new method for plasma activation at ambient pressure [3, 4, 5]. It provides new design and fabrication possibilities, for example in microfluidic applications, where two or more substrates are supposed to be bonded, in order to develop a functioning chip, in a second step. For simultaneous realization of hydrophilic bond surfaces and hydrophobic channel surfaces the bond surfaces are locally pre-treated in a different way than the micro-channel surfaces.

2.2 Local Plasma Treatment

The application described in this paper is based on the principle of dielectric barrier discharges. For a uniform plasma discharge two electrodes are needed. At least one on them needs to be covered by a dielectric of an adequate thickness leaving a small gas gap between the insulator surface and the counter electrode. The application of an AC voltage in the range of 20 kHz and 5-10 kV leads to a gas discharge which, dependent on the conditions, may be uniform or consist of thousands of microscopically small filaments. One method of barrier discharge that has already been used for wafer treatment is characterized by two bar-shaped electrodes with an electric po-



tential between them. During treatment chuck and wafer are positioned on ground potential, so that the discharge can be ignited between the electrodes and on the wafer. During plasma scanning of the wafer with the electrodes, the whole wafer area gets exposed to the plasma [1, 2].

However, the new treatment employs a thin, planar electrode, which covers the whole wafer. This new electrode is made of a glass wafer coated with a transparent, conductive layer on the backside. It is now possible to monitor the discharge during treatment. When the planar electrode is adjusted in a small gap opposite to the wafer, it becomes possible to ignite the plasma at an ambient pressure through application of an adequate AC voltage.

How is it possible to treat the wafer just selectively with the plasma?

Therefore, two new treatment methods were developed and will now be described. The first method has been developed for local treatment of wafers with high topography, which can often

be found in MEMS/ST applications. When the electrode is adjusted above a wafer with high topography variations, electric fields are generated between the wafer surface and the electrode that show different strengths in the lower and higher areas of the wafer.

When wafer and electrode are brought into contact, the plasma ignites in the cavities (Figure 3a) and in larger gaps it flashes on the elevated structures (Figure 3c). This means that the already existing structures or topography of a wafer, the electrode gap and the electrode voltage are crucial factors for the final location of the plasma ignition. In this set-up a wafer without topography would get a full surface (unstructured) treatment, as shown in Figure 3a.

The second variation of the new treatment has been specially designed for substrates without topography that still need to be treated selectively. Local cavities of the structured electrode are used to limit the formation of plasma to those surface areas that need to be treated (Figure 3b). This effect can be additionally supported by local metallization or other structured dielectrics.

Figure 4 shows a snapshot of a process detail from top view during a selective plasma discharge (light areas). A process observation was possible, as for the treatment an electrode coated with a transparent, conductive ITO layer was used. In this application nitrogen was used as process gas.

Figure 5 shows the same wafer detail after treatment. The test with DI water clearly shows changes in the surface tension of the wafer that was made

Figure 5: Local hydrophilization (visualized through wetting with DI water).

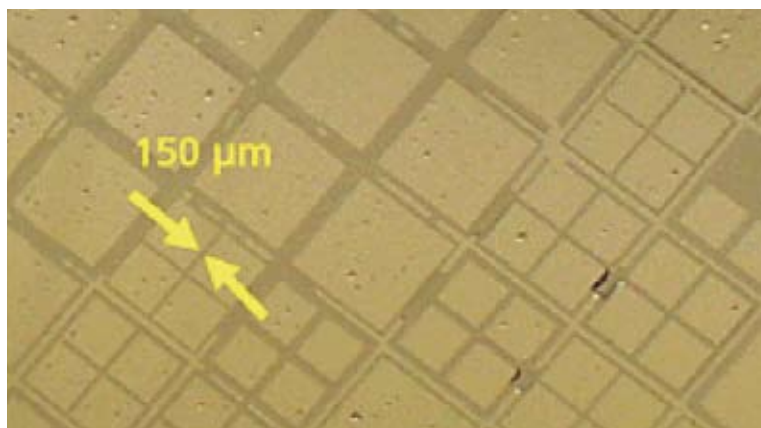




Figure 6:
MA/BA6 Mask
and Bond Aligner
from SUSS MicroTec.

hydrophobic by an HF dip beforehand. Water adheres to those areas that had been treated with plasma, while those that had not been pre-treated remain water-repellent.

3. Local Plasma Treatment – Integration in Mask Aligner

SUSS MicroTec has already started to integrate Local Plasma Treatment into its equipment. The first question that had to be answered was: Do we need to design a completely new system or can we adapt it to already existing technologies? Between substrate and electrode a process alignment is needed. However, the decision was easy - the SUSS Aligner (Figure 6) is the systems of choice. Besides, the standard UV-Lithography SUSS MicroTec Aligners can be easily upgraded with additional functions like bond alignment or nano-imprinting.

In order to be able to employ the bond aligner for the new treatment the following prerequisites need to be fulfilled:

- A dedicated device to integrate a planar electrode and wafer in a parallel set-up
- A mechanism to compensate the wedge error (WEC) between the electrode and the wafer
- Lateral, micrometer precise alignment between electrode and wafer
- Reproducible, micrometer precise gap setting between electrode and wafer

All of these prerequisites are already available in a standard SUSS Aligner. Process relevant modifications refer mainly to the newly designed and exchangeable device for plasma treatment (plasma tooling) and the control software, in order to guarantee the correct process flow.

The relatively high electrode voltage is seen as a critical aspect of integration that affects operator and machine safety. Furthermore, appropriate design set-up, safety inquiries during operation and additional arrangements are concerned. For the process itself the reproducible settings of the electric field between substrate and electrode are crucial and make sure that the discharge really ignites on those areas that are intended to be treated.

The process has to be applicable for conductive, semi conductive as well as for non conductive substrates. In addition the electrode holder and the wafer chuck of the plasma tooling are forming a closed process chamber (mini environment) that enables precise monitoring of the gas atmosphere in the discharge area. Upon applying two process gases at ambient pressure or minor low-pressure, a defined and reproducible process atmosphere is created.

In this process significantly reduced process gases are consumed - compared to existing plasma systems - because of the combination of a relatively small gap between substrate and electrode and the formation of a closed process chamber. Purging gas cycles before and after the plasma process make sure that the operator does not get in touch with the process gas or process gases such as ozone, that can be generated during plasma discharge. The planar and exchangeable electrode is loaded through the loading slide of the MA/BA8 Aligner and transferred automatically to the electrode holder (equivalent to mask holder). The reversible electric contacting of the high voltage electrode as well the electrical isolation of the wafer chuck represents

a challenge. During the concept phase of this serious question SUSS MicroTec was supported by Fraunhofer IST with its specific process know-how.

The integration of the new »Plasma Tooling« into the SUSS MicroTec aligner was designed for new and for used machines, that can be retrofitted with the plasma toolkit and opens owners of used SUSS Aligners an easy and cost-efficient way to new plasma treatment. The first system will be installed at Fraunhofer IST in Braunschweig, Germany by the end of the first quarter in 2010.

ACKNOWLEDGEMENTS

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MARKO EICHLER

went through vocational training as a certified measure and control technician. Subsequently he studied physics at the Technical University of Braunschweig, where he also received his Diploma. Since 2000 he is research associate in the Atmospheric-Pressure Processes department of the Fraunhofer IST. Presently he is focusing on low-temperature wafer bonding and surface modifications by micro plasmas, the topics of his PhD thesis research.



MARKUS GABRIEL

is product specialist for new wafer bonding business like the temp. bonding and debonding for 3D integration. He has been working for more than 10 years with Suss MicroTec in Germany and USA on various position. He is member of the SEMI Europe committee on MEMS.



In the Spotlight

LED Production on the New SUSS MA100e Mask Aligner

Light emitting diodes (LEDs) are increasingly used in many lighting products covering not only the visible spectrum but also ultraviolet and infrared applications. To replace conventional light bulbs the costs for the production of LEDs must be low. Historically, the semiconductor industry has relied on increasing the diameter of silicon wafers in order to push productivity and lower cost. LEDs, however, are made from compound semiconductors rather than from silicon. And while red LEDs can already be manufactured on 150mm GaAs wafers other compound semiconductor substrates for technical reasons are still limited to a wafer diameter of 2, 3 or 4 inches. Therefore, the demand for increased productivity and lower cost needs to be met by dedicated equipment that combines highest throughput with the ability to meet the particular technological requirements and cost constraints of the LED industry.

These requirements can be met by the new MA100e Mask Aligner. On the basis of the well established MA150e, the MA100e was optimized for small wafer sizes up to 4 inch and is equipped with a special high throughput upgrade, including a new pre-aligner, especially designed for transparent wafers. With the high throughput upgrade on the MA100e, up to 140 wafers per hour can

be exposed in auto alignment mode. For LEDs in the short wavelength range (green, blue, ultraviolet) the commonly used materials are group III – nitrides. As GaN substrates are still very expen-

sive, the GaN layers are grown on less expensive sapphire wafers. In contrast to conventional silicon IC technology sapphire substrates as well as the functional layers of the LED are transparent





Figure 1: Microscope image of an alignment target on a GaN-Wafer. The contrast between the target cross and the background is very poor.

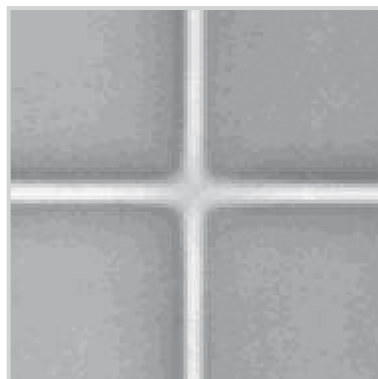


Figure 2: Image of the alignment target on the screen of the MA100e. The contrast is good enough for training and auto alignment.

to visible light. Even electrical contact layers such as indium tin oxide (ITO) are transparent. Thus the contrast of micro structures (e.g. alignment keys) on the patterned wafer is typically very poor and therefore challenging for the alignment system. In order to increase the efficiency of LEDs the wafer is often textured (roughened) before depositing the functional layers adding another challenge to the pattern recognition system. The surface roughness causes light scattering and diffuses the image of the alignment target (see Figure 1).

The alignment microscope and camera system of the MA100e in combination with its advanced alignment software, however, can cope with this challenge. Figure 2 shows the image of the alignment target when using the SUSS MA100e. Obviously, it offers much better contrast than the image obtained from a standard optical microscope. Generally, pattern recognition and alignment is no problem with the MA100e and targets are found even if the surface background changes on each wafer. For these challenging targets, however, careful target training is essential.

Due to the crystal lattice differences of sapphire and GaN, these wafers often tend to exhibit a dome-like warpage caused by strain. With the special

warped-wafer-handling system of the MA100e, such wafers can be handled efficiently and reliably.

Resolution requirements are still fairly relaxed compared to standard IC technology. Lift-off processes are common because the quantum efficiency of LEDs is sensitive to the condition of the wafer surface. However, new types of photoresists such as the DNR-L300 series from Dongjin Semichem Inc. (South Korea) are increasingly used. The DNR-L300 is a negative acting chemically amplified resist. The advantages of this material are that it is developed in common aqueous base developers and is easy to strip/lift-off with organic solvents. As a chemically amplified resist it delivers straight sidewalls even when exposed in larger proximity gaps.

In the following example the DNR-L300 resist was coated on 2-inch sapphire wafers using the manual SUSS Delta80 Coater. The mean layer thickness was $2.95\mu\text{m} \pm 1.16\%$ (1s). The MA100e was equipped with UV400 High Resolution Optics and a 1000W mercury lamp. The achieved resolution of lines and spaces depends slightly on the wafer surface and the evenness of the top epitaxial layer (Table 1). The surface of a deposited GaN layer is not as even as that of a

Contact mode	Lines and spaces resolution
Proximity 20µm	≤ 3.5µm
Soft contact	≤ 3.0µm
Hard contact	≤ 2.5µm
Vacuum contact	≤ 2.0µm

Table 1: Resolution of MA100e in 3µm thick negative tone DNR-L300 resist. The given resolution refers to the resolution limit on the most challenging surface.

THE AUTHOR:



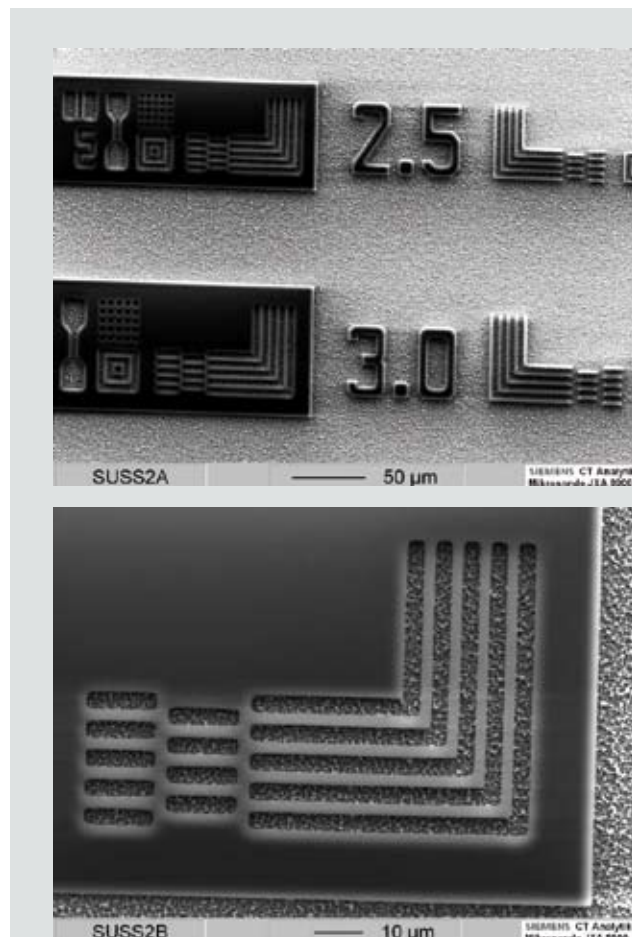
Barbara L'huillier

Barbara L'huillier joined SUSS MicroTec as application engineer for mask aligners in October 2006.

In 2009 her field of activity was extended by spin coaters. She received her diploma in electrical engineering from Ulm University, Germany, in 2002 and her PhD degree from Ulm University in 2008, working with GaN light-emitting diode structures on semipolar crystal planes.

silicon or GaAs wafer (see Figure 3). The exposure optics of many low-cost aligner feature only a resolution limit of about 5µm with this resist. The MA100e, therefore, features superior exposure results than competing equipment and can cope with all lithography challenges given by the LED manufacturing process.

Figure 3: Electron microscope images of 2.5µm and 3µm lines and spaces in a 3µm thick layer of Donjin DNR-L300 D1 negative tone resist.



Metal Based Wafer Bonding Techniques for Wafer Level Packaging

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DR. SHARI FARRENS

As chief scientist for the SUSS Micro-Tec Bonder Division Dr. Farrens has authored and co-authored over 100 publications on SOI, wafer bonding and nanotechnology. With over 15 years of hands-on experience in academia and industry she is worldwide considered an expert on MEMS and wafer-to-wafer bonding technologies.

Her most recent paper Metal Based Wafer Bonding Techniques for Wafer-Level Packaging was awarded Best Practises Paper by MIG (MEMS Industry Group) as part of the effort to provide varied perspectives on the successful practices of fellow MIG members.



SCOPE OF THE PRACTICE

This BKP (Best Known Practice) describes the necessary conditions required to successfully utilize metal based wafer bonding techniques, including diffusion and eutectic bonding, for wafer level packaging.

PROBLEM STATEMENT AND GOALS OF THE BEST PRACTICE

Wafer level bonding utilizing metal based technologies are coming to the forefront of manufacturing methods in numerous 3D integration schemes and advanced MEMS processing. Copper to copper bonding of TSVs (through silicon vias) is used for 3D IC stacking of individual layers as well as in 3D packaging operations. A primary differentiator is the via size and therefore the placement accuracy needed to obtain production yields. Meanwhile gold and aluminum diffusion bonding and numerous eutectic alloys are replacing traditional MEMS glass based bonding methods and allow for higher degrees of hermeticity. The increased hermeticity enables device scaling and vertical packaging options that dramatically reduce production costs. This document describes the necessary conditions for these metal based bonding processes.

GENERAL DESCRIPTION OF APPROACH/STRATEGY

Types of Metal Bonds:

There are two broad categories of wafer level bonds using metals. Diffusion bonds using copper to copper are very popular for 3D integration using TSV fabrication scenarios. In MEMS device packaging, gold and aluminum diffusion bonding methods are more common. The second category of metal bonding technologies includes a variety of metal alloying methods called eutectics. The eutectic is a specific alloy composition that changes directly from solid to liquid

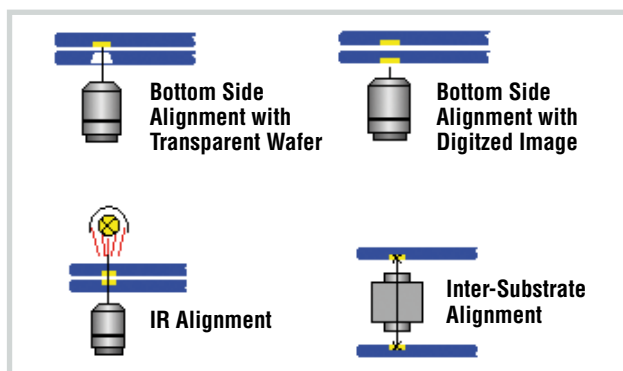
at a unique triple point in the phase diagram. The transition to a liquid phase provides a viscous interface that can self-planarize over surface topography and particles. The metal bonds provide several advantages over other bonding methods. These include provisions for electrical interconnects, higher levels of hermeticity, and device scaling.

Alignment Strategies and Methods:

Alignment accuracy is affected by the quality of the alignment keys, the method of imaging used during wafer to wafer alignment and the thermal response of the wafers during heating and bonding. Alignment with metal bonding technologies is facilitated by the high levels of contrast that can be achieved with both optical and IR (infrared) imaging of metal fiducials on the semiconducting substrate materials. There are four fundamental types of alignment used in wafer bonding. They are TSA, (top side alignment), BSA (bottom side alignment), IR (infrared alignment), and ISA (intersubstrate alignment or face-to-face). The positioning of the wafers with respect to the objectives is shown in Figure 1.

The BSA alignment methods have matured over several decades and are used extensively with anodic and glass frit bonding techniques. BSA alignment works equally well with all types of metal bonding assuming that one of the wafers includes backside targets that are clearly imaged on the polished or unpolished surface. Increased levels of overlay accuracy often benefit from more precise IR and ISA techniques.

Figure 1:
Four basic alignment methods used in wafer level bonding.



The IR or the ISA alignment methods both use alignment marks at the bond interface and therefore eliminate differences in focal plane depth and front to backside registration.

The advantage of IR imaging lies in the ability to observe both sets of alignment marks simultaneously and in principle maintain image information via live acquisition during the process of bringing the wafers into contact. Figure 2 shows the basic IR imaging concept. Limits to the IR method include double side polishing requirements on at least one of the wafers, limited dopant range, and metal free windows surrounding the fiducial locations. The backside polishing requirement is because light scattering from the backside roughness on standard wafers reduces the brightness and image quality of the alignment key at the camera.

IR absorption also limits the light reaching the imaging system. For silicon substrates, the substrate resistivity must be >0.01 Ohm-cm unless the wafers are sufficiently thin to ensure sufficient brightness. Naturally the area around the alignment keys must be metal free since the metal layers are 100% absorbing. For samples in which the substrates are not transparent to IR radiation or backside polishing is not an option, face-to-face alignment is needed. Figure 3 shows an example in which the front side marks on both wafers are aligned using ISA mode by inserting a thin camera between the substrates and imaging the alignment keys. Once aligned, the camera is retracted and the wafers are contacted. This technique is popular with compound semiconductor substrates that are opaque to IR radiation, power devices built on highly doped substrates, or device wafers with extensive layers of metal that occlude IR transmission. Most 3D applications use intersubstrate alignment because metal layer obstruction is extensive in substrates with several thousands to millions of copper vias and multiple metal interconnect layers. The selection of the alignment keys is equally important and recommendations exist for each of the types of bonds and alignment methods discussed here. These are further subdivided depend-

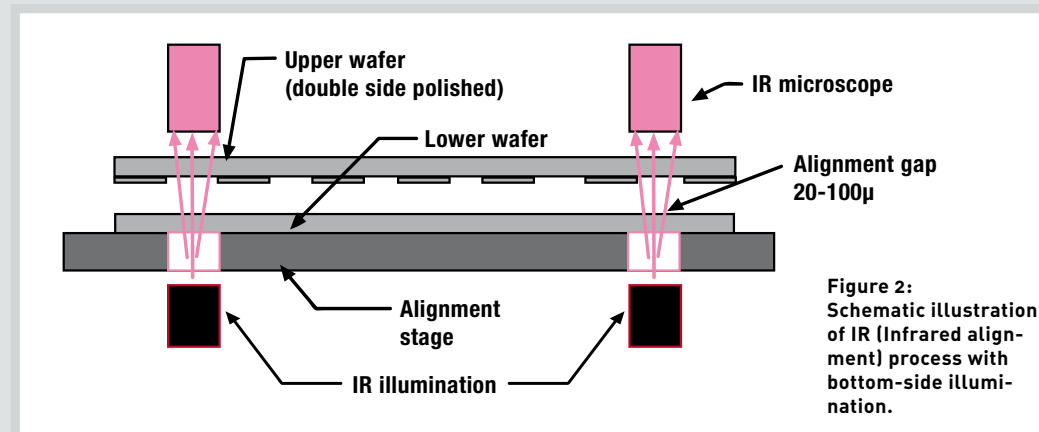


Figure 2: Schematic illustration of IR (Infrared alignment) process with bottom-side illumination.

ing upon if a human will be doing the alignment on manual systems or if an automated system is used with pattern recognition. Please refer to reference 1 for additional details.

Alignment Requirements:

Overlay/alignment accuracy is determined by several requirements. Most specifications arise from architectural design rules that will determine how accurately the upper wafers must align to the circuits or components on the lower wafer. Next are the requirements for adequate sealing and electrical connections. For a sealing ring surrounding the device it is often required that the width of the sealing ring align to within 80% of the opposing feature. This means only 20% of the width may misalign on either side. Thus, for a 100 micron wide sealing ring the offset on each side could be as much as 10 microns and the device and hermeticity needs would be satisfied.

Equipment:

The sensitivity of the metal bonds to uniform temperature and force has led to improvements in wafer level bonding equipment. Improvements in materials and design for bonders such as the

SUSS MicroTec CB8 (or CB200 and CB300 in 200mm and 300mm cluster tools) and have led to temperature uniformity levels with $<1\%$ difference within wafer or between upper and lower heaters. The force uniformity in advanced bonders is now 5% and results from the fact that in these bonders the upper and lower pressure plates establish parallelism by a WEC (wedge error compensation) operation before bonding.

DETAILED STEPS/ ACTIVITIES FOR PRACTICE IMPLEMENTATION

Diffusion Bonding:

Diffusion bonding is when two metals are pressed together under applied force and heat causing atoms to migrate from lattice site to lattice site “stitching” the interface together. Diffusion processes require intimate contact between the surfaces since the atomic motion is driven by lattice vibration. Copper, gold, and aluminum are the most commonly used metals in 3D integration and MEMS packaging.

Table 1 compares the recommended processing ranges for the three lead-

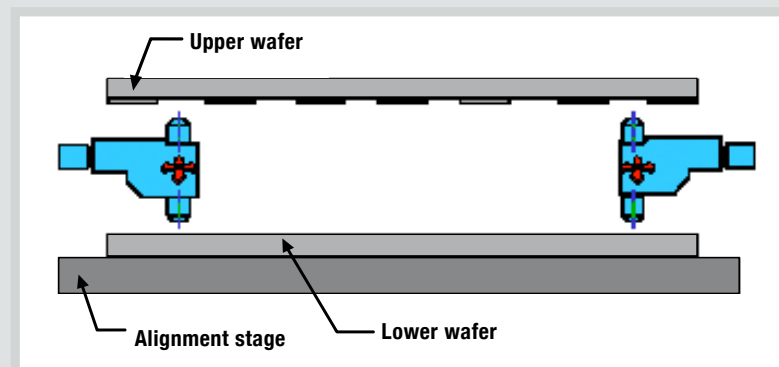


Figure 3: Schematic illustration of the ISA (intersubstrate alignment) configuration. ISA Alignment utilizes dual imaging objectives on both the left and right alignment optics.

Metal	Temperature	Applied Force Range*	Time	Atmosphere
Al	400 - 450° C	> 70 KN	20 - 45 min	Vac or H ₂ /N ₂
Au	300 - 450° C	> 40 KN	20 - 45 min	Vac or H ₂ /N ₂
Cu	380 - 450° C	> 30 KN	20 - 60 min	Vac or H ₂ /N ₂

Table 1:
Typical processing parameters for metal diffusion bonding.

* Applied force depends on wafer diameter and pattern density. Table values are representative of 200mm blanket layer wafers.

ing metal diffusion bonding techniques. Aluminum bonding is generally not pure aluminum but rather the metallization alloys used in the fab which includes up to 4% Cu or other binary additions. Both aluminum and copper bonding require temperatures above 400°C to achieve a good hermetically sealed interface. Aluminum also requires a large applied force which is apparently needed to crack the surface oxide which spontaneously forms on any aluminum surface. The surface oxide of aluminum is not soluble in the matrix (<2e-8 wt %) and tracer studies have proven that aluminum does not penetrate the oxide.^[2-3]

Gold diffusion is the lowest temperature process of the three metal diffusion choices and is successfully managed at temperatures as low as 300°C. Unlike copper and aluminum, gold does

not readily form an oxide and under normal processing conditions it is not necessary to use surface cleaning prior to bonding. It is recommended that all metal bonds use either a vacuum bonding atmosphere or forming gas (H₂/N₂ for example) environment during the thermal cycles.

Copper on the other hand, readily forms a surface oxide. The oxide can be successfully removed and the surface passivated by the use of formic acid vapor cleaning. Vapor cleaning with formic acid is used in 3D vertical integration to ensure high conductivity of interconnects.^[4]

Eutectic Bonding:

The other major category of metal based bonding used in wafer level packaging is the eutectic bond. A eutectic alloy is sometimes called a "solder" however,

Choosing the correct eutectic alloy for an application is most often determined by the processing temperature and compatibility of the materials with the existing manufacturing flow. In addition to alloy selection, it is equally important to determine the method of eutectic alloy formation.

The eutectic bond can be achieved by melting the alloy or by a combination of diffusing pure materials together in the solid state to reach the eutectic composition and then melting the alloy.

When the alloy can be deposited as a compound layer on both sides of the interface, the wafers are simply aligned, brought into contact and pressed together. After contact is established the wafers are heated slightly above the eutectic temperature, melted, and re-solidified. Alloys can be deposited by sputtering of alloy targets and sometimes by dual component electroplating. The advantage of the direct melting of alloy layers is speed because the diffusion step can be avoided.

Alternatively, the pure materials that constitute the alloy can be deposited separately on each substrate. Then the wafers are pressed together and heated below the eutectic temperature until the interface mixes to form a solid solution layer via diffusion. Note that limited solid solubility means that the diffusion is typically only a few percent and grain boundary reactions will play a major role in the success or failure of the bonds when completed with this strategy. After mixing the material, the wafers are heated above the eutectic melting temperature under reduced force, reflowed, and cooled.

Table 2:
Eutectic alloys commonly used in Wafer level packaging. (WLP)

Eutectic Alloy	Eutectic Composition	Eutectic Temp.
Al-Ge	49/51 wt%	419°C
Alu-Ge	28/72 wt%	361°C
Au-In	0.6/99.4 wt%	156°C
Au-Si	97.1/2.9 wt%	363°C
Au-Sn	80/20 wt%	280°C
Cu-Sn	5/95 wt%	231°C

Table 3:
IR aligned fusion bond overlay accuracy.

Wafer #	Alignment in μm	Wafer #	Alignment in μm
1	0.1701	13	0.0484
2	0.0736	14	0.1008
3	0.1648	15	0.1326
4	0.0967	16	0.1898
5	0.1586	17	0.0793
6	0.0353	18	0.1195
7	0.1139	19	0.1088
8	0.0730	20	0.0725
9	0.0941	21	0.1280
10	0.0899	22	0.0951
11	0.1264	23	0.1258
12	0.0649	24	0.1165
Average	0.1088	Max	0.4385
St Dev	0.0428	Min	0.0190

this is not precisely the correct metallurgical term. A eutectic alloy is a two component alloy that undergoes a direct solid to liquid phase transition at a specific composition and temperature. The composition and temperature define the reaction and this type of phase change is unique to only a few materials systems. Table 2 shows the eutectic alloys most often used for wafer level bonding. The choices are alloys of gold, aluminum, or copper since these materials are already used in semiconductor fabrication labs and in most cases have established processing and deposition methods. The most common choice is the gold/tin system with interest in other alloys fairly evenly distributed.

Alignment Shift X-axis and Y-axis in Three Locations								
X1	Y1	X2	Y2	X3	Y3	X misalign (μm)	Y misalign (μm)	
-0.03	0.02	-0.08	0.07	-0.10	0.10	1.25	1.85	
-0.03	0.02	-0.08	0.07	-0.10	0.10	0.80	0.90	
-0.03	0.02	-0.08	0.07	-0.10	0.10	0.50	-1.75	
-0.03	0.02	-0.08	0.07	-0.10	0.10	0.96	-1.05	
-0.03	0.02	-0.08	0.07	-0.10	0.10	1.70	-2.15	
-0.03	0.02	-0.08	0.07	-0.10	0.10	1.85	-2.40	
-0.03	0.03	-0.08	0.08	-0.10	0.10	1.60	2.25	
-0.03	0.03	-0.07	0.07	-0.10	0.10	-1.20	0.30	
-0.03	0.02	-0.08	0.07	-0.10	0.10	0.56	-1.75	
Average	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.89	-1.03

Table 4:
Post bond alignment accuracy. Average alignment shift ~1μm.

Results:

The three leading wafer level bonding techniques used in 3D integration are the fusion bond, copper to copper diffusion bonding and to a lesser extent the BCB bond. The fusion bond affords the highest potential for submicron alignment because the initial bonds are performed at room temperature in an aligner and tend to experience less thermal induced shifts when annealed in batch to create the permanent bonds. Table 3 shows an example of a fusion bond using IR alignment techniques that achieve deep submicron alignment accuracy.

Metal diffusion processes can make it more difficult to control thermal expansion differences between upper and lower wafers. Using precision alignment, quality fixtures, and state of the art bonding equipment, excellent alignment results can be obtained for 3D devices utilizing Cu-Cu TSV technology and also for Au-Au bonding of hermetically sealed MEMS devices. Tables 4 and 5 show recent results of both types of metal diffusion bonds.

The newest technique to emerge from R&D to manufacturing are the aluminum based bonding methods for hermetic packaging. Shown in Figure 4 are examples of a 150mm MEMS wafer bonded with the aluminum diffusion process. Also shown is a 200mm wafer bonded with a blanket layer of aluminum resulting in a void free interface. Both bonds were done on the SUSS MicroTec CB8 advanced bonder.

CONCLUSION AND RECOMMENDATIONS

Wafer level bonding has a long history in the production MEMS devices such as accelerometers, pressure sensors, and gyroscopes. As these products have matured, their scaled down cousins are entering consumer markets for gaming and mobile communications. Wafer level bonding with metal based technologies is meeting the demands of these products while presenting attractive cost models. The utilization of metal bonds to realize vertically integrated devices and facilitate wafer level packaging with smaller form factors appears to be coming to market in 2009. Image sensors and stacked memory will test the manufacturability of these methods in production in the coming years. Successful implementation will drive further advancements in CPU and logic integration as well as heterogeneous integration. New state of the art alignment and bonding production equipment will be key to the success of these evolutionary advances in semiconductor processing.

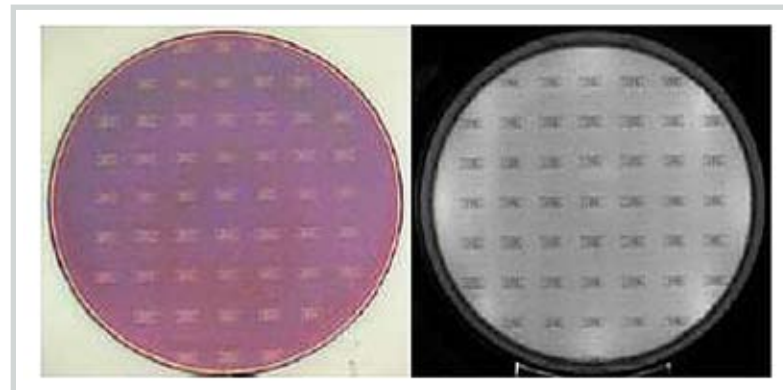


Figure 4:
Optical image (left)
and IR image of BCB
bonded image sensor
wafer. No voids visible.

Sample #	POST BOND ALIGNMENT DATA				
	LX	LY	RX	RY	ACC POST
1.0	-3.0	0.0	-1.5	0.0	2.3
2.0	-0.5	-2.0	0.0	2.0	2.0
3.0	-3.5	-0.5	1.5	0.0	1.1
4.0	0.0	0.5	0.0	0.5	0.5
5.0	-1.0	-1.0	-0.5	-1.0	1.3
6.0	-0.5	0.0	0.0	0.0	0.3
7.0	0.0	-2.0	-0.5	0.0	2.0
8.0	-0.5	-2.0	-0.5	2.0	2.1
9.0	0.0	0.0	-0.5	-2.0	2.0
10.0	0.0	-1.5	-0.5	0.0	1.5
Max	0.0	0.5	1.5	2.0	2.3
Min	-3.5	-2.0	-1.5	-2.0	0.3
Avg	-0.9	-0.9	-0.3	0.2	1.5
St Dev	1.3	1.0	0.8	1.2	0.7

Table 5:
Copper to copper
200mm post bond
alignment results
using ISA alignment
methods.

Additional process are already evolving which combine techniques of advanced CMP (chemical, mechanical polishing) and bonding to realize Cu/Oxide, Cu/BCB and other hybridized bonding techniques. Like the microprocessor roadmaps, wafer bonding roadmaps continually seek to increase throughput and alignment accuracy while reducing production costs. This requires optimization of equipment, process flows, and materials science.

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Plasma Assisted Low Temperature Silicon to Glass Direct Bonding as an Alternative to Anodic Bonding

INTRODUCTION

Glass has continuously been attractive to MEMS and medical device applications because of its high insulation, easy workability and excellent transparent behavior. In the last few years, glass as a wafer bonding substrate has also made it to the CMOS Image sensor market. However most of existing methods for glass bonding (anodic, adhesive) are not suitable for packaging advanced MEMS devices. For example, anodic bonding is a popular bonding(1) method often utilized for MEMS packaging

in which the glass wafers are heated to a temperature of 300-500°C under high electric

field. The use of high electric field during bonding limits the use of anodic bonding. The issue of electrical compatibility of anodic bonding is especially critical if anodic bonding is to be applicable to monolithically integrated MEMS (structure and active devices on Si wafer) devices whose characteristics could considerably deteriorate following the bond process. Anodic wafer bonding process typically takes about 20-40 minutes per bond. For the integration of multi-functional MEMS devices especially in

advanced micro fluidic MEMS applications, it is necessary to reduce the processing

temperature for wafer level packaging. Another driving factor towards a low temperature process for Si to glass bonding is the CTE mismatch between Si and glass substrates. Even though glass substrates that closely match the Si CTE have been developed, high temperature bonding (>350°C) can still induce some thermo-mechanical stresses between the two substrates leading to bow/warp in the bonded pair. In addition, high throughput production of such devices requires a fast bond process. Plasma assisted direct bonding of Silicon to glass provides a low temperature (<300°C), high throughput alternative to anodic bonding. The two wafers are plasma activated and bonded at room temperature followed by batch anneal.

The feasibility of silicon to glass direct bonding is mainly determined by the cleanliness, waviness and smoothness of the wafer surfaces. Some of the important wafer surface parameters that need to be considered for direct bonding of wafers include roughness (usually RMS roughness or mean roughness), TTV, TIR, bow and warp. Wafer surface micro-roughness values are critical for direct bonding in which near atomic registration of the surfaces is necessary. Surface micro-roughness measurements performed on an area of a wafer that is typically a 1µm x 1µm to 5µm x 5µm area using atomic force microscopy (AFM) can provide information on whether the surface is suited for direct bonding. The RMS roughness value for wafers to be direct bonded should be ≤2nm.

Figure 1: SUSS PL300 vacuum plasma activation system and SUSS CL8 cleaner/bonder was used for Si-glass activation and bonding



Plasma Treatment using PL300



Cleaning and Bonding using CL8

Substrate 1	Substrate 2	Substrate Diameter	Process	Bond Propagation Time
Si	Schott AF32, Alkali free glass (700µm)	8"	No Plasma activation, DI rinse only	15-30seconds
			O ₂ Plasma on both wafers	< 8 seconds
Si/SiO ₂	Corning Pyrex 7740 (700µm)	8"	No Plasma activation, DI rinse only	20-60 seconds
			PL300 O ₂ Plasma on both wafers	<8 seconds
Si/SiO ₂	Schott Borofloat 33 (700µm)	8"	No Plasma activation, DI rinse only	20-60 seconds
			O ₂ Plasma on both wafers	<10 seconds
Si/SiO ₂	Corning AMLCD 1737 (1.2 mm)	8"	No Plasma activation, DI rinse only	90-360 seconds
			O ₂ Plasma on both wafers	<10 seconds

Table 1: Comparison of Bond Propagation speeds for various Silicon to glass bond combinations with and without O₂ plasma treatment

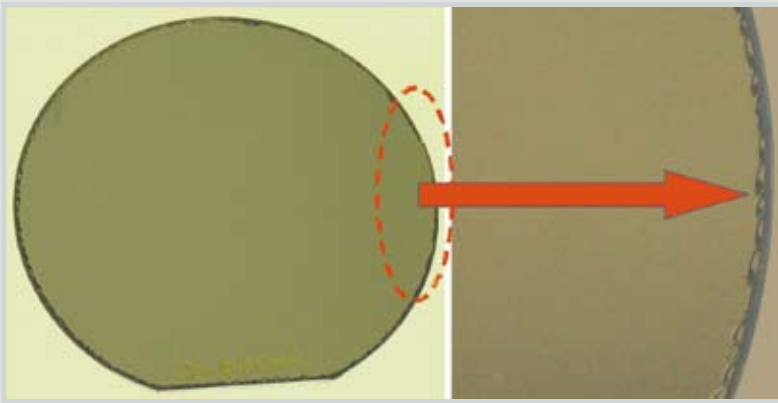


Figure 2:
Bond strength testing using a 100um razor blade confirmed that the strength of Si-Glass interface was greater than the fracture strength of the glass substrate

MATERIALS & METHODS

A series of experiments were conducted to demonstrate Si to glass bonding using the following SUSS equipment: SUSS PL300 vacuum plasma activation system and SUSS CL8 cleaner bonder. The purpose of these experiments was to establish a low temperature production friendly process for Si-glass bonding using vacuum plasma treated wafers.

Different types of alkali and alkali-free glass wafers commonly used in MEMS applications from two different glass manufacturers (Corning and Schott) were tested as part of these experiments. For all experimental runs, 6" Si wafers with and without 100nm thermal oxide were used to bond to 6" glass substrates. For bonding to 8" Schott AF32 glass, bare Si wafers were used. All incoming wafers were first inspected under shallow angle monochromatic illumination to check for any artifacts on the bonding surface of both Si and glass wafers. The glass and silicon substrates were used AS-IS out of the cassette without any kind of cleaning. Both Si and glass wafers were then plasma activated using SUSS PL300 plasma system using O₂/N₂ plasma (150W, 300-385mTorr, 30-60 seconds). The total process time from loading to unloading the wafers in PL300 was less than 4 minutes.

The wafers were then immediately subjected to a short megasonic DIW clean (2 scans) and IR assisted dry cycle (70 seconds) followed by edge-initiated bonding in the CL200. The bond propagation speed for each run was measured

for non-plasma treated as well as plasma treated pairs as shown in Table 1. Following bonding, all bonded pairs were subjected to a 250°C, 4 hour anneal in an oven. The bonded pairs were inspected for any voids before and after the anneal cycle via visual inspection. Razor blade and acoustic inspection (Figure 3) was conducted on selected annealed pairs.

RESULTS & CONCLUSION

Spontaneous bonding for all Silicon to glass pairs was achieved for both non-plasma treated and plasma treated wafers even though the bond propagation speeds varied greatly between different glass substrates (Table 1). All plasma treated substrates showed a bond propagation time of less than 15 seconds demonstrating the marked effect of surface activation. None of the plasma treated Si to glass pairs developed post anneal voids after 250°C anneal as shown by SAM results (Figure 3). The bond strength of plasma treated Glass-Si pairs was higher than the fracture strength of glass demonstrating good bond quality using PL300 activation compared to non-plasma treated wafers which demonstrated bond strengths of <0.8J/m². In conclusion, void-free Glass to Si and SiO₂ was demonstrated using the following commercially available glass wafers

- Schott AF32
- Schott Borofloat 33
- Corning 1737 AMLCD
- Corning Pyrex 7740

A demonstrated process for low temperature high-bond strength direct bonding of Si to glass wafers provides an opportunity for this process to be used for CMOS Image Sensor applications as well as a viable alternative to anodic bonding in a broad range of MEMS packaging and microfluidic applications.

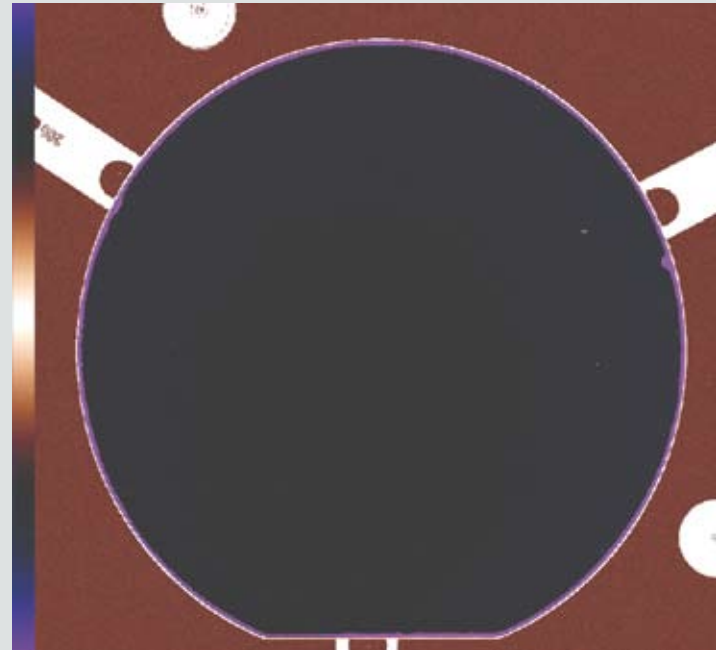


Figure 3:
Void-free SAM Image of a Schott Borofloat 33 wafer bonded to a Si/SiO₂ substrate annealed at 250°C

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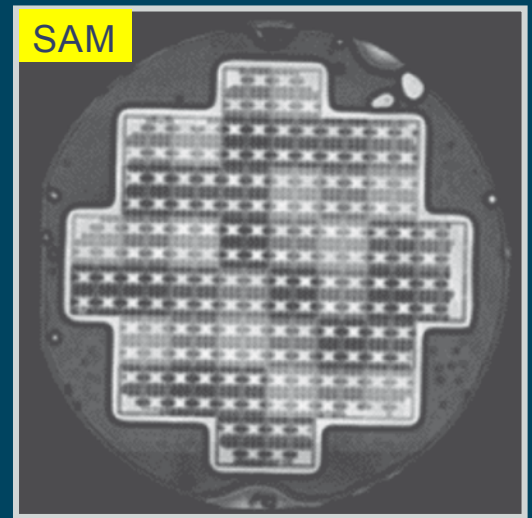
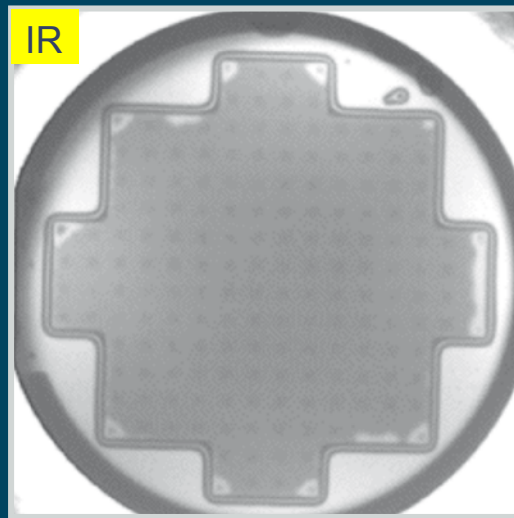
- (1) Anodic bonding for monolithically integrated MEMS, Sensors and Actuators A: Physical, Volume 114, Issues 2-3, (2004), K. Schjølberg-Henriksen, G. U. Jensen, A. Hanneborg and H. Jakobsen
- (2) Silicon-glass wafer bonding with silicon hydrophilic fusion bonding technology

SUMANT SOOD

is the Senior Applications Engineer for Wafer Bonders at SUSS Microtec Inc.. His recent experience includes development of wafer bonding processes for 3D integration, MEMS, SOI, and HB-LED applications.

Sumant has authored and co-authored more than 25 journal and conference papers in wafer bonding, SOI, strained silicon and related areas. He received his B.Tech in Electrical Engineering from Punjab Technical University, India and MS in Microelectronics from University of Central Florida.





Hermeticity Characterization of Eutectic and Low Temperature Direct Bonded SI Wafers Without Getters

ABSTRACT

For many MEMS products hermetic encapsulation is necessary to enable stable functioning over the device lifetime. In this paper low temperature direct bonds and eutectic bonded Si wafers will be compared in terms of hermetic sealing. The leakage test was performed by two different methods, a He leakage test and an FTIR spectroscopy method to determine or quantify the leak rate. It is well known that the bond seal pattern consumes valuable area on the wafer and adversely affects production costs. This study evaluated seal ring width reduction by examination of bonded structures with pattern width sizes from 25 μm , 50 μm , 75 μm and 100 μm .

Volkan Cetin, Suss MicroTec

INTRODUCTION

Wafer bonding as a part of the MEMS packaging process enables the encapsulation of sensitive microstructures. It protects the device during subsequent processing as well as from environmental impacts such as mechanical stress, humidity and high temperatures. Apart from the protective function, wafer bonding enables proper functioning of actuating components and sensing elements. Wafer bonding is also used when each wafer is individually patterned with structures and vertically integrated. As an example, acceleration

sensors, yaw rate sensors and pressure sensors use vacuum packaging to create long device lifetimes and to fulfill a correct functioning in internal components or to provide a reference pressure. During wafer bonding defined pressure levels can be adjusted and encapsulated^[1].

The focus of this work was on low temperature direct bonding (LTB) and eutectic bonding (EB). During EB the bond interface is created by a eutectic reaction of two metals at a precise bond temperature and composition called

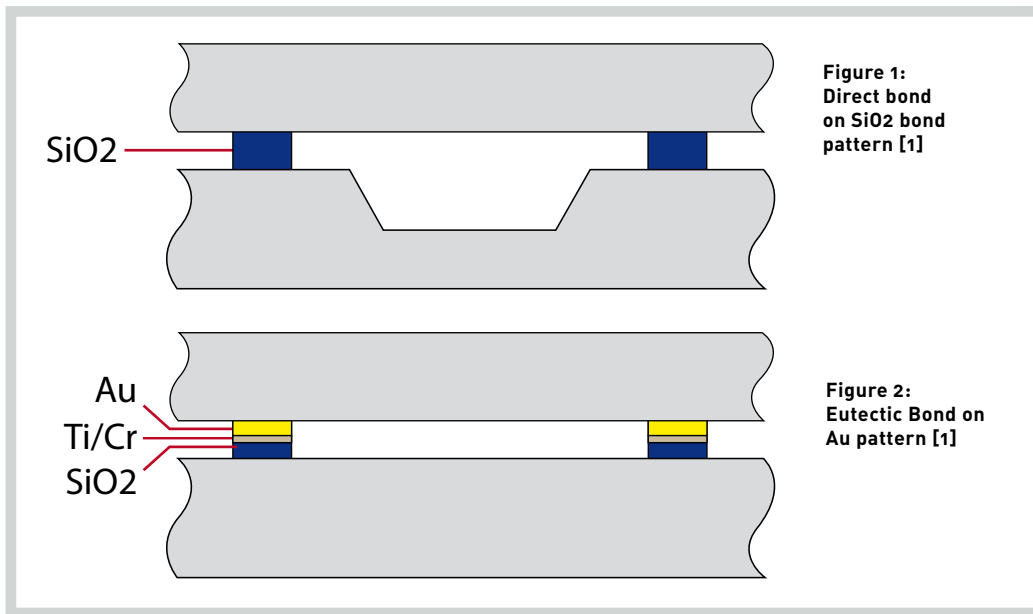


Figure 1:
Direct bond
on SiO2 bond
pattern [1]

Figure 2:
Eutectic Bond on
Au pattern [1]

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- [1] Marco Haubold, "Hermetizitätscharakterisierung von strukturierten und verschiedenartig gebondeten Silizium Waferpaaren", Chemnitz University of Technology, p. 7-8, 2009.
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- [3] Department of Defense, "Test Method Standard Micro-circuits", MIL-STD 883G Method 1014.12, February 2006

the eutectic point. In LTB the interface bond is initially based on van der Waals forces and by annealing it converts to covalent bond formation^[2]. For both methods the best bonding parameters were chosen to avoid bond defects and achieve high bond strength, although it is not proven that high Bond strength correlates with hermeticity.

This paper presents the results of the hermeticity of eutectic and LTB bonded Si wafers without getters. Moreover the bond sealing width is also taken into account. The LTB bond was between Si and SiO2 wet oxide whereas two different eutectic Bond alloys were tested; Si-Au and Au-Sn. After wafer bonding the samples were cingulated and exposed to a bombing chamber with He or N₂O for several hours. It was assumed that the gas will penetrate via the defects at the bond interface into the cavities. After bombing two different leakage tests were applied; the He leakage test and the FTIR spectroscopy leakage test with N₂O test gas to characterize the hermeticity. For the evaluation of the hermeticity with the leakage rate the military standard MIL-STD 883G was taken as reference^[3]. The standard defines a fixed bombing time, pressure and the maximum acceptable leakage rate for a defined internal volume in the cavity. Furthermore the maximum elapsed time between bombing and start of measurement is defined.

pretreatment	bonding method	hermeticity	subjective bonding strength
SC1/SC2/SC1 + O2 plasma + H2O	LTB	+++	++++
SC1/SC2/SC1 + N2 plasma + H2O	LTB	++	++
SC1/SC2/SC1 + N2 plasma	LTB	++	+
SC1/SC2/SC1 + O2N2 plasma	LTB	+++	++
HF oxide etching on Si	EB	+	+

++++ very high
+++ high
++ moderate
+ low

CONCLUSION

LTB and eutectic bonding were successfully performed. The hermeticity characterization of the bonded samples showed good hermetic sealing in accordance to MIL-STD 883G. The application of He leakage test showed that the leakage rates are not measurable which means that there are hermetically sealed packages or the He already diffused out before IT could be measured, which means that volume size of the cavities should be larger for this type of measurement. The FTIR measurement showed that the LTB bonded wafers have a very low leakage rate in the range of 10⁻⁸ – 10⁻⁹ mbar*1/s whereas the EB wafers showed a higher leakage rate which could be related to adhesion problems of the Ti/Cr layer to the SiO2 layer. During dicing the chips separated at this interface due to adhesion issue to the SiO2 layer. Table 1 summarizes the experiments and general observations that will be covered in detail.

Table 1:
Experiment Conditions and Results of Hermeticity and Bond Strength Analysis



VOLKAN CETIN

As Applications Engineer for Wafer Bonders at SUSS Micro-Tec Volkan Cetin has been responsible for development and improvement of bonding processes since 2004. He has co-authored several papers about atmospheric plasma enhanced wafer bonding processes for direct bonding applications and related areas. Volkan received his Dipl.-Ing(FH) in Precision- and Microengineering from the University of Applied Sciences in Munich.



SUSS

Building

Blocks

of

Lithography

INTRODUCTION

By now you will be familiar with Clif's Notes and some of the engineering concepts that have been presented in the SUSS Report. We intend to show how these concepts can be used as building blocks to define and optimize a lithographic process.

YOUR TASK SHOULD YOU CHOOSE TO ACCEPT IT

Suppose you work in a lithographic production area and you've been asked to implement a new resist material in the manufacturing line and that you've been given only three to five days to start your first production lots! You may think it is the end of the world but fear not, help is as close as your SUSS Report! Using the SUSS building blocks with the SUSS ACS200 Coater and MA200Compact you may accept this job without fear of failure.

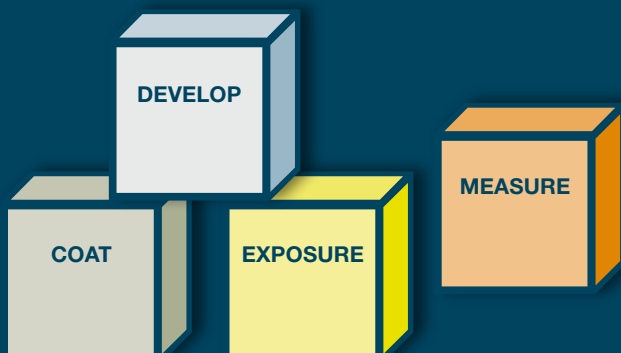
The goals of your project are to

- Define, optimize the coating process to obtain a $7.5 \pm 0.2 \mu\text{m}$ film.**
- Define, optimize the exposure process to resolve a $7.0 \mu\text{m}$ image.**

All of these steps are to be accomplished with the lowest possible cost in the shortest time. It goes without saying that the process must be robust and stable.

OPTIMIZATION OF THE COATING PROCESS

The manufacturing line currently is running 200mm wafers, you are very aware that these wafers are costly and you would like to reduce the costs of experimentation. It would be nice if you could use some of those 150mm wafers left over from the recent conversion to 200mm wafers. Then you remember that article from SUSS dealing with coating of 100mm to 300mm wafers made easy¹ which indicated that the size of the wafer had little effect upon the final thickness results. In addition the report also indicated the use of statistically designed experiments, specifically response surface analysis (RSA), would allow you to define the coating process in the fewest number of wafers at the lowest cost. Based upon the procedures used in that paper you design an experiment evaluating the effects of spin speed and spin time, Table 1, columns 2 and 3, for the new resist material using 150mm wafers.



Trial	Speed	Time	Mean	Sigma1	Sigma2	Range	EB Width	EB Height
1	1439	17.3	14.122	0.250	0.276	0.8093	2.18	11.56
2	3561	17.3	7.091	0.046	0.047	0.1474	0.98	6.11
3	1439	52.7	11.065	0.051	0.059	0.1895	1.84	12.44
4	3561	52.7	6.758	0.044	0.033	0.1832	0.86	6.37
5	1000	35.0	14.789	0.144	0.130	0.4725	2.10	14.27
6	4000	35.0	6.406	0.049	0.042	0.1592	0.72	4.26
7	2500	10.0	10.435	0.150	0.162	0.493	1.90	11.25
8	2500	60.0	8.145	0.070	0.034	0.3138	1.50	8.14
9	2500	35.0	8.230	0.099	0.068	0.4172	1.26	8.40
10	2500	35.0	8.263	0.122	0.046	0.5539	1.54	11.00
11	2500	35.0	8.242	0.054	0.040	0.1889	1.68	10.92
12	2500	35.0	8.251	0.067	0.047	0.2745	1.62	10.65
13	2500	35.0	8.285	0.060	0.045	0.2466	1.62	10.10

Table 1:
Response Surface
Experiment Design

Again you have a concern with taking too much time at the coater running these thirteen samples and you remember another of Clif's Notes article dealing with the SUSS automated spin coaters, ACS200 Plus and Gamma tools². This method called 'sequence stacking' allows the engineer to define and load each trial of the experiment as a separate sequence, identify which wafer in the cassette to be used for each sequence, start the process and walk away from the tool. Each experiment/sequence will now be run automatically. So now you can devote your time to other engineering tasks while the SUSS tool coats and bakes your wafers per the experiment design.

At this point in the evaluation you realize that the specification for thickness uniformity of plus or minus 0.2um may not be possible since your site just received a new resist measurement tool and you have no idea of the capability of the measurement tool. Thank goodness you remember yet again another of Clif's Notes dealing with measurement tool gage capability analysis³ and he recently sent you the Excel file to be used for the study. So you quickly go off to gather some samples for the capability study, five or six wafers will do, and start the evaluation.

While the resist tool measurement capability study is being run by your helpful staff you take the recently coated RSA wafers from the Gamma tool and start some other measurements. Although the requirement was for this process was only for a specific thickness you realize there are other parameters that may affect your process such as edge

bead height and width. These measurements may be completed on the Tencor P-16 just down the aisle from the new thickness measurement tool, see results in Table 1, so you can monitor the process for the gage capability study.

Finally the gage study has been completed and the results of the analysis

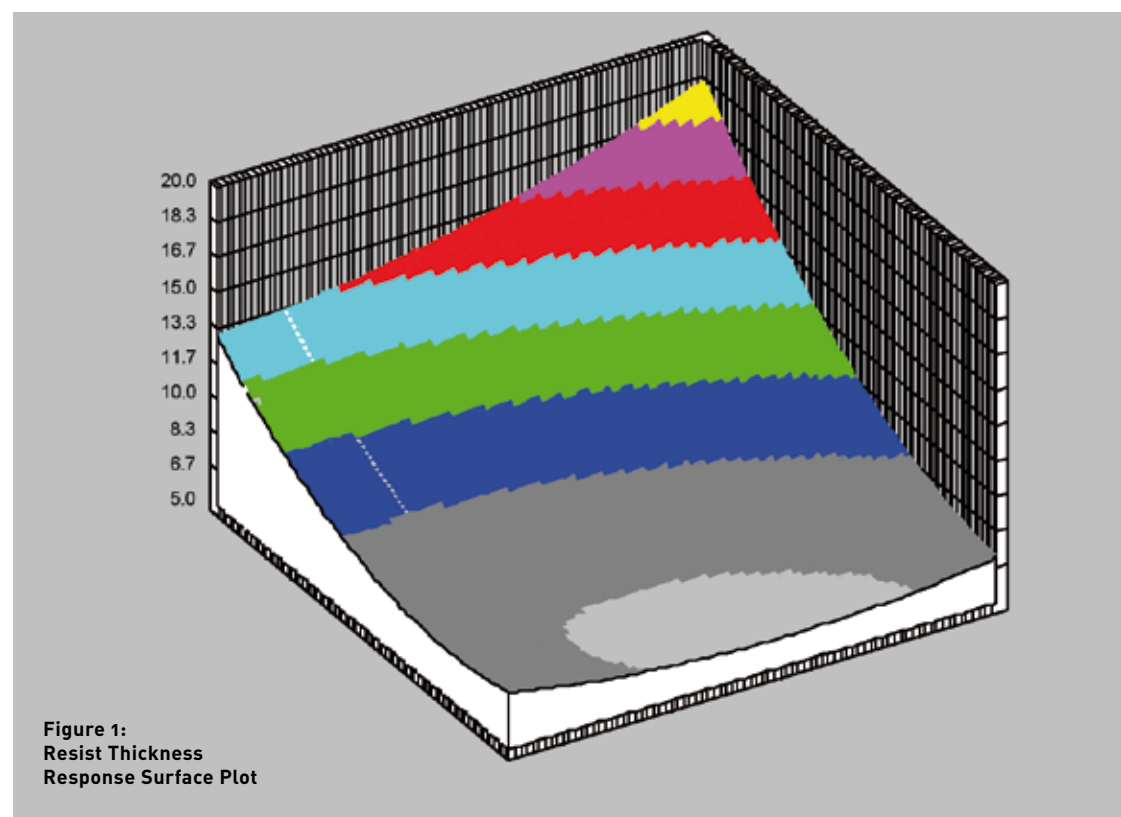


Figure 1:
Resist Thickness
Response Surface Plot

Variable Levels Set Points				
Name	Plot	Low	High	Set Pts
Speed	yes	2000.00	4000.00	3400.00
Time	yes	10.00	50.00	15.00

Responses: Min, Max, Optimum, Estimated, & Plot Values									
Response	Min	Max	Optimum	A	B	Estimate	Plot	From	To
Mean	7.00	8.00	7.50	.1	.1	7.49	yes	5.00	20.00
StdDev	.05	.15	.05	.1	.1	0.06	Yes	.00	.00
EB Wide	.10	1.50	.10	.1	1	1.20	Yes	.00	.00

Table 2:
Desired Response Levels for Process

from the Excel spreadsheet provided by SUSS indicates the precision to tolerance ratio of less than ten percent! Based upon current thinking a value less than ten percent for the P/T ratio is excellent so you may now complete the film thickness measurements which are presented in Table 1. The results are input to the experiment design program with a very good correlation between the calculated and measured values.

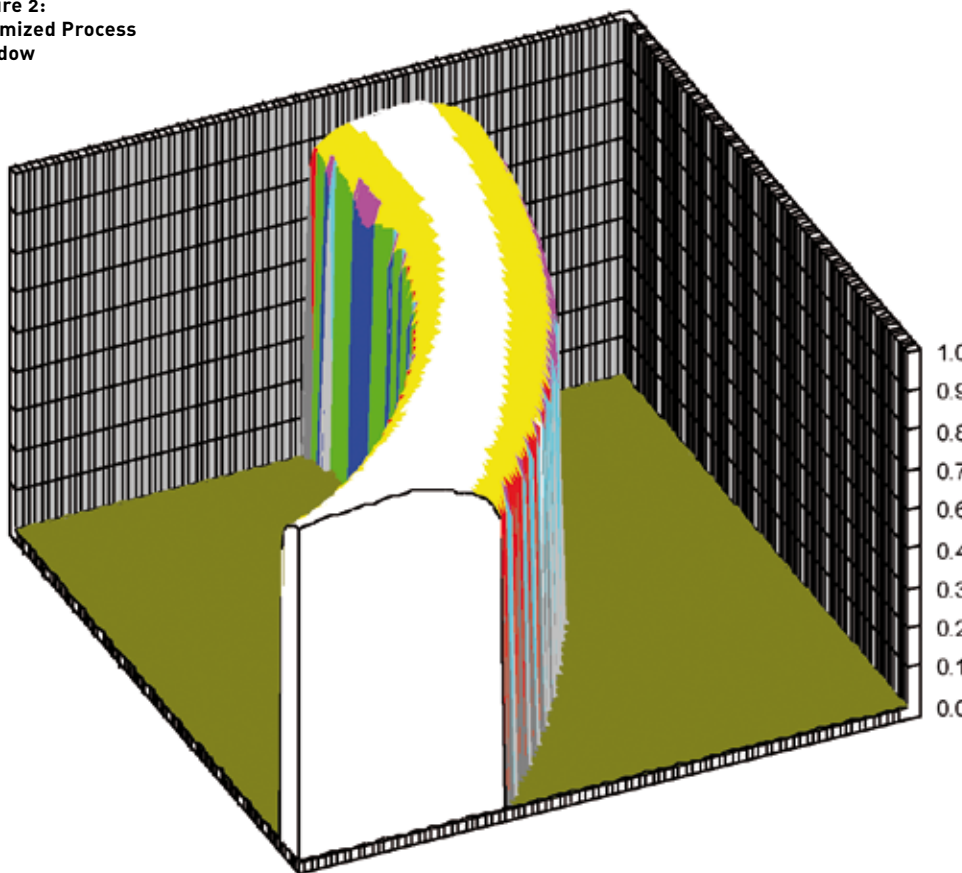
This means the response surface equations may be used to estimate each response with a good probability of being correct. A sample response surface for the thickness of the film is shown below, Figure 1.

We don't have the luxury of taking the time to review each response and trying to find the best process manually so why don't we let the computer do

it for us! We simply input the desired levels for each response, see Table 2, and have the computer find the set of conditions which will meet all of our requirements simultaneously, see process window in Figure 2.

The graph shown above represents the region in multi-dimensional space where the desired levels of each response will be met at the same time as a function of spin speed and spin time. Any point within this band will meet the specifications for the process. In order to meet throughput requirements the process is defined at the shortest allowed spin time of about 15 seconds at 3400 rpm. A group of wafers are coated to confirm the optimized process with the very good results shown in Table 3. Definition of the coating process should have taken two to three days maximum.

Figure 2:
Optimized Process Window



OPTIMIZATION OF THE EXPOSURE PROCESS

We have an optimized coating process and must now define the exposure dose required to produce the images we want in the shortest possible cycle time. Fortunately another of the Clif's Notes articles describes a method to determine the optimum dose with only one or two wafers which were just coated as a part of the thickness confirmation test⁴. By using an exposure step tablet you will be able to obtain up to six levels of exposure on one wafer using only one exposure cycle. Simply measure the overall light intensity and set the exposure time sufficient to totally expose the resist based upon the formula proposed in the SUSS Report article. One wafer was exposed in proximity mode for ten seconds then developed using an existing process on the SUSS coater, developer. Using an existing documented develop process will reduce the engineering time needed to implement this new process. The results of this test presented in Table 4 indicate that a

Table 3:
Predicted versus Actual Results

	Speed	Time	Thickness	1-Sigma	EB-Wide
Predicted	3400	15.0	7.49	0.06	1.20
Actual	3400	15.5	7.41	0.06	1.17

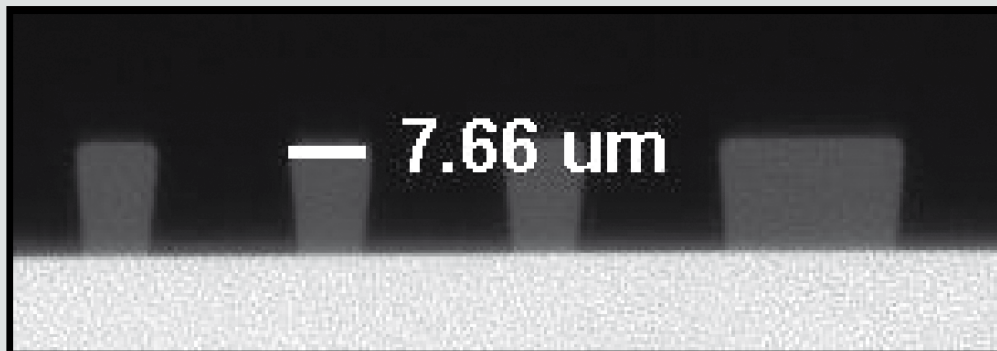


Figure 3:
Cross-Sectional
View of Test
Images

Step	Intensity	% Trans	Exp Time	Dose	Thickness Remaining
1	55.0	100%	10.00	550.0	0.01
2	47.1	86%	8.56	471.0	0.08
3	36.3	66%	6.60	363.0	2.50
4	29.9	54%	5.44	299.0	4.00
5	23.9	43%	4.35	239.0	7.45
6	11.8	21%	2.15	118.0	7.50

Table 4:
Time To Clear
(TTC) Results

nominal time of about 9 to 10 seconds should be used in order to insure the resist is completely developed. This is the shortest possible exposure cycle for this new resist material using the existing develop process.

Upon completion of the first test wafers exposed at 500 mJ/cm² you find images printed nicely with a slight print bias of about +0.7μm, i.e. the 7.0μm designed image is actually 7.7 μm. You will implement this process and continue to monitor image size with a goal towards moving the size closer to the target.

SUMMARY

In a very short time of three to five days we have shown how it is possible to define an optimized lithographic process for coat, expose and develop. This process is optimized for the best possible coating quality and the shortest possible cycle times.

CLIFF HAMEL

is the principle applications engineer at SUSS MicroTec, Inc. for lithography processes involving full field mask aligners and automated cluster coating equipment. Over the last ten years at SUSS he has co-authored several papers in the field of thick resist processes and process optimization. He has over 26 years of BEOL process and mask fabrication experience at IBM where he was the principle engineer and inventor for lift off process development. He received his BS in chemical engineering at Trinity College of Vermont.

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- Is the Tail Wagging the Dog?
http://www.suss.com/company/news/customer_magazine
http://www.suss.com/company/news/customer_magazine/issue-0209
- You Can Define That Exposure Dose in One Wafer
http://www.suss.com/company/news/customer_magazine
http://www.suss.com/company/news/customer_magazine/issue-0108

SUSS MicroTec in the News

Here's a summary of our recent press releases.
To read the entire press release, please visit
<http://www.suss.com/company/news>

September 28, 2009

SUSS MicroTec Cooperates with Research Institute ITRI on Technology Development in 3D Integration

SUSS MicroTec announced today that it is engaging with one of the world's leading research institutes, the Industrial Technology Research Institute (ITRI) in Taiwan, on the development of 3D integration technologies. The Advanced Stacked-System Technology and Application Consortium (Ad-STAC), a multinational research association led by ITRI, will implement the 300mm lithography cluster LithoPack300 and the 300mm bond cluster CBC300 of SUSS MicroTec in its 300mm demo production line at ITRI in Hsin-Chu, Taiwan. With this SUSS MicroTec is joining the consortium and will actively apply its expertise in 3D Integration to further process development.

"SUSS MicroTec is known as the leading expert in their field so I am confident that their experience will become a real asset to the challenging environment of our demo production line"

Dr. Ian Chan, VP & EOL General Director, ITRI

January 13, 2009

SUSS MicroTec AG: Contract Negotiations for the Purchase of HamaTech APE GmbH & Co. KG Successfully Concluded

SUSS MicroTec AG today announced the conclusion of contract negotiations to acquire HamaTech APE GmbH & Co. KG, a wholly owned subsidiary of Singulus Technologies AG. Yesterday night, both parties signed a corresponding



Steve Harris (Executive Vice President Cascade Microtech, Inc.) and Frank Averdung (President & CEO Süss MicroTec AG) kick off the strategic partnership

purchase agreement, subject to the negotiated closing conditions. The agreement stipulates a purchase price of EUR 4.5 million plus a further EUR 4.5 million for the acquisition of the land and company building at the Sternenfels site. The closing date of the transaction is set for January 2010.

"HamaTech APE's 20 years of experience in developing processes and equipment along with its highly innovative cleaning technology ideally complement SUSS MicroTec's core competency of critical wet processing in semiconductor production."

Frank Averdung, President & CEO, SUSS MicroTec

January 19, 2010

SUSS MicroTec Expands Activities in Wafer-Level Camera Applications Installation of Solution Set at Q-Technology

SUSS MicroTec announced that Q-Technology Limited (Q Tech), manufacturer of compact camera modules for the global cell phone, notebook computer and security industry, has successfully installed a full SUSS equipment set at Q Tech's facility in Hi-Tech Industrial Park Kunshan City, Jiangsu Province, China. The 200mm mask and bond aligner, spin and spray coaters and wafer bond systems are utilized for Q Tech's wafer-level camera manufacturing services. With this project SUSS MicroTec expands its activities as an equipment supplier supporting

image sensor packaging and wafer-level camera manufacturing processes.

"For us the leading-edge wafer-level packaging systems of SUSS MicroTec are the equipment of choice."

Dr Hao Zhou, CEO, Q Tech

January 28, 2010

SUSS MicroTec AG sells Test Systems Division

SUSS MicroTec announced the sale of its Test Systems Division, which is located in Sacka near Dresden, Germany, plus other related assets. The Company was sold to Cascade Microtech, Inc., a worldwide leader in the precise electrical measurement and test of integrated circuits. With the divestment of the SUSS MicroTec Test Systems GmbH and the recent acquisition of HamaTech APE, SUSS MicroTec will focus on its core competency of microstructuring for microelectronics applications.

"Having a broad product range for 3D integration, we anticipate future collaboration with Cascade Microtech in order to address the complex issues in developing and testing 3D through silicon vias (TSVs)."

Frank P. Averdung, President and CEO of SUSS MicroTec

February 16, 2010

HamaTech APE Completes Initial Stage of EUV Mask Cleaning Program at imec

HamaTech APE, a SUSS MicroTec company, today announced that it has completed the initial stage of the Extreme Ultraviolet (EUV) Mask Cleaning Program in partnership

with imec, a world-leading nanoelectronics research center. With the installation of HamaTech's MaskTrack Pro, imec's 300mm clean room is the first facility in the world equipped with a mask integrity infrastructure for EUV point-of-exposure cleaning research.

"Working with imec, we will look beyond the normal parameters of the infrastructure to develop a holistic approach that guarantees the most stringent mask integrity requirements of Next Generation Lithography, including EUVL."

Wilma Koolen-Hermkens, Chief Executive Officer of HamaTech APE

March 9, 2010

Amkor Technology Installs Systems from SUSS MicroTec

SUSS MicroTec has received orders for multiple 300mm lithography systems from Amkor Technology Inc., an industry leading supplier of innovative packaging solutions. The equipment package includes MA300 Gen2 mask aligner systems and ACS300 Gen2 wafer processing clusters for wafer level packaging, wafer bumping and 3D integration technology. Installations at Amkor's K4 plant in Gwangju, Korea, and T1 fab in Hsin-Chu, Taiwan, are scheduled to be completed in Q3 2010.

"SUSS MicroTec's lithography systems have been an integral part of our success and have set an exceptional track record for process capability, reliability, support and overall cost of ownership for our worldwide operations."

ChoonHeung Lee, CVP and CTO, Amkor Technology

Training Schedule 2010

Lithography Equipment

A P R I L	Machine-Type	Level
29/03/10 - 01/04/10	Litho Application Training	
29/03/10 - 01/04/10	ACS300 Gen2	L3
07/04/10 - 09/04/10	MA200Compact	L2
08/04/10	Litho Application Training	
12/04/10	MJB4	L2
13/04/10	MA6/8	L2
14/04/10 - 15/04/10	AltaSpray	L2
14/04/10 - 16/04/10	Gamma	L2
16/04/10	Nanoimprint Training	
19/04/10 - 23/04/10	Gamma	L3
19/04/10 - 20/04/10	MA150/200CC	L2
26/04/10 - 29/04/10	Litho Application Training	
26/04/10 - 29/04/10	MA150/200E	L3
M A Y	Machine-Type	Level
03/05/10 - 06/05/10	MA150/200e	L3
03/05/10 - 06/05/10	MA300	L2
04/05/10 - 06/05/10	Gamma	L2
07/05/10	MA8 Gen3	L2
10/05/10 - 12/05/10	MA8 Gen3	L2
18/05/10 - 20/05/10	MA150/200e	L3
18/05/10 - 20/05/10	MA8 Gen3	L3
18/05/10 - 20/05/10	ACS300 Gen2	L2
25/05/10	MA6	L2
25/05/10 - 27/05/10	PatMax	
26/05/10 - 27/05/10	MA6	L3
27/05/10	Spray Coater Nozzle Training	
J U N E	Machine-Type	Level
07/06/10 - 09/06/10	AltaSpray	
07/06/10 - 11/06/10	MA200Compact	L3
15/06/10 - 17/06/10	E Plan	
21/06/10 - 25/06/10	MA300	L3
22/06/10 - 24/06/10	ACS200P	L2
J U L Y	Machine-Type	Level
28/06/10 - 02/07/10	ACS200P	L3
05/07/10	MJB4	L2
06/07/10	MA6/8	L2
07/07/10 - 08/07/10	AltaSpray	L2
09/07/10	Nanoimprint Training	
12/07/10 - 15/07/10	COA/DEV Pump Training	
13/07/10 - 15/07/10	MA200Compact	L2
20/07/10 - 22/07/10	Gamma	L2
20/07/10 - 22/07/10	MA300	L2
J U L Y	Machine-Type	Level
26/07/10 - 29/07/10	MA150/200e	L3
26/07/10 - 30/07/10	Gamma	L3
A U G U S T	Machine-Type	Level
02/08/10 - 06/08/10	MA200Compact	L3
03/08/10 - 05/08/10	AltaSpray	
10/08/10 - 12/08/10	MA8 Gen3	L3
11/08/10	Spray Coater Nozzle Training	
16/08/10 - 18/08/10	PatMax	
17/08/10 - 19/08/10	ACS300 Gen2	L2
24/08/10 - 26/08/10	E Plan	
S E P T E M B E R	Machine-Type	Level
30/08/10 - 02/09/10	Litho Application Training	
20/09/10 - 24/09/10	MA300	L3
21/09/10 - 23/09/10	ACS300 Gen2	L2
27/09/10	MJB4	L2
28/09/10 - 30/09/10	ACS300Plus	L2
28/09/10	MA6/8	L2
29/09/10 - 30/09/10	AltaSpray	L2
O C T O B E R	Machine-Type	Level
01/10/10	Nanoimprint Training	
04/10/10 - 08/10/10	ACS300Plus	L3
05/10/10 - 07/10/10	MA200Compact	L2
12/10/10 - 14/10/10	Gamma	L2
12/10/10 - 14/10/10	MA300	L2
18/10/10 - 21/10/10	MA150/200e	L3
20/10/10	Spray Coater Nozzle Training	
25/10/10 - 28/10/10	Litho Application Training	
N O V E M B E R	Machine-Type	Level
02/11/10 - 04/11/10	AltaSpray	
08/11/10 - 12/11/10	MA200Compact	L3
16/11/10 - 18/11/10	ACS300 Gen2	L2
16/11/10 - 18/11/10	MA8 Gen3	L3
22/11/10 - 25/11/10	COA/DEV Pump Training	
23/11/10 - 25/11/10	E Plan	
D E C E M B E R	Machine-Type	Level
29/11/10 - 02/12/10	Litho Application Training	
06/12/10 - 10/12/10	MA300	L3
07/12/10 - 09/12/10	Gamma	L2

Further information on trainings at
www.suss.com/training

Some of the opportunities to meet with SUSS MicroTec in the upcoming months:

April

- MRS Spring Meeting** · San Francisco, CA, USA 5. - 9. Apr
Photonics Moscow · Moscow, Russia 19. - 21. Apr

May

- Technologien und Werkstoffe der Mikrosystem- und Nanotechnik** · Darmstadt, Germany 10. - 11. May
ICEP 2010 · Hokkaido, Japan 12. - 14. May
Semicon Singapore · Singapore 19. - 21. May
ECTC · Las Vegas, NV, USA 26. - 29. May

June

- EIPBN** · Anchorage, AL, USA 1. - 4. Jun
Semicon Russian · Moscow, Russia 12. - 14. Jun

July

- Semicon West** · San Francisco, CA, USA 13. - 15. Jul
Micromachine · Tokyo, Japan 28. - 30. Jul

August

- COMS** · Albuquerque, NM, USA 28. Aug - 2. Sep

September

- Semicon Taiwan** · Hsin-Chu, Taiwan 8. - 10. Sep
ESTC · Berlin Germany 13. - 16. Sep
MNE · Genoa, Italy 19. - 22. Sep

October

- NNT** · Copenhagen, Denmark 13. - 15. Oct
IWLPC · Santa Clara, CA, USA 11. - 14. Oct
Semicon Europe · Dresden, Germany 19. - 21. Oct
EOS Annual Meeting · Paris, France 26. - 29. Oct
IMAPS · Raleigh, NC, USA 31. Oct - 4. Nov

November/December

- MRS Fall Meeting** · Boston, MA, USA 29. Nov - 3. Dec
Semicon Japan · Tokyo, Japan 1. - 3. Dec

Please check our website for any updates: www.suss.com/events

We hope you found this edition of the SUSS Report interesting and informative. For more information about SUSS and our products, please visit

www.suss.com

or write to info@suss.com with your comments and suggestions.

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SUSS + MicroTec
 Our Solutions Set Standards