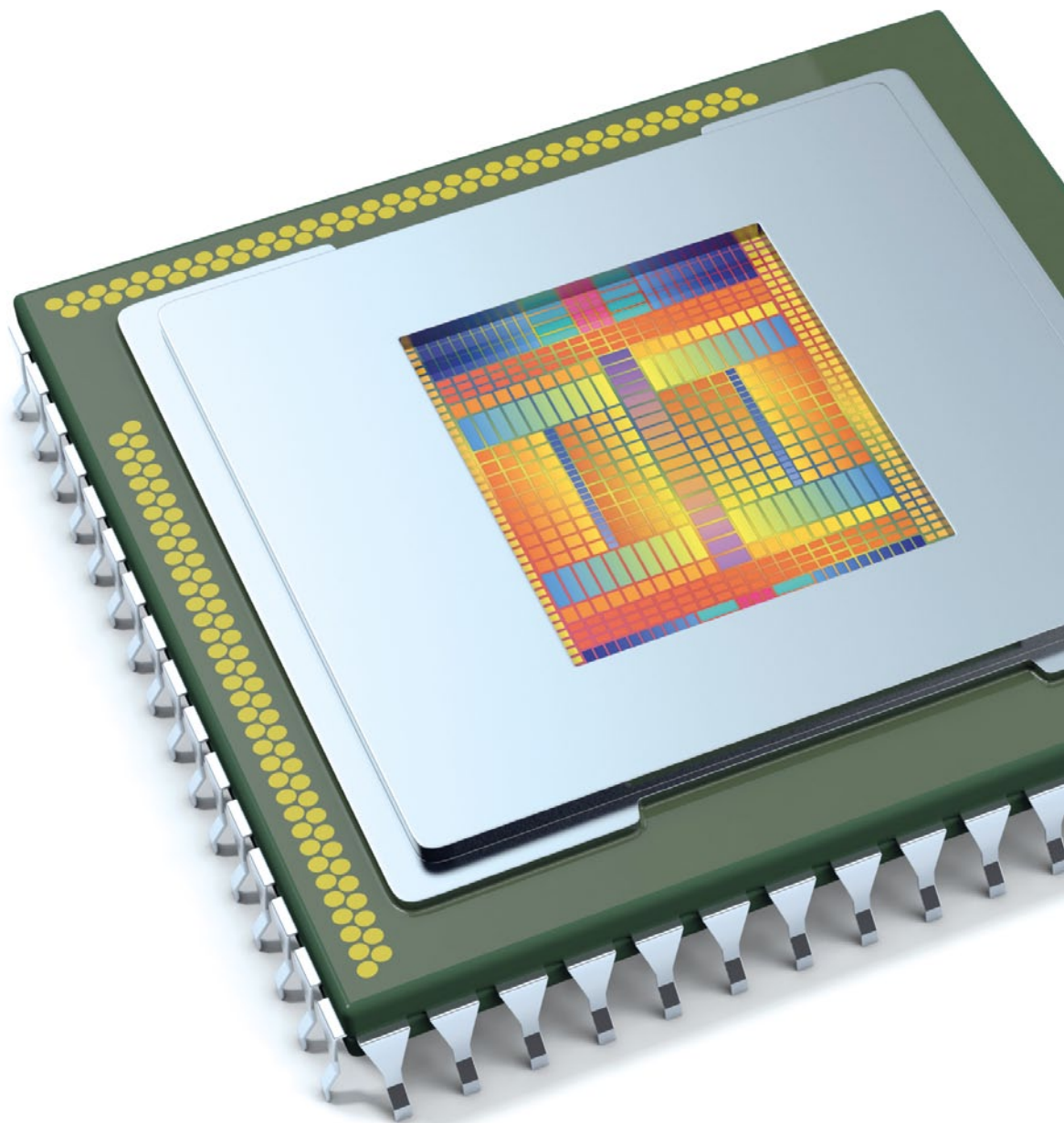




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CEO, SÜSS MicroTec AG

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+ EDITORIAL



Dr. Franz Richter, CEO, SÜSS MicroTec AG

Dear Reader,

I am Franz Richter and I am President and CEO of SÜSS MicroTec AG. The magazine you are holding is the latest edition of our customer magazine SUSS Report 2016 and is hot off the press. Have a look and read about new developments at SÜSS MicroTec over the last months.

Besides those, we have more developments in progress, which will come to market during the next quarters. Strong R&D activity remains extremely important for our industry and for our company. We are operating in fast-changing markets with very demanding customers. Product life cycles of only a few years, if that much, force our customers to constantly invent new processes and subsequently new technologies. We as an equipment supplier have to support this trend and provide state-of-the-art solutions for many different production needs.

But we are no longer just an equipment supplier, we also do a lot of process development and optimization. Our understanding of the processes currently used in production must be complete in order to improve our equipment to the best advantage of our customers.

I strongly believe that some of the markets we operate in face strong growth over the next years. Wafer-Level Fan-Out, Panel-Level Fan-Out and ultimately 3D-stacking using TSVs for chip connection will play a dominant role in future packaging applications.

We see strong growth opportunities not only in the field of electronics packaging. Similar growth is being spurred by new developments like "Industry 4.0" or the "Internet of Things" (IoT), leading to completely new levels of mobility, connectivity and cloud computing. On the device level, there is a strong need for more and new MEMS and optical systems to support faster communication and connectivity.

Exciting and demanding challenges lie in front of our customers and our company. In many cases, outstanding solutions and results can only be achieved if users and developers of production equipment closely work together in order to optimize the whole production process for highest quality and productivity. As an equipment provider, we are dedicated to such close collaboration with our customers to better understand their needs and provide best-in-class solutions to those needs. Let's continue to work together as engineers and business partners for our mutual benefit.

Enjoy reading the SUSS Report 2016!

A handwritten signature in blue ink that reads "F. Richter". The signature is stylized and fluid.

Franz Richter

NEW EXCIMER LASER-BASED DUAL DAMASCENE PROCESSES FOR HIGH I/O APPLICATIONS WITH ULTRA-FINE LINE ROUTING

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In this paper a novel excimer laser dual damascene process is presented to generate a fine line multi-metal layer routing. A laser stepper technology together with a quartz mask allows a high throughput in combination of ultra-fine RDL and via openings below 5 μm . The depth of ablation into the polymer is controlled by the number of laser pulses and fluence. The patterning of RDL and Via is done in one excimer laser ablation step, with an aspect ratio of 1:1. A landing pad is not needed in the lines to allow via full contact because of the sub-micro meter overlay accuracy of the laser ablation system, which allows to realize a fine routing layer density. The vias and lines are metallized by a galvanic process. Test structures have been designed and fabricated by using low cure temperature PI, BCB, and ABF as dielectric material to demonstrate the material flexibility.

INTRODUCTION

Advanced packaging has become the key point for reaching the goal of continuous miniaturization, higher performance, low cost and decreasing of time-to-market of electronic devices. The wafer-level packaging is today the dominating method in high-end mobile smartphone systems and it is still trending to increase. The next big packaging trend will be Fan-Out Wafer-Level Packaging (FOWLP) with reconfigured wafers based on placed known good dies which are embedded in molding compound. This opens a lot of opportunities for innovative packaging and is also a key for heterogeneous packaging like the integration of memory and ASIC chips aside of passives in one package. The major application today is only a single chip package, where the molding is used as expanded area for higher pitch breakout of one chip. The demands regarding the feature size is similar to the classical Fan-In package and still relatively moderate and could be achieved with one copper redistribution layer.

In the future, FOWLP will be used more and more for multi-chip packages. The function of the chip-to-chip routing, which is normally done on Printed Circuit Boards (PCB), is now done by the redistribution layer. This results in increasing demand for RDL and sets new challenges on the layers stacking. The new approach of laser enabled dual damascene process for wafer-level packaging could be used to overcome these challenges.

The laser structuring of the dielectric layer for interconnect formation between metal layers is the dominating process in PCB processing. The structuring is done with UV or IR lasers, where ultra-short picoseconds pulses are used. The laser process is proven to be a cost efficient process with the benefit to realize a feature size of the via which is less determined by the choice of the used material. Figure 1 shows a UV laser drilled via to connect an embedded die in a printed circuit board with a diameter of 30 μm .

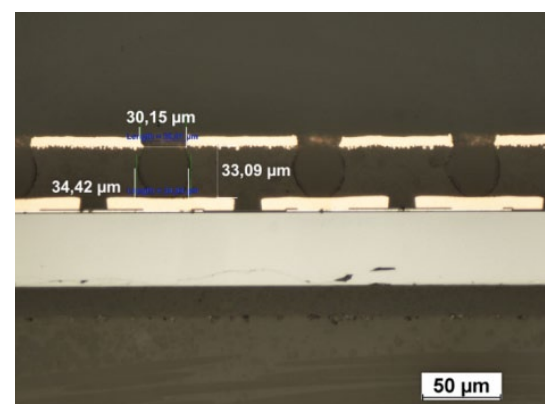


Figure 1 Micro-via in a PCB which is drilled with a UV laser

In contrast to PCB technology, the structuring of dielectric layers for wafer-level packaging is mainly done by a photolithographic process. The feature size is dominated by the photolithographic properties of the used polymer material.

The laser ablation of thin film polymers is in principle not a new technology for wafer-level packaging. The laser ablation of polymers was first reported by Srinivasan et al.^[1] in 1982. Low speed and high cost was the major barrier for further developments twenty years ago. But the combination of excimer laser systems with scanning/stepper technology platforms with quartz masks has improved this technology to overcome the limited throughput. The excimer laser structuring is able to realize smaller via with smaller feature sizes compared to current photo-polymer processes where a via is limited to an aspect ratio below 1.5. In this work a laser ablation system from SUSS MicroTec (ELP300) has been used which is equipped with a laser source from Coherent (LPXpro 305) where vias are generated with an aspect ratio close to 5 (Figure 2). The laser has a power of 40 W and the characteristics are summarized below:

- Wave length: 248 nm (KrF)
- Shoot repetition rate: 50 Hz
- Puls length: ~ 30 ns
- Beam spot size: 6.5x6.5 mm²
- Fluence range: 70-650 mJ/cm²

The used tool is configured for a reticle size of 6.5 by 6.5 mm and the moving speed of the stage is 50 mm/s.

LASER SCANNING ABLATION PROCESS USING A MASK

The laser ablation process can be simply described by the removal of the polymer without damaging the surrounding areas. No cracks or any other heat-affected zone should limit the high-density applications^[9]. When a high-energy UV-Laser pulse is focused onto a material so that

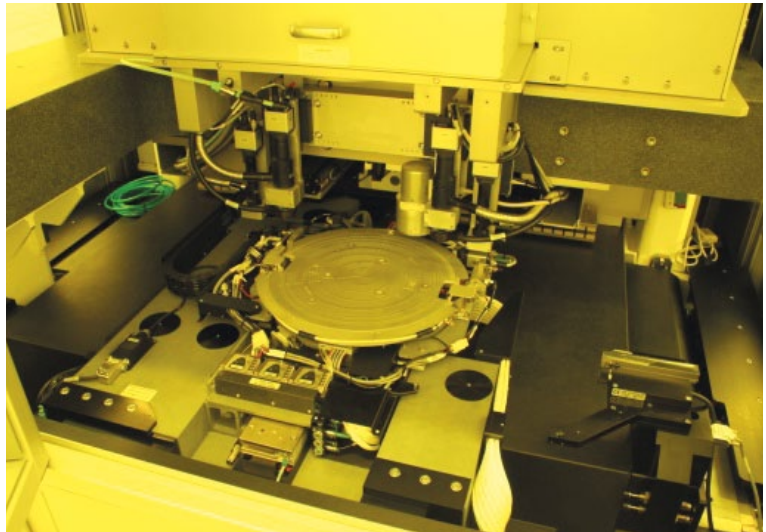


Figure 2 300µm wafer stage of the excimer ablation tool ELP300

the intensity (which is measured as the fluence) is above a material-dependent threshold value, then the high-energy ultraviolet photons directly excite electrons and break interatomic bonds. This threshold is quite important because it can be used to structure polymers on top of inorganic materials like metal without destroying the metal underneath because the threshold of metals is mostly very different to the threshold of dielectric materials. Along with the subsequent shock wave, this causes material to be ejected at high velocity in the form of a fine powder or gaseous organic byproducts. Each pulse lasts a few nanoseconds and removes a thin layer of the polymer. Unlike most other laser types, the excimer produces a large area beam that is usually rectangular in cross-section. This has the advantage to be highly compatible with the use of photomasks. For the light blocking metal Al is most suitable due to a very high threshold level

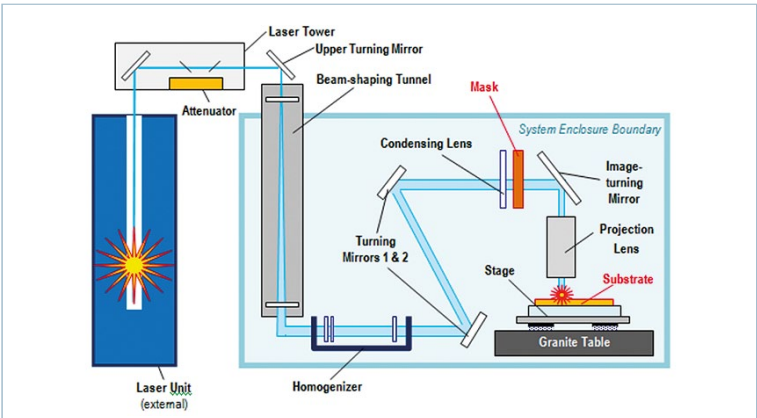


Figure 3 Schematic setup of an excimer laser stepper

which makes the Al mask stable for a long production cycle time. The schematic of the excimer laser stepper is shown in Figure 3.

The aluminum is patterned as the inverse of the pattern to be structured on the actual polymer layer. The openings in the metal on the mask define the pattern that will be laser ablated. The photomask output is then reduced through a reduction lens (for example 2.5x) onto the target – the targeted area depends on the laser power and the ablation threshold of the target material. Regarding the reduction of the optical system there are less demands of the feature resolution of the mask which leads to lower mask costs. Hence, the throughput is very high compared to a PCB drilling system because multiple vias

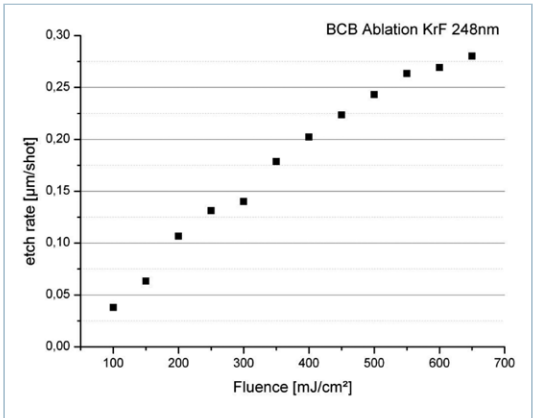


Figure 4 Etching rate of BCB vs the fluence

are generated simultaneously during exposing of one reticle. (i.e., multiple vias per second) and throughput is independent from the number of vias. The reason is that the amount of material removed with each laser pulse, i.e., the depth of any hole or trench, is dependent only on the fluence (energy), number of pulses and the specific materials to be ablated. The etch rate in relation to the energy is shown in Figure 4. The reticle size and the fluence are defined by the available laser systems.

The etch rate is less than 50 nm for low fluence of 100 mJ/cm² and can reach around 300 nm per pulse for a fluence of 650 mJ/cm² (this is the maximum of the used laser system) and can reach up to 1000 nm per pulse for some materials with a fluence of 1,200 mJ/cm², which is the maximum fluence, if a 300 W laser source is used. The investigations show that the ablation rate between different polymers is nearly similar. Figure 5 shows the etching profile of a line into a low cure polyimide layer at a fluence of 400 mJ/cm² with different number of pulses from 1 to 30.

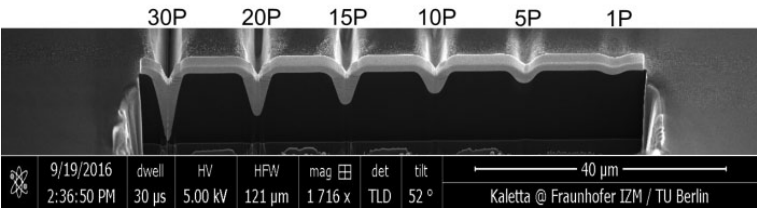


Figure 5 Ablation profile in low temperature polyimide vs number of pulses

The ablation rate is nearly constant for different geometry sizes and is not affected by the depth of the structure which could be seen in Figure 6.

The throughput for such a system is now defined by the fluence power of the laser system, the number of pulses per second and the reticle size. From view of the tool design the important factors are the reticle size and the stepping speed of the mask. The nature of the polymer is less important and only the thickness of the polymer layer is important.

EXCIMER LASER DUAL DAMASCENE PROCESS

The principle of the excimer laser ablation process is the direct removal of polymer materials from the desired pattern on a fully cured film. Patterning after curing provides complete pattern integrity of the structure profile as compared to structures made using photolithography process. For example, the via formed by a lithography process will need to be subjected to a curing process after exposure which in turn reflow/shrink the resist. Therefore, the initial via profile will be in turn lost. In the dual damascene process using excimer laser, the Via and RDL patterning is done in one step and would be either via first and trench (RDL) last or trench first and via last. The last option is the most preferred one for advanced packaging as it allows better control of the via profile and its bottom critical dimension. The dual damascene is already well defined and vetted in the Front-End-of-Line (FEOL) using lithography and dry etching. The process flow for an excimer laser enabled dual damascene process is shown in Figure 7 (trench first and via last process).

First step is the polymer coating on the wafer and curing. The curing of the polymer is done before the patterning process. The thin film poly-

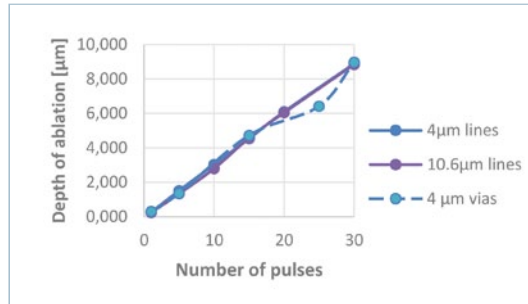


Figure 6 Measured ablation rate of different feature sizes and number of pulses

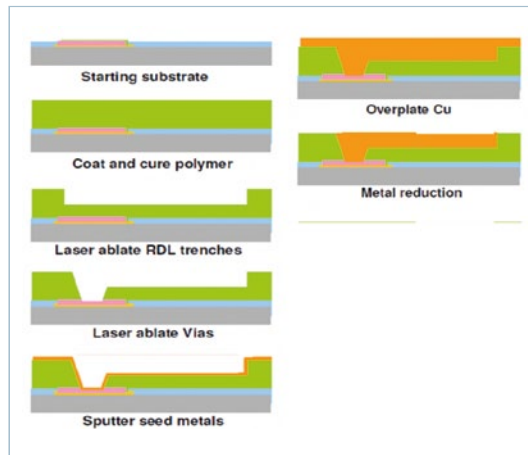


Figure 7 Process flow of an excimer laser dual damascene process

mer could incur shrinkage during cure up to 40 percent, which limits the feature sizes patterned by the photolithography. In the next step the traces are ablated into the polymer layer with the excimer laser. The ablation depth is set by the number of pulses. After trace ablation the mask is changed, and the vias are drilled by the laser. The tool allows high sub-micron alignment accuracy between the two mask layers. It is therefore not necessary to provide a larger capture pad size. After formation of the via and RDL, a seed layer is sputtered which consists of 100nm titanium adhesion layer and 400nm copper layer.

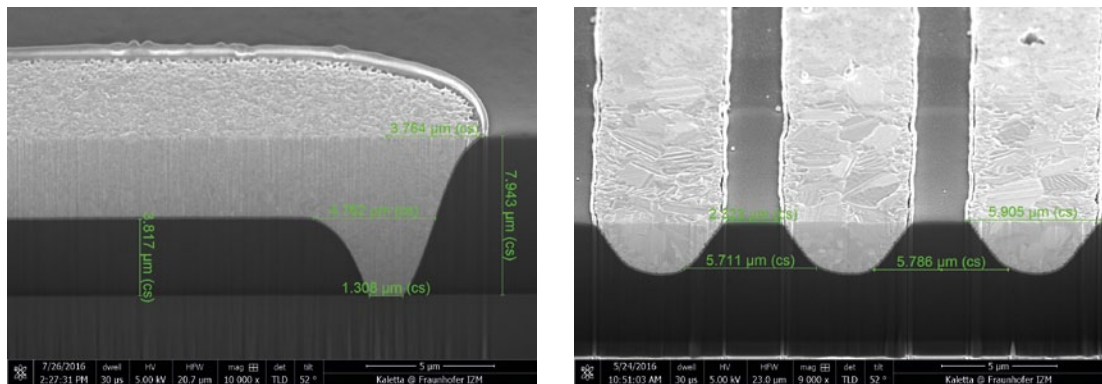


Figure 8 Laser ablated line and via in a low temperature cured polyimide layer (via first dual damascene was used on this case)

The structure is then filled by electro plated copper. The copper overburden is removed by a chemical and mechanical polishing step (CMP). Instead of a regular semi-additive process the copper structure height is not defined by the plating process. Therefore the copper thickness is independent of the local feature densities, feature size differences and galvanic bath flow conditions over the wafer. The copper CMP process stops on the titanium adhesion layer. The laser is then used instead of a second CMP step to remove the remaining thin titanium metal layer by a single laser pulse process. The seed layer removal by excimer laser is proven to be much faster than the CMP process. Figure 8 shows an excimer laser dual damascene structure of a 5 μm line and a 5 μm via without any misalignment. We have also demonstrated a dense routing of a 5 μm lines structure with a space of only 2 μm. The tita-

ni-um removal by laser shows no remaining metal parts even in small line spacing which will be very challenging to achieve for an SAP process. The seed layer removal has no effect on thicker copper trace lines. The successful isolation between dense lines was demonstrated by an inter-digital electrode structure where only a low leakage current below 10e-9A was measured. The test results demonstrated an excellent isolation between dense lines using the excimer laser enabled dual damascene process described above.

A thicker metal layer is not affected by the laser because the energy threshold for metal ablation is much higher than for the polymer. This means that the via ablation can land on any underlying metal layers without harming it or features underneath. Figure 9 shows FIB cuts of laser drilled vias which stops on a sputtered AlSi layer

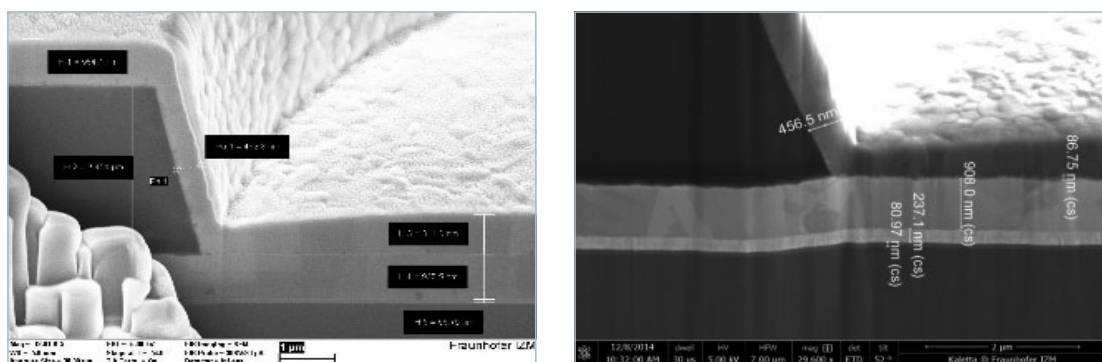


Figure 9 Laser-ablated polymer via landing on AlSi (left) and plated Cu (right) (20 μm Via CD, 650 mJ/cm²), Met 2: 1 μm sputtered AlSi

and on a plated copper layer. AlSi is a typical metallization for contact pads from CMOS chips where the plated copper layer is used for multi-redistribution layers. For the second metallization only a sputtered AlSi layer was used. There is no undercut or recess at the via opening edge which indicates that the laser made no interaction with the metal layer. The polymer in the via is completely removed which is shown by the clean interface between the metal layers.

For the evaluation of the yield, a daisy-chain design was set up which contains two metal lines. The line width is $5\mu\text{m}$ and the via diameter is also $5\mu\text{m}$. Each chain contains of 960 vias. The average resistance of a complete chain is in the range of 150 Ohms. Figure 10 shows a yield map of a 200mm wafer where the daisy-chains were ablated in a low temperature cured (230°C) polyimide which is commonly used for RDL generation on temperature sensitive re-configured wafers. Each green mark is a functional chain and a red mark indicates an open circuit in the chain. Therefore an excellent yield over the whole wafer is demonstrated. The defected chains at the edge are related to the edge bead removal of the polymer.

The excimer laser based dual damascene process flow is currently under evaluation for other polymers which are used for fine line routing of organic interposers like the non-photo dry film Ajinomoto Build-up Film ABF. First results are comparable to polyimide results. Figure 11 shows a cross cut of an embedded line in ABF.

CONCLUSION

The application of the PCB like laser ablation technology on a stepper like platform allows the fabrication of ultra-fine structures with high throughput. Features sizes of $5\mu\text{m}$ and below are demonstrated and show an excellent yield. There are many benefits from using excimer laser

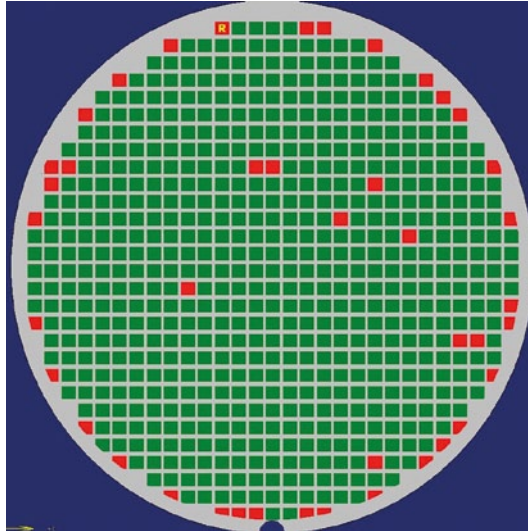


Figure 10 Daisy-chain yield over a 200 mm wafer

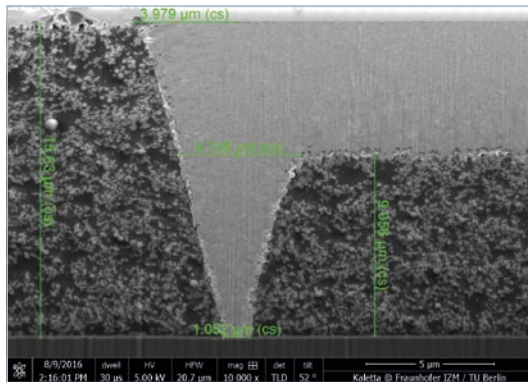


Figure 11 Excimer laser enabled dual damascene formation in ABF film

as compared to a regular lithographic structuring, such as the elimination of many process steps and consumables from the integration flow, the pattern integrity of the structuring ("What you see is what you get"), the ability to pattern ultra-fine vias and RDL, or the use of non-photo-definable materials that enable a wider option for CTE matching and are often cheaper. Therefore, the excimer laser enabled dual damascene process presents significant cost benefits compared to

the current process of record based lithography process flow. The excimer laser ablation enables users to reach the requirements for advanced packaging platforms where dense routing in combination with multi-layer build-ups are needed.

Acknowledgement

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Markus Woehrmann (born 1984) did graduated work on the material properties of polymers in packaging at the Technische Universität Berlin, and received the M.Sc. electrical engineering in 2010. Since 2010 he is working on electrical and mechanical property estimation of thin film layers at the Technische Universität Berlin in cooperation with the Fraunhofer Institute for Reliability and Microintegration (IZM). He is leading the glass interposer technology development at the Fraunhofer IZM since 2012 and he works in the group "Lithography and Thin Film Polymers" at the Fraunhofer IZM on the process development of RDL processing for Fan-Out Wafer-Level Packaging.





WAFFER-LEVEL PACKAGING USING HIGH FORCE BONDING OF AlGe

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ALUMINUM-GERMANIUM EUTECTIC WAFER BONDING

Aluminum-Germanium (AlGe) eutectic wafer bonding is the most widely used wafer-level packaging process for MEMS gyroscopes in high volume production today. The history behind its usage for wafer bonding dates back over 20 years. A patent describing the usage of an Aluminum-Germanium layer stack to bond two wafers together, no mention of MEMS though, was first filed in 1991 by G. Schuster, et. al. [1]. The first MEMS specific publication was by P. M. Zavracky in 1995 and the first mention of using an AlGe eutectic wafer bond process to electrically connect a MEMS inertial sensor wafer to an ASIC wafer can be found in a German patent application from 1995 by G. Flach et. al. [2-3]. One of the main advantages of AlGe compared to other eutectic wafer bond processes like Gold-Silicon (AuSi) is its compatibility with a standard in-house CMOS ASIC wafer fab or outside foundries like TSMC, Globalfoundries, X-Fab. No overly burdensome countermeasures and procedures to limit process line cross contamination need to be implemented. The eutectic point for AlGe has a melt temperature in the vicinity

of 690 K with an AlGe weight percent ratio of 48.4/51.6 according to literature [4]. This is about 60 K higher than the temperature of the AuSi eutectic point but not too high for having an ASIC compatible wafer bond process [5-7].

A eutectic alloy is sometimes called a “solder” however, this is not necessarily the correct metallurgical term. A eutectic alloy is a two component alloy that undergoes a direct solid to liquid phase temperature at a specific composition and temperature.

The composition and temperature define the reaction and are unique to only a few materials systems. Table 1 shows the alloys most often used for wafer-level bonding. The choices are alloys of gold, aluminum or copper since these materials are already used in semiconductor fabrication labs and in most cases have established processing and deposition methods.

Eutectic Alloy	Eutectic Composition	Eutectic Temp
Al-Ge	49/51 wt%	419° C
Au-Ge	28/72 wt%	361° C
Au-In	0.6/99.4 wt%	156° C
Au-Si	97.1/2.9 wt%	363° C
Au-Sn	80./20 wt%	280° C
Cu-Sn	5/95 wt%	231° C

Table 1 Eutectic alloy commonly used in MEMS wafer-level packaging

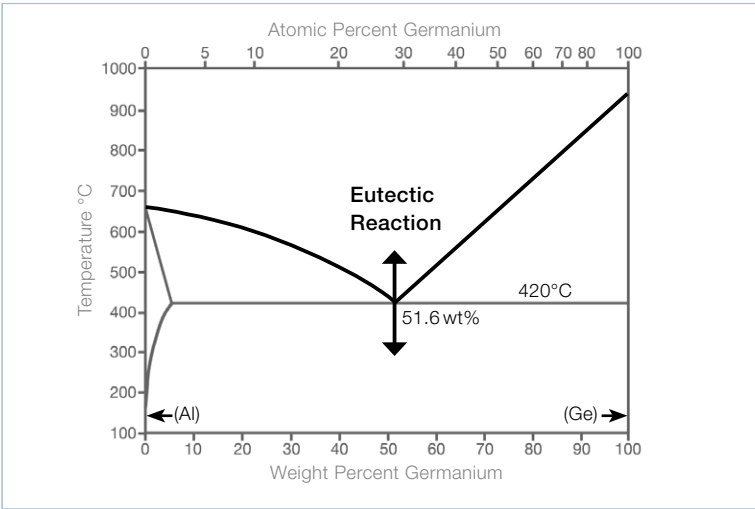


Figure 1 Aluminum-germanium phase diagram showing simple eutectic reaction at 51.6 wt% Ge and at 420° C

Figure 1 is the AlGe phase diagram.[7] This is a simple eutectic phase diagram with no intermetallic phase formation. The aluminum has a melting point of 660° C and germanium melts at 938° C. The eutectic reaction is at 51.6 wt % Ge and has a solid to liquid transition (eutectic point) at 420° C. In most eutectic bonding applications the rule of thumb is to remain at 7-15° C above the eutectic temperature.

Going to higher temperatures will increase the fluidity of the alloy and can lead to excess flow into unwanted regions in the die. However, if the temperature is not uniform the viscosity of the melt will vary. Some areas on the wafer may be solid and others liquid and the wafers will crack under the applied force as bending moments develop in regions with varying compliance.

METAL DEPOSITION

Ge can be deposited as an alloy layer on both sides of the interface then the wafers are simply aligned, brought into a contact and pressed together. After contact is established the wafers are heated to the eutectic temperature, melted and re-solidified. Alloys can be deposited by sputtering of alloy targets or electroplated in some but not necessarily all cases. The advantage of the direct melting of alloy layers is speed because the diffusion step can be avoided. Alternatively the aluminum can be deposited on one wafer and the germanium on the other substrate. Then the wafers are pressed together and heated (below 420° C) until the interface mixes. Note that limited solid solubility means that the diffusion is only a few percent and grain boundary reactions will play a major role in the success or failure of the bonds when completed with this strategy. After mixing the material the wafers are reflowed and cooled.

After eutectic bonds are cooled there is a possibility that microvoids form in the eutectic microstructure. These voids may be due to the Kirkendall effect which occurs when one element diffuses more quickly than the other and the lattice sites left behind are empty. Or rather then are filled with vacancies. If a substantial vacancy concentration exists then the vacancies can cluster and lead to microvoiding. In most cases this can be overcome by adjusting the cooling rates and the amount of hyper eutectic heating.⁽⁷⁾

CONVENTIONAL SURFACE PREPARATION

The goal of seal surface preparation before bond is to minimize the amount of surface oxides and other contaminants negatively impacting the wafer bond result as well as the process stability. Depending on the exact seal metal layer stack configuration, one has to prepare either Aluminum, Germanium or both types of surfaces. Germanium forms mainly Germanium-dioxide (GeO₂) with a suboxide layer (GeO_x, $x < 2$)^[8]. The GeO₂ is water soluble, whereas the suboxide is not^[8]. A dip in HF with a sufficiently long DI water rinse afterwards enables also the removal of the suboxide layer^[8]. The wafers should be stored under Nitrogen in the bond wait queue to prolong the time until the native oxide reforms. It has been reported that using a HBr based etchant and Nitrogen storage reformation of the native oxide layer on Germanium can be inhibited up to 24 hours^[8]. Aluminum forms a hard native oxide layer up to several nanometers thick. One documented solution is using a Hydrogen containing gas mixture and try to reduce the oxide in-situ during the wafer bond process. The efficiency of the process in the available temperature range is undocumented though^[5]. Another possibility to deal with the native oxide layer on Aluminum is by using brute bond force to break thru the passivation layer. Published bond recipes for AlGe therefore usually mention bond forces in the 40-60 kN range, the exact amount of seal area per wafer and therefore the actual pressure on the seal area is rarely documented though^[7-8]. A further process option to remove the native Alumina layer is using a reduced pressure Argon plasma before bonding to remove the oxide using an ion milling/Argon sputtering process.

HIGH FORCE BONDING

Based on the assumption that high force should be able to break through and enable normal AlGe eutectic seal formation, a DOE based on process of record recipe was set-up to test the hypothesis on eutectic bond short loop wafers. Wafer bonding was accomplished using a SUSS MicroTec XB8 high force bonder with improved bond force uniformity compared to the previous generation and a maximum bond force of 100kN. Another change from the previous tool generation is the dual zone heating configuration enabling better control of the temperature distribution within the bond chuck.

Bond	Bond force	Bond result
B01	20 kN	OK
B02	100 kN	OK

Table 2 High force bond

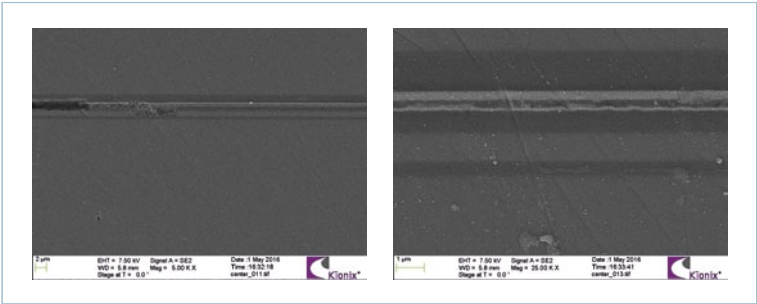


Figure 4 XB8 bonded AlGe structures, 274 nm thickness of eutectic layer @ 100 kN

Capshear / kgf	Sample 1 XB8	Sample 2 XB8	Reference @ 20 kN
Average	5,34	5,09	4,03
Min	4,77	4,27	2,84
Max	5,99	5,83	5,13
stdev	0,35	0,37	0,69

Table 3 Capshear testing, comparison XB8 and reference bonded AlGe structures



Figure 2 SUSS MicroTec XB8 semi-automated permanent bonder

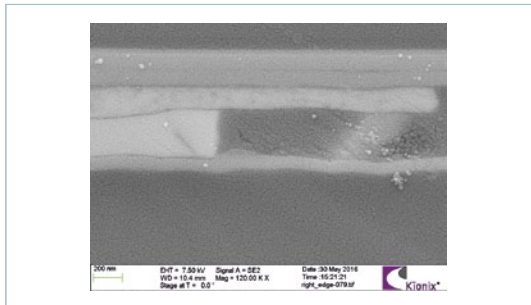


Figure 3 Close up of AlGe eutectic mixture

RESULTS

The wafers were successfully bonded in a void free fashion. Figure 3 and 4 show cross section pictures of the bonded wafers. Where 20kN were applied as a reference bond which shows a thickness of the eutectic layer of 563 nm. Using the 100kN bonding force in the recipe a thickness layer of 274 nm could be achieved. Metal squishing into scribe line could not been observed. Also the SAM with 5µm resolution shows no voids or microvoids. The post bond wafer bow is in the range of only 100 to 150µm, which is a very good result as all bonded wafer pairs tend to result in a higher wafer bow due to the different cooling effects in the bonder. Shear strength is slightly better compared to 20 kN (table 3) and SEM cross-sections show very good contact on all chips across the wafer with 100 kN recipe.

Results summary:

- Median capshear strength shows a dependency on the applied bond force
- Larger bond force leads to an increased capshear strength
- Dependency between capshear strength and bond force is non-linear (Figure 5)

CONCLUSION

The AlGe high force bonding shows an increased capshear strength, which is caused by the increased bond force and resulting in thinner eutectic metal layers. The uniformity of the bonded structures over the wafer leads to a higher yield. The new heater design with its double side air cooling, with special thermal isolation and flange cooling, leads also to a better post bond bow of the bonded wafers. In summary one can say the new features lead to a high yield due to the homogeneity of the temperature and bonding force distribution in the XB8.

In general for device manufacturers the key motivation to transition to metal based wafer-level bonding is the increased hermeticity which improves device functionality but more importantly enables the continued scaling of the device to smaller sizes. But it also needs a better temperature and bond force homogeneity in the bond equipment itself.

The economic and technological advantages of metal bonding in MEMS wafer-level packaging are clear and these methods will continue to increase in use as market became more consumer oriented and integration with other components increases.

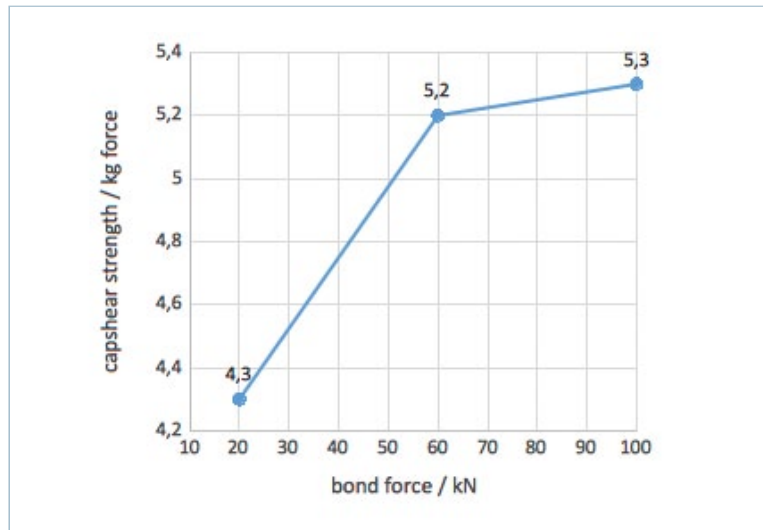


Figure 5 Capshear strength as a function of bond force

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CONTOUR MOVE – EDGE COATING AND EDGE STRIPPING OF WAFER FLATS

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Common issues when processing 150mm and smaller wafer sizes for the semiconductor and especially MEMS market are arising from the wafer flat(s). Today's demand for maximizing the used area on a wafer requires a technique to perform an edge bead removal (EBR) not only at the round areas of a wafer but also on the wafer flat. In MEMS processes often a technology is required to protect the wafer edge against etching agents – this is where edge coating comes into play, that also needs to be applied not only at the round areas on the wafer, but also on the straight edge of the wafer flat. SUSS MicroTec's "Contour Move" option addresses these challenges and has gained considerable demand in the MEMS and optical components market. Its potential is growing as it offers a solution to many fabrication problems.

WAFER FLATS AND THEIR CHALLENGES

Wafers of 150mm in diameter and below have a flat instead of a round edge. When a wafer is spin coated, the resist on the substrate builds up at the edge, at the round part as well as on the flat. This is what we call the edge bead. It has many disadvantages:

- 1) It can contaminate chrome masks during exposure
- 2) It prevents clamping of the wafer during subsequent electroplating
- 3) It can increase developing time,
- 4) It prevents good contact between mask and wafer
- 5) It sometimes causes wafers to break during subsequent processes

Traditionally the edge bead is removed by a stream of solvent directed at the wafer edge, while the wafer is rotating. The nozzle applying the solvent is fixed in its position, which does not change during the process. Thereby the stream can remove all the excess resist at the edge, but not at the flat. The flat still remains covered by the edge bead.

EDGE BEAD REMOVAL (EBR) AT THE WAFER FLAT

In currently used approaches, the wafer remains static and does not rotate. The nozzle sweeps over the wafer flat using a linear motion. This linear motion arises some drawbacks. The first disadvantage of a static non-rotating wafer is the lack of centrifugal forces. Thereby the solvent creeps away from the edge, preventing a clean coating. This problem can be mitigated by applying an additional air stream, but the air stream is not applicable with all resists and it can even cause more edge bead build-up and extreme contamination of the process bowl. In addition, special hardware is often required and the process cannot be performed in a standard coater module.

FLAT EBR WITH CONTOUR MOVE

With the contour move option, the wafer is not static during the flat EBR process. It keeps rotating like during a standard EBR process. In addition, the standard EBR nozzle is used for the special procedure. At the point where the flat starts passing the EBR nozzle, the arm moves towards the wafer center while the nozzle is dispensing, as seen in Figure 1. This inwards movement is carried out until the nozzle hits the center of the flat. Consequently, the arm changes the moving direction and starts moving outwards to its starting position. Because the EBR nozzle position follows the flat, the complete edge can be stripped, while the wafer is rotating.

Timing, dispense arm acceleration and positioning as well as spin speed parameters must be under close control to achieve the presented results. The first challenge is performing a dispense arm movement at the right point in time;

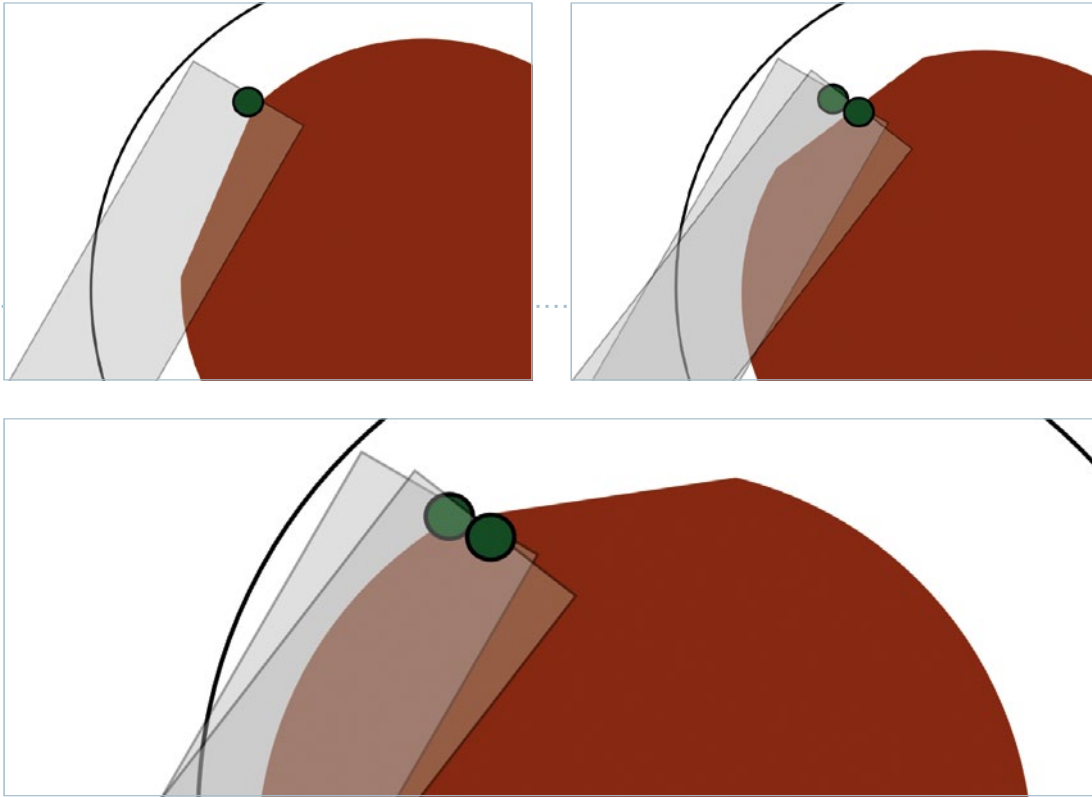


Figure 1 Demonstration of the working method of the contour move; first the wafer is rotated until it reaches the point of impact of the solvent stream. At that moment the arm swings towards the center of the wafer. When the point of impact reaches the center of the flat, the arm swings back to the initial position

especially when the wafer is rotating at high speed. As mentioned the high rotation speed is necessary in order to utilize the centrifugal forces and prevent solvent from creeping into the resist. This means the movement of the arm has to be quick and accurate enough to perform the desired task. However, the time the EBR nozzle is at the wafer flat is minimal as it is inverse, proportional to spin speed, as illustrated in Figure 2. Meaning, with higher rpm the timing of the arm movements becomes critical. For example: for a spin speed of 10rpm, 100rpm and 1000rpm the complete inwards/outwards movement must be carried out within 0.787 s, 0.0787 s and 0.00787 s respectively. Hardware and controller software were optimized for this task.

Another challenge that arises with high spin speed is the timing. With increasing the spin speed, it is critical to start the arm movement at the right point in time. Meeting the exact time to

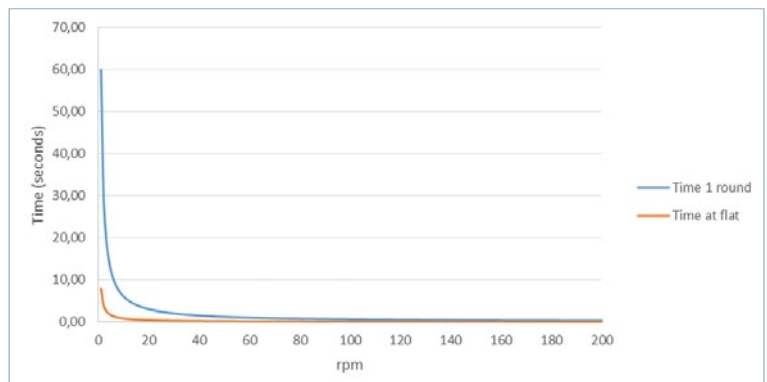


Figure 2 Time required for one round of the wafer (blue line) and time required for the flat (orange line) over the spin speed. The diagram illustrates the short times available to perform the edge bead removal at the wafer flat

start the inward/outward movement becomes critical. A millisecond lag in time can result in (or lead into) a huge difference in the performance of the system.

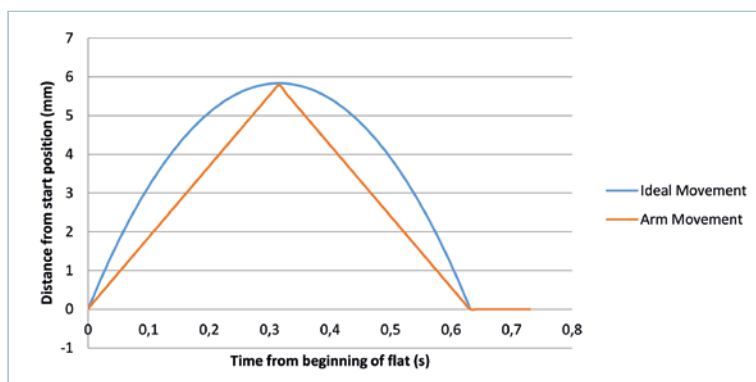


Figure 3 Typical arm movement (orange line) and ideal movement to ensure parallelism (blue line)

The main challenge is getting a parallel movement of the EBR nozzle relatively to the wafer flat. The arm is mounted to a stepper motor, which commonly performs the motion profile linearly: it accelerates to the desired speed, keeps the speed, brakes and accelerates into the opposite direction, as illustrated in Figure 3 (orange line). In order to be parallel to the flat the arm needs to do a circular motion as also shown in Figure 3 (blue line). The linear motion of the motor is far different than the ideal movement, which the arm has to take. Thereby the arms speed profile is tweaked in order to ensure the parallel movement to the wafer flat.

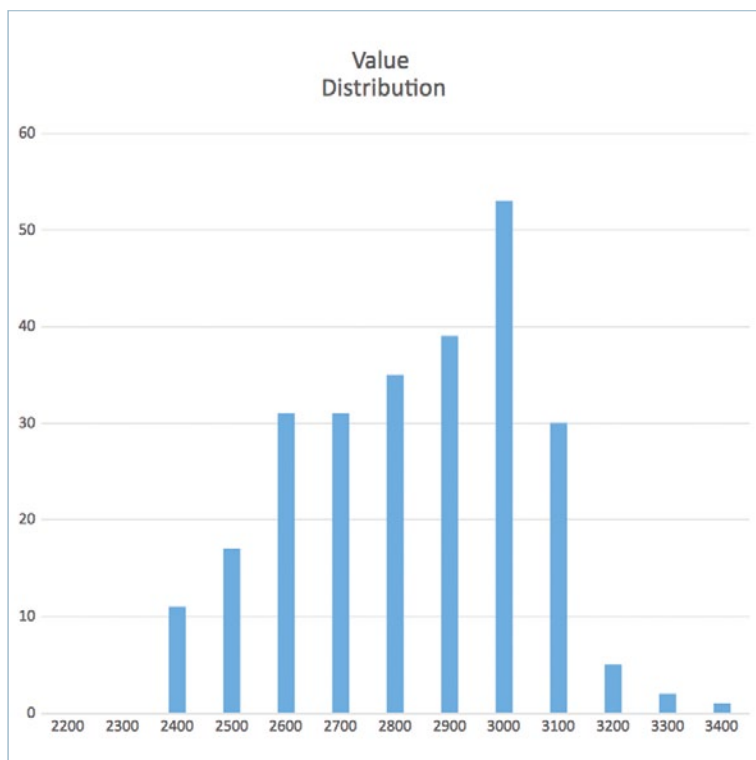


Figure 4 Histogram showing the repeatability of the system over 240 measurement points

RESULTS

The contour move feature ensures good repeatability and accuracy at high speed. The EBR profile can be adjusted to several flat sizes, from 3 inch to 150mm wafers. Within a wafer, the deviation of the values can reach down to 400 μm . As for process capability and repeatability, Figure 4 shows results of 240 measurement points. All data values are within 1 mm. These results meet and exceed the requirements of several applications in the field and have proven good performance. Figure 5 shows adge bead removal at the flat with a width below 2 mm.

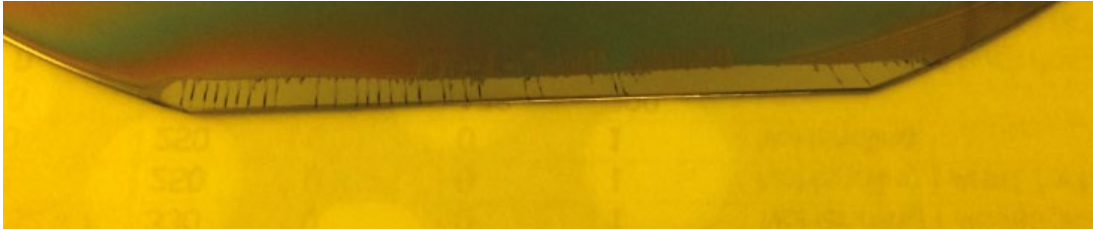


Figure 5 Edge bead removal at the wafer flat for a resist with 5 μm thickness

EDGE COATING WITH CONTOUR MOVE

The contour move system is designed to follow the wafer flat. It is not only capable to remove resist from the flat, it can also cover the flat of the wafer with a protection layer. This is desired when deep etching is performed to the wafer. The deep etching could attack the edges, which in turn has consequences to subsequent processes. The two modes, edge removal and coating, can be integrated easily in one module and can be used consequently without any mechanical change over. The edge coating is slightly different from edge stripping. The thickness of the resist is determined by the flow of the resist and the spin speed. For edge coating, the dispense method is crucial in achieving the same coating width throughout the wafer flat, as seen in Figure 6. A standard deviation of only 0.16 mm over a lot of 25 wafers was achieved. The results are shown in Figure 7.

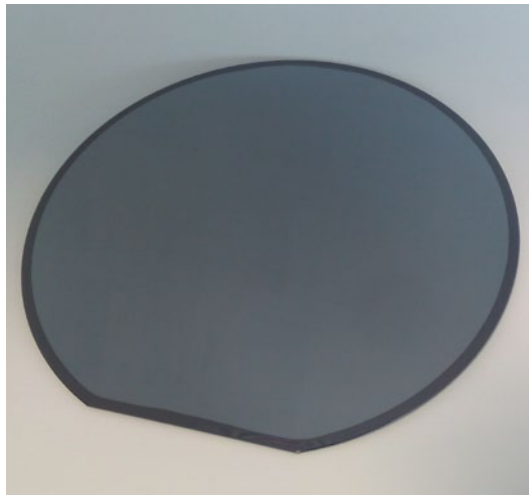


Figure 6 Wafer coated with a protection layer using contour move

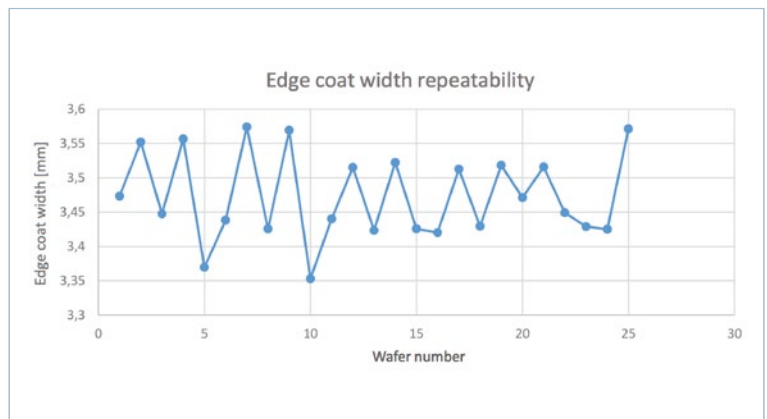


Figure 7 Edge coat width repeatability over a lot of 25 wafers. The standard deviation is 0.16 mm

BACK SIDE COATING WITH CONTOUR MOVE

Coating the edge with conventional methods is often not enough as a protection against e.g. etching agents. The edge is rounded and the coating only covers the top part. The backside of the edge remains uncovered and unprotected. Therefore a method was developed that can perform an edge coat at the backside of the wafer, including the flat, without the need of flipping the wafer. Results can be seen in Figure 8 and Figure 9.

CONCLUSION

Contour move is a versatile method that can perform edge stripping, as well as top- and back-side edge coating. The reproducibility of the system lies within a 3sigma of 1.5mm for edge stripping and 1 mm for edge coating. Further improvements are expected over time as the technology is continuously optimizing for higher accuracy and repeatability.

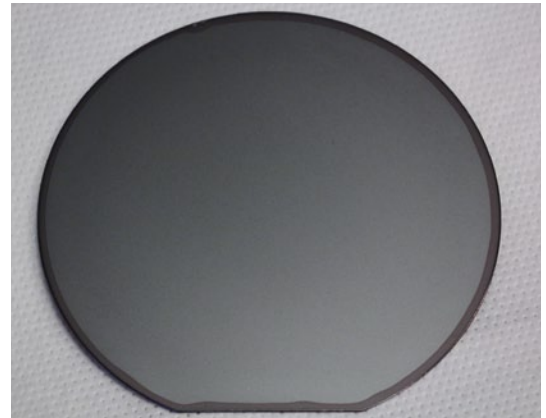


Figure 8 Backside of a wafer with edge coated without flipping the wafer

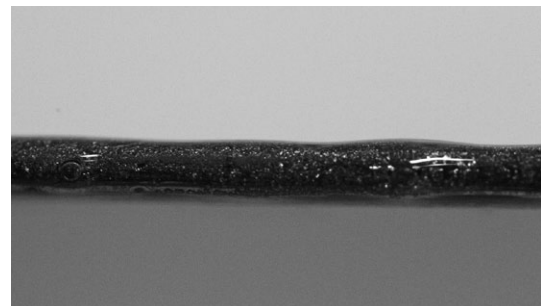
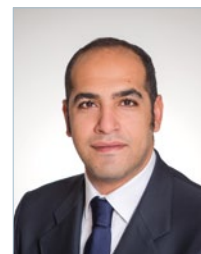
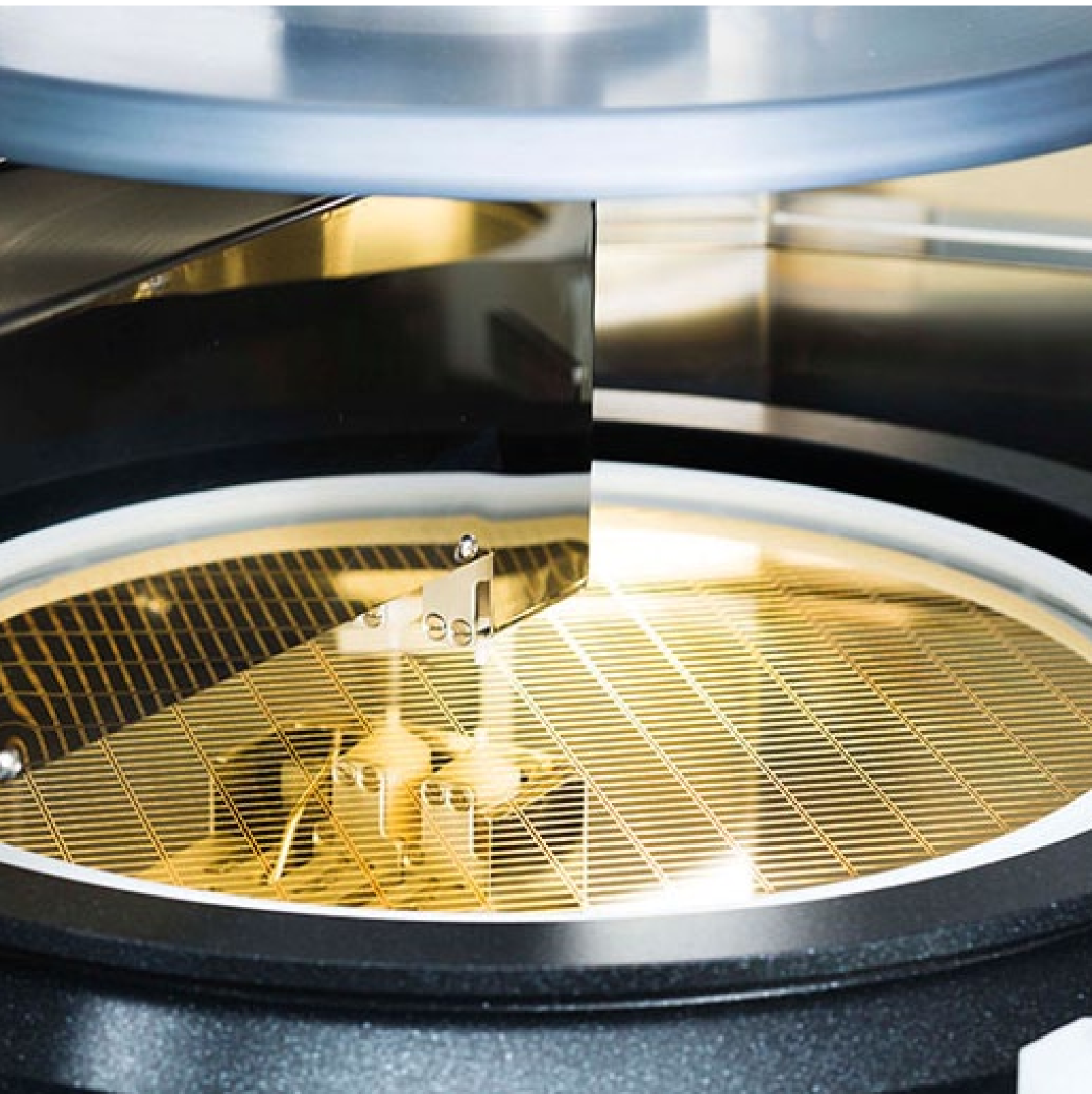


Figure 9 Side view of a wafer edge coated on top and backside to ensure complete coverage of the edge curve

Dr. Omar Fakhr graduated in 2006 from the Technische Universität München in Electrical Engineering with focus on semiconductor device fabrication and nanotechnology. At the age of 28 he earned his PhD degree, where he designed and tested new methods for the fabrication of nanometer sized structures. He joined SUSS MicroTec in 2011 as an application engineer for spin coating systems. During that time he has installed numerous machines at customers worldwide and conducted jointed research with renowned institutes. Since 2014 he is an application scientist responsible for spin coating, nanoimprinting and laser imaging systems.





WAFER SCHEDULING ALGORITHMS – DECISION ON THE FLY WITH DYNAMIC INPUT PARAMETERS

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In a previous SUSS report (V2 11/2014) the basic scheduling algorithms used in automated SUSS coating and developing tools were introduced. The different strengths and drawbacks of fixed sequential handling and dynamic handling, at SUSS MicroTec named *cyclic mode* and *decision on the fly* (DOF) mode, respectively, were discussed. While the cyclic scheduling mode ensures constant handling conditions over a process sequence, it is not optimized to run different process sequences in parallel. In addition, it cannot adapt to changing conditions in a tool. The DOF mode is by its different approach always reacting to the current situation, which makes it the preferred scheduling mode when adapting to varying tool conditions.

In this article, further improvements and optimizations to the DOF mode are presented and discussed. In particular, predictive measures are added to the scheduling algorithm to adapt to varying input conditions. This especially addresses e.g. overbaking issues in hotplates if manual parameters are not set correctly.

INPUT DELAY

A process sequence typically consists of several modules in which a substrate needs to be processed. An example coating sequence can be (process times in brackets):
cassette → coater (60 s) → hotplate (45 s) → coolplate (45 s) → cassette.

In this example, every module shall only be used once. The coater module is clearly the bottleneck

in the sequence as it has the longest process time. A new wafer needs to leave the cassette about every 60 s, which is self-regulating as the bottleneck is the first module in the sequence: the coater will be unloaded about every 60 s, ready to receive the next substrate. In this simple example, no overbaking errors are expected, as all process modules downstream have shorter process times.

Looking at another example sequence with a dehydration step added before the coating: cassette → hotplate (45 s) → coolplate (45 s) → coater (60 s) → hotplate (45 s) → coolplate (45 s) → cassette.

In this case if not restricted by any means, the first wafers will leave the cassette every 45 s. This leads to a situation where the substrates are kind of “backing up” upstream the coater module. The wafer in the first coolplate will have to wait for 15 s before it can be handled to the coater. As that coolplate is blocked, also the wafer in the first hotplate has to stay 15 s longer than needed. Up to now, this condition was prevented by programming a so-called “input delay” parameter. In the case just discussed, an input delay of 60 s would lead to wait another 15 s after a wafer left the first hotplate before letting in a new wafer from the cassette. As a result, the wafers would be ready just in time for the next module.

DYNAMIC INPUT DELAY

For simple process sequences as described above, the manual adjustment of the input delay time is a viable approach. However, when addressing complex sequences, finding the right parameter is sometimes not easy and experience is needed to find the right balance between a high enough input delay to prevent overbaking errors and a low enough input delay to avoid an artificial bottleneck that decreases the tool throughput. E.g. the assumption of only single modules is greatly simplified. Usually, multiple coater modules, hot- and cool-plates are used in a sequence to utilize the given hardware in an

optimal way. Typically, additional tasks put extra load on the modules:

- Other sequences run in parallel, and a resource is shared between those two sequences.
- Cleaning recipes are running from time to time in the module.
- Single modules might be down for maintenance influencing the manually set input delay to be suboptimal.

All these added delays might not directly lead to e.g. an overbaking error but can add up over time.

The new approach of dynamically calculating the input delay addresses these influencing parameters. Based on monitoring all relevant modules as well as all substrates in the system and their expected finishing times in the single modules, the input delay is continuously recalculated and corrected if necessary. This allows the scheduler to self-adapt to changing tool conditions and even unexpected events are addressed properly.

HANDLING PRIORITIES

The decision on the fly (DOF) scheduler from SUSS MicroTec constantly monitors the process situation and decides on what operation can be carried out next. The handlings are scheduled on a first-come, first-serve basis. As sometimes several handlings are possible at the same point in time and the first one on the list is not necessarily the most important one, the so-called “handling priority” was introduced in the past. By this parameter, the handling priority of a module can be set higher, although it might be further down on the handling list. A typical candidate for high handling priorities are hotplates, as too long times of coated wafers in a hot condition might damage the substrate. In an example case a coater would have the handling priority “0” (standard) and a hotplate the priority “100”. In case the recipes on both modules were successfully finished and the substrates are ready to be handled to the next module, the hotplate would be unloaded first.

DYNAMIC HANDLING PRIORITIES

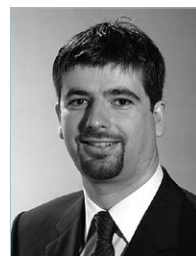
The recently introduced dynamic handling priority further improves the scheduling procedure. An additional priority layer that also takes already advanced idle times into consideration is added to the algorithm. If the idle time of a substrate is approaching the maximum time before damage value, the handling priority will be dynamically set higher. This makes sure that e.g. a wafer in a hotplate that is closest to the overbaking time is handled with the highest priority. The new scheduling algorithm holds back handlings that can be carried out immediately and waits for a substrate that is e.g. ready to be handled in 1 s if that one is close before being damaged by overbaking.

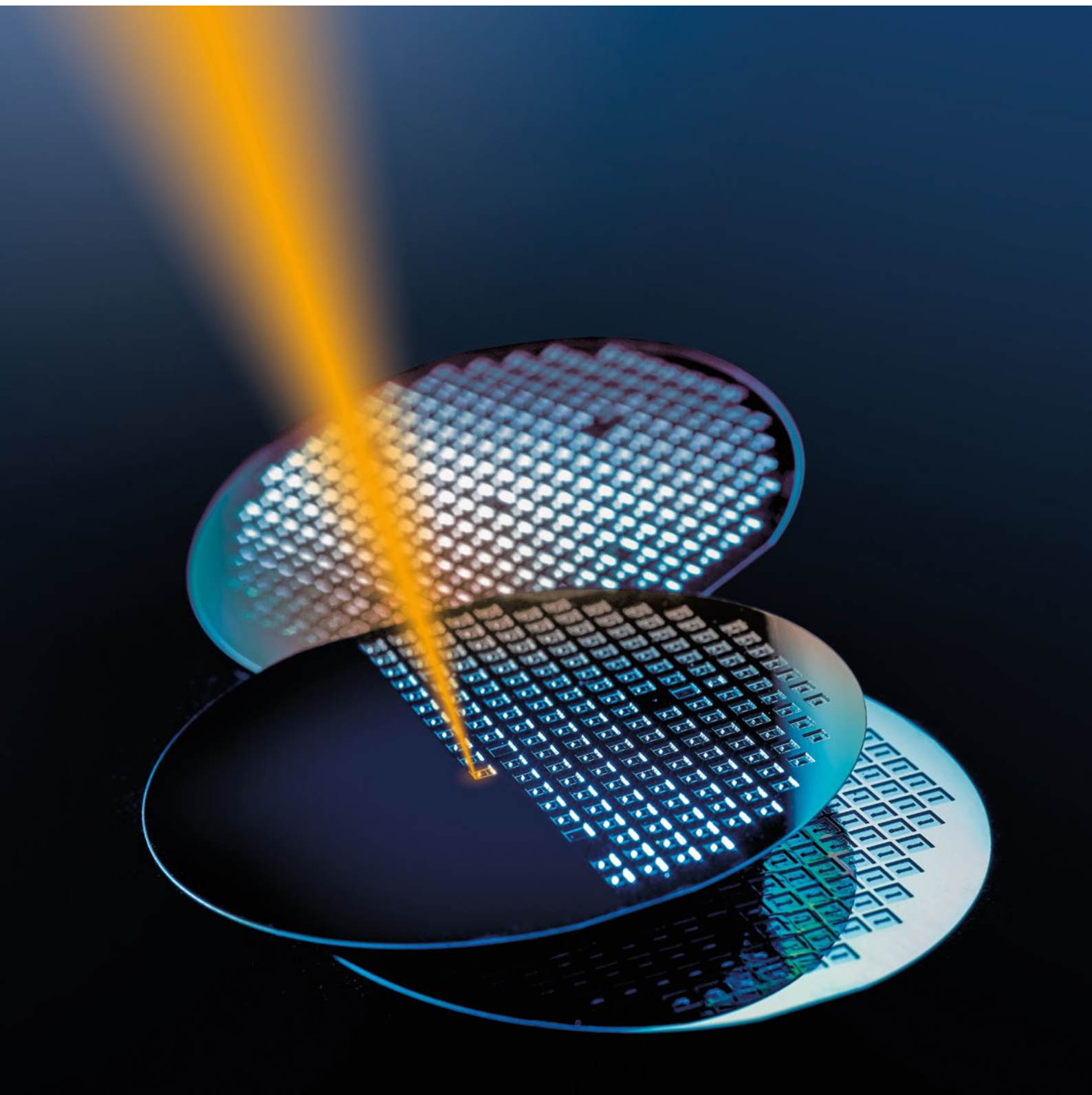
SUMMARY

For improved process stability and tool throughput, SUSS introduced two scheduling innovations. The dynamic input delay and dynamic handling priority parameters are constantly recalculated and adapted to the current tool status.

We at SUSS MicroTec continuously refine our scheduling algorithms. This ensures that the hardware of a SUSS tool is used in the most efficient way possible. Smart and intelligent scheduling algorithms increase the usability of a tool, improve its throughput and process performance without adding additional hardware – leading to the best possible cost of ownership and performance.

Thomas Grund studied mechanical engineering with a specialization in microsystems technology at the Technical University of Karlsruhe. For his work on batch integration technologies for hybrid microsystems he earned a PhD degree from the Karlsruhe Institute of Technology (KIT) in 2010. Afterwards, Thomas Grund became project manager for an application of deep X-ray lithography at the KIT. He joined SUSS MicroTec at the beginning of 2012 as Product Manager Coater/Developer Systems.





SUSS LI SERIES: DIRECT LASER WRITING TECHNOLOGY FOR FAST PROTOTYPING IN ACADEMIC AND INDUSTRIAL R&D

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Artwork generation by laser direct writing on resist is a highly versatile complement to traditional mask-based lithography. This technology results also particularly cost effective when fast turnaround must be achieved in research activities and small productions.

The Laser Imager addresses a wide range of applications, such as microelectronics, micro-fluidics, diffractive optics, MEMS, conformal micro-patterning, microwave integrated circuits (MICs), and graphene and nanotube technology.

In R&D, for example, the LI Series equipment stands for flexibility and ease of use, resulting in a key enabling technology for the fastest optimization of all research processes. Due to the combination of its optical apparatus and its high precision stage movement controls, the same tool can be used first to produce a pattern and then for inspecting the results. The system transforms a laser beam into a controlled writing tool, reaching a sub-micrometric resolution over large areas.

Particularly effective is the use of direct laser writing technology within a complete process transfer from product optimization to high volume production. The layout of a micro-electronic device, for example, can be quickly optimized by modifying a software mask (i.e. a CAD file) for directly writing onto a resist coated substrate using the SUSS Laser Imager. Once the layout of the device is finalized, the same LI equipment can be used to produce the photolithography mask to then transfer the complete lithographic process to the high through-put mask aligners.

For micro-optics, laser writing, with its grey-scale lithography capability, ideally complements the manufacturing processes of optical devices. This technology allows for the definition of high-quality masters from whom micro-lenses and diffractive optical elements can be effectively replicated.

When employed in micro-parts fabrication, the extensive customization possibilities of the SUSS LI tools offers the option to include additional laser sources, with wavelengths tailored to specific process requirements. For example, a second 375 nm laser would allow the effective patterning of thick layers such as SU-8 resists, typically for fabricating high-quality micro-mechanical parts, for example in the watch industry.

The new Laser Imager from SUSS MicroTec is a versatile direct writing tool with a cost/performance ratio optimized for each specific application. In this view, each unit is unique, including a combination of standard and customized features matching the requirements of the user in R&D activities or specialty industrial productions.

TECHNOLOGY AND FEATURES

Laser direct imaging is based on the possibility of exposing a photoresist film, deposited on a substrate, by means of focalized laser radiation and defining the desired pattern by moving the focus spot and the substrate in a variety of write modes, allowing the user to select the patterning strategy best suited for each specific design.

Besides the possibility of selecting among different write modes, a host of other features makes up the unique capabilities of the Laser Imager.

- **Surface tracking:** the laser spot can follow and remain in focus on the substrate surface even if this is slightly concave, convex or uneven. The focusing system exerts no pressure on the substrate, allowing patterning on delicate substrates like thin free-standing membranes or soft samples. The laser writing process can be performed also on slightly tilted substrates (max 2 degrees).

This characteristic is especially useful if small samples with non-parallel surfaces are used, or when they are glued on a larger carrier plate.

No dead area: the laser beam can pattern substrates of any size and shape, remaining in focus up to their edges. This feature is especially useful in R&D activities if small chips or irregularly shaped samples are used.

- **Wide selection of minimum linewidth and patterning speeds:** by simple mouse clicks, the user can define the minimum laser spot size used for patterning (from submicron to 8 μm) and the positioning resolution for each pattern element (from 0.1 μm to 2 μm). Furthermore, the automatic lens exchanger allows the user to select in a few seconds the most suited resolution for each specific part of the layout, optimizing system through-put.
- **Possibility of hosting one or two lasers for micro-lithography.** Normally, a 405 nm laser is installed, corresponding to the h-line of the mercury lamp used in mask aligners. This gives the tool a full compatibility with the most popular photoresists used in traditional micro-lithography. But a 375 nm laser can be added, well suited for thick SU8 resist or other thick UV-sensitive photo-polymers. Of course, wavelength selection requires only a mouse click. It is also possible to host **an additional laser source for surface processing or micro-ablation.** A nano-, pico-, or femto-second laser can be installed in addition to 405/375 nm lasers, making the Laser Imager a unique combined tool for both micro-lithography and laser processing.
- **Bottom-side alignment capability:** an optional back-side microscope, combined with a chuck adapter, allows also for back-to-front pattern alignment.

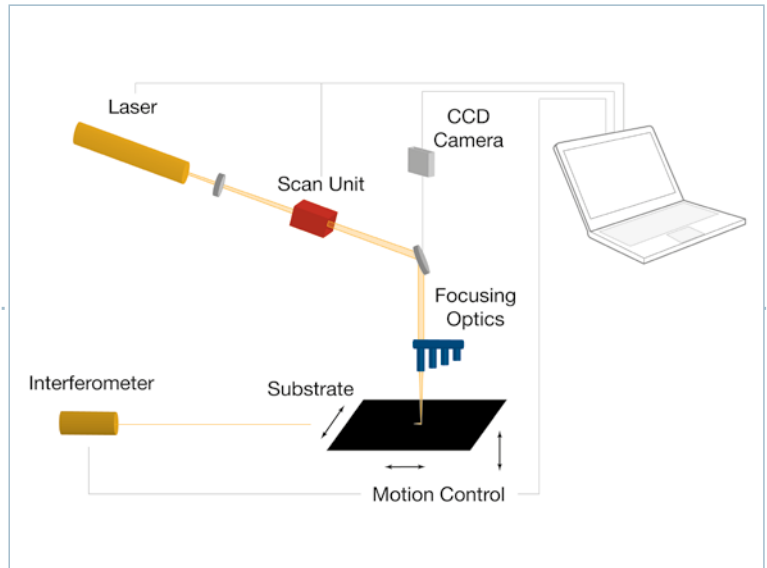


Figure 1 Sketch of the SUSS LI equipment: the laser beam, after passing through the scan unit, is scanned on the substrate surface via a set of focusing lenses capable of achieving different resolutions. At the same time, the XYZ stage is moved synchronously with the scanned beam. In the **Pro Series** an additional interferometer allows for submicron control of the relative position between beam spot and substrate

- **Extremely long lifetime for the 405/375 laser sources.** These are directly modulated (no acousto-optic modulator) and have a practically infinite lifetime (a warranty of 4 years is given for the laser sources).
- **Fully customizable substrate chucks,** capable to host samples of any size and shape, with thickness up to 10 mm.
- **Wide range of resist thickness,** from 0.3 to 100 μm . Therefore, the same tool can be used for ultrafine submicron patterns on thin resist (e.g. for micro-electronics, micro-optics) as well as in low resolution applications on thick resist (e.g. for microwave circuits, PCB, solar cells, MEMs, micro-fluidics). The user can also set the beam focus above or below the resist surface, for controlling the *sidewall* shape.
- **Possibility of surface photoluminescence mapping,** with 405/375 nm pump wavelength.

With its particularly compact footprint and the minimal requirements posed on the cleanroom infrastructures (no compressed air required, no air cooling duct, no water), those tools are an optimal fit for any laboratory.

The unique capabilities listed above are complementary to a number of other traditional features that the user may expect in an advanced pattern generator:

- Multilayer patterning, with manual/automatic top-side overlay alignment.
- Videomicroscopy and surface metrology.
- Grey level lithography.
- Simple and intuitive Windows™ user interface.
- Minimum or null maintenance.

TOOL DESCRIPTION

The Laser Imager is composed of three parts: the Write Unit (with dual beam XY laser interferometer in the *Pro* versions), the Control Unit and the powerful PhotonSteer control software.

As mentioned above, the Write Unit hosts normally a 405nm laser (60 or 200mW) for general purpose lithography. An additional 375nm laser (50mW) can be included, as well as another laser for surface microprocessing.

A large choice of write areas is available, from 2"x2" to 13"x13", with an allowed substrate size at least 2" wider than the write area.

Substrate motion is achieved through a XY stage equipped with state-of-the-art linear motors having 10nm resolution and a Z stage with 100nm resolution. If the laser beam is kept still, the XY motion system provides for defining the trajectories of the focused spot on the substrate surface. This corresponds to **stage-scan**, **vector** and **contour** modes. Such modes are well suited for patterning long straight or curved lines or for specific applications (photochemistry, trimming, etc.). Any linear XY stage movement can be programmed, with position-synchronized beam on/off and a maximum drawing speed of 10 mm/s.

But in most applications, with generic complex and dense patterns, the default **beam-scan** mode is used: the whole pattern is converted into a bitmap image and divided into parallel strips. The laser beam is scanned on the substrate while this moves along each strip (Y direction), orthogonal to the scanning direction (X). The bitmap pattern is obtained by modulating the beam during each scan. After completing one strip, the stages move to the beginning of the next strip and the process is repeated. All strips are precisely aligned to each other, with no visible stitching error between adjacent strips, thanks to a proprietary **zero-stitch technology** used in the tool. The surface patterning speed in beam-scan mode depends on the resolution set by the operator, and can range from 5 mm²/min to 160 mm²/min.

In all LI systems, XY metrology relies on state-of-the-art optical encoders embedded in the linear motors, with an absolute positioning precision around 1/10000 of the motion value. For



Figure 2 The SUSS LI8 Pro model: The Write Unit contains the laser source(s), the chuck for the different substrates, and the XYZ stages that move the substrate under the focused laser beam. A rack cabinet contains the Control Unit

	LI2	LI4	LI6	LI8	LI6 Pro	LI8 Pro	LI12 Pro
Substrate Size	100x100mm	150x150mm	200x200mm	250x250mm	200x200mm	250x250mm	350x350mm
Write Area	50x50mm	100x100mm	150x150mm	200x200mm	150x150mm	200x200mm	300x300mm
Autofocus and Surface Track	No		yes				
Setup	TableTop		Stand Alone				
# Focusing Optics	2		4				
Automated Lens Exchanger	No		Yes				
Auto Multilayer Alignment	No		Optional		Yes		
Double Write Speed	No		Optional		Yes		
Laser Interferometer	No				Yes		

Figure 3 Summary table of the different models in the SUSS LI Series and of their main characteristics

more demanding application and for achieving low sensitivity to environmental temperature variations, the **LI Pro** range of Imagers is recommended. All LI Pro tools are equipped with dual-beam XY laser interferometer, in addition to the embedded optical encoders, and guarantee submicron positioning precision over the full motion range.

All Imagers include substrate video monitoring through the focusing objective, with red light illumination, image averaging, frame grabbing and metrology tools.

The amount of energy used for resist exposure can be selected in a wide range, from a few mJ/cm² to several thousands of mJ/cm². This corresponds to a wide selection of resist thickness, from a fraction of micron to about 100 µm.

The **Control Unit** is an easy serviceable rack cabinet hosted below the write head. Therefore, it does not require any additional floor space.

The **PhotonSteer** package includes all necessary software drivers and the user interface for managing the Imager through the Control Unit. A layout editor is also included (CleWin5), with format converters to/from GDSII, DXF, CIF, Gerber, etc

No special facility or safety measure is required for system installation. Only a standard 220-230 V or 110-115 V grounded wall plug is required. The

system enclosure protects the user from any laser stray light and interlocks switch off the laser beam or the whole system in case of intentional access to the interior of the system.

CONCLUSIONS

SUSS MicroTec's LI series, with its versatile surface laser patterning technology, lends itself as an ideal tool for the many requirements of academic and industrial R&D laboratories. With their primary focus on flexibility, robustness, ease of use, and large spectrum of possible customization, the several models within this product range allow to provide always the most suited solution for each specific user application.

Dr. Claudio Arnone is President and R&D manager at MICROTECH srl, Italy. He graduated in Italy in 1978 and later he carried out pioneering work on laser processing at MIT-Lincoln Laboratory. Co-founder of MICROTECH in 1992, now actively collaborates with SUSS MicroTec in the field of laser writing.



HIGH PRECISION DISPENSE SYSTEM

Dinesh Vijayaraghavan Electronics Test Engineer Coater Systems, SUSS MicroTec Lithography GmbH, Schleissheimer Str. 90, 85748 Garching, Germany

Presisely controlled dispensing of photoresist is one of the key process steps in photolithography. Beside basic requirements like a bubble free dispense, the accuracy and flowrate profile influence the uniformity of a coating. Up to date, high precision dispensing was an exclusive domain of positive displacement pump-systems.

SUSS MicroTec recently introduced a pressure based dispense system, which breaks into this area. A dispense volume repeatability of $\pm 1\%$ (3σ) and accuracy of $\pm 2\%$ was made possible by means of sophisticated monitoring and control mechanisms. Furthermore a flow-sensor located at the latest possible point allows for monitoring the real flow and controlling the system accordingly. Software algorithms act as back bone of the system performance. The system can be used to dispense chemicals with viscosities from 1 cps to 10,000 cps.

Accuracy of a high end pump built with off-the-shelf parts

Usage of smart sensors at critical places combined with optimized control algorithms leads to the system's superior performance.

- Flow sensor: Measuring at the point of dispense.
- Bubble sensor: Placed at a location where enough resist is left to finish the current dispense. In a next step the bubble can be purged out without affecting the wafer.
- Strategically reducing the tube size down the line leads to increased resistance against bubbles.
- Usage of less pressure (<1 bar) to attain a required flow. When compared to other pumps which require up to 5 bar.

Figure 1 shows the performance over complexity of the SUSS dispense systems vs. other systems available and well known on the market.

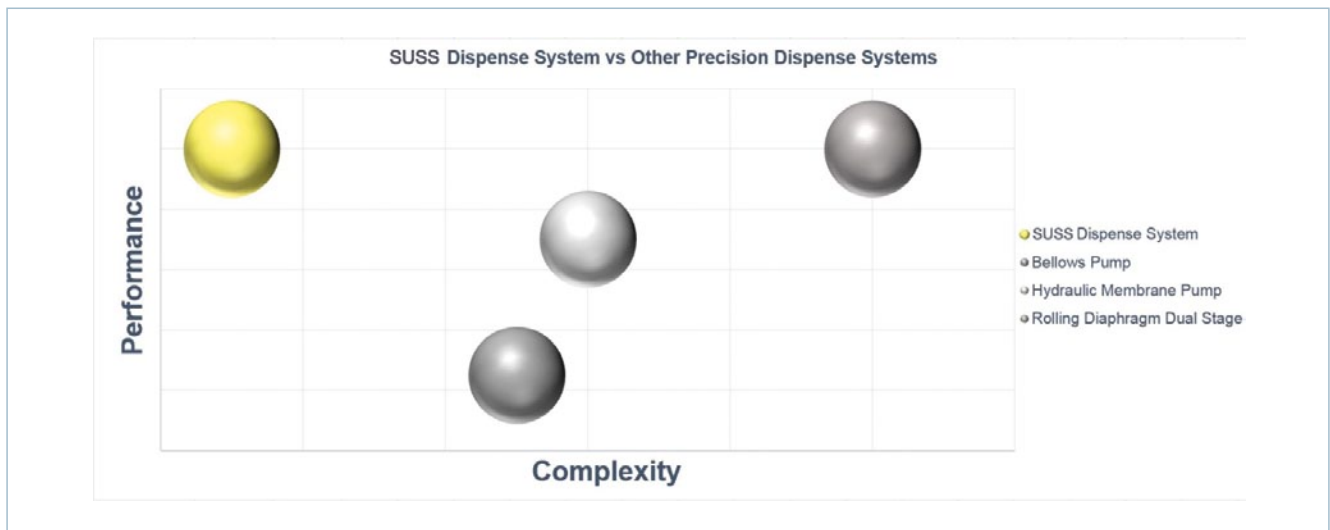


Figure 1 Comparison of SUSS Dispense System to other systems on the market

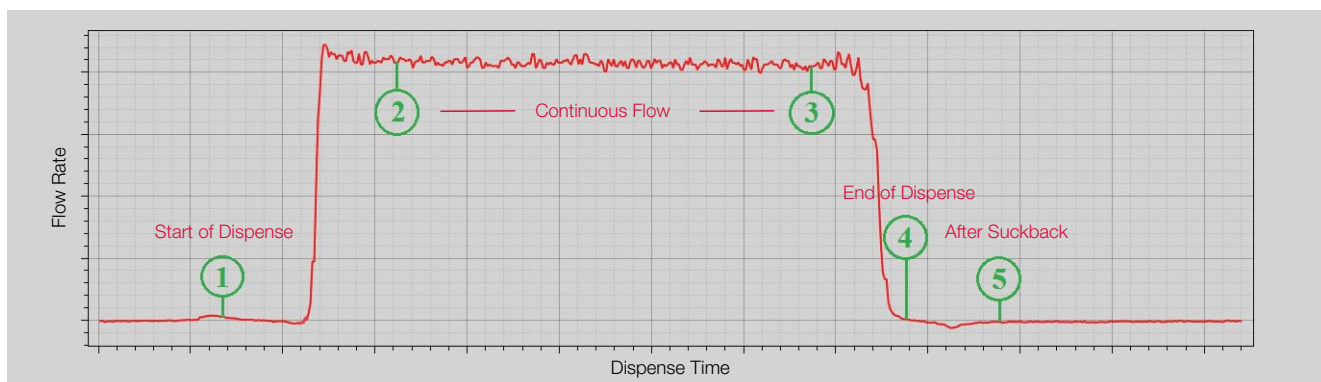


Figure 2 Actual screen-shot of the control software showing the flow rate over time

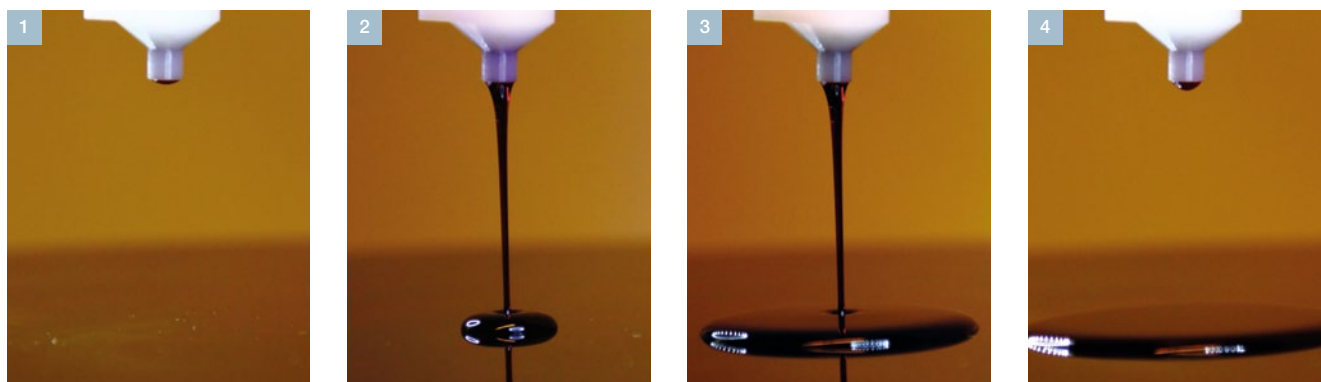


Figure 3 The different phases of a dispense at the nozzle – see figure 2 for correlation

LOGGING OF REAL FLOW

The dispense system is monitoring and logging each dispense in real time.

In figure 2, an actual screen-shot of the control software is shown. The different phases of the dispense are marked and described.

In figure 2, the different phases of a typical dispense are shown. The dispense is being spilt into 5 sections:

- 1) **Start** – The suck-back volume is being pushed out almost simultaneously with the ramp up of the dispense flow. This ensures that the precision of the dispense amount is not affected in any means.
- 2) **and 3) Continuous flow** – The picture shows the constant flow rate over the period of the dispense.
- 4) **End of dispense** – Ramp down of the dispense rate by closing of the dispense valve. As can be seen in the picture there is a small drop of resist hanging out before the last step.
- 5) **After suck back** – By activating the suck back valve this small drop is pulled back into the line as can also be seen in the graph.



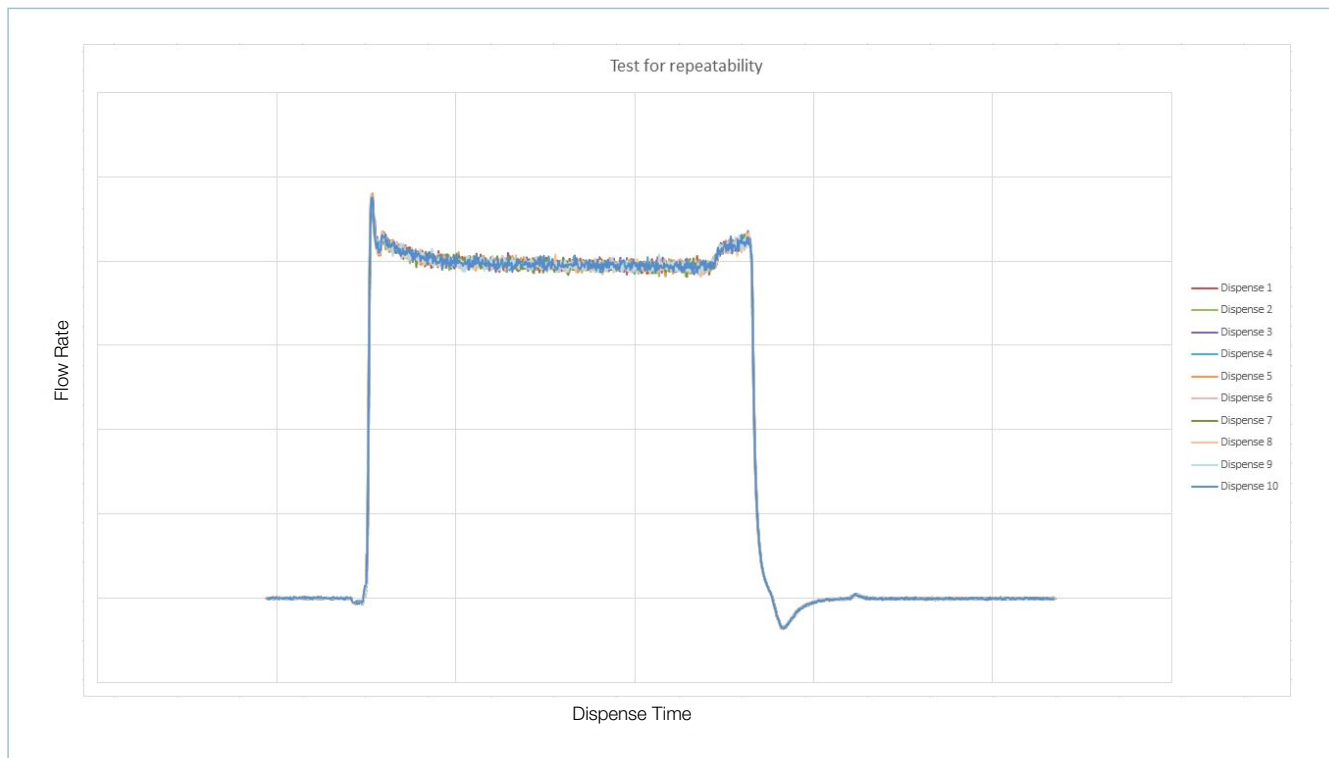


Figure 4 Overlay of 10 dispense graphs

The suck-back rate and amount are programmable via software which helps to optimize a dispense to e.g. various viscosities and specific requirements. All of this shows the precision monitoring and control capabilities of the SUSS Dispense System.

By overlapping multiple dispense graphs the repeatability of the system is shown in Figure 4.

ADAPTABILITY OF SYSTEM (temperature and viscosity changes)

The SUSS dispense system is designed to be insensitive to temperature changes and changes in viscosities. The accuracy of the system stays inside the specification range even at notable change in temperatures. This makes the system less dependent on a temperature controlled environment, thereby lowering the total cost of ownership of the system.

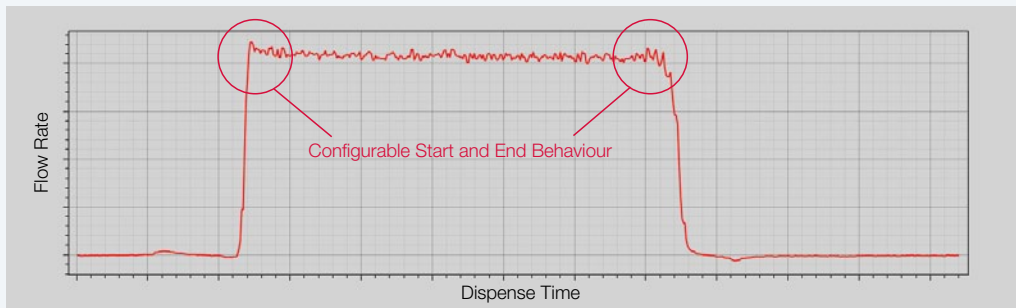


Figure 5 (1) *Optimized to get square wave dispense*

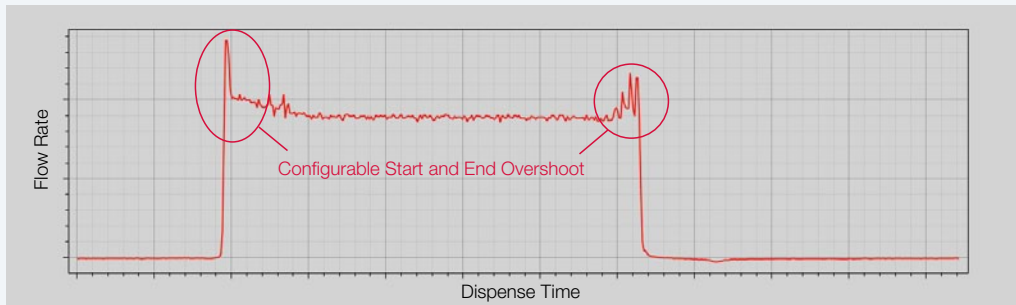


Figure 5 (2) *Optimized to get overshoot in the start and end*

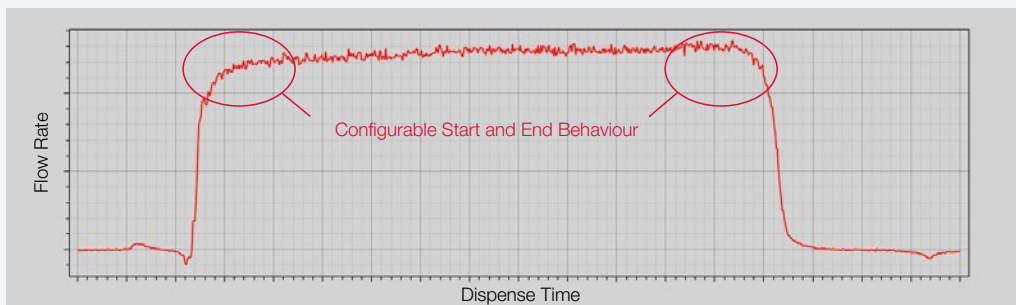


Figure 5 (3) *Optimized to have slow opening and closing behaviour*

COMPLETE CONTROL OF DISPENSE (adjustment of START and END slope):

As different processes may require different flow behavior, the SUSS dispense system gives possibilities for all sort of variations. This opens up the door for optimization of the dispense profile. The user can ensure that the process is optimized to the specific needs and the system is immune to various drifts.

Figure 5 gives a basic idea of how the dispense characteristics can be changed.

Figure 5 (1):

Shows a dispense similar to a digital square form.

Figure 5 (2):

Shows a dispense with a spike in the beginning and also at the end of dispense. The slope of the spike can also be optimized to match the customer process.

Figure 5 (3):

Shows dispense with smoothened open and closing behaviour.

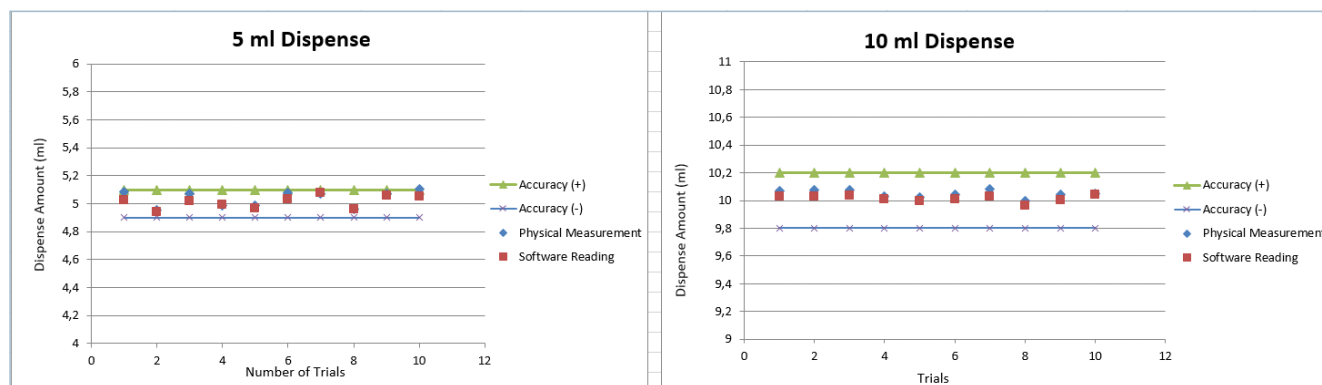


Figure 6 Results

ACCURACY AND REPEATABILITY OVER A RANGE OF FLOW:

The system accuracy and the repeatability is being specified as $\pm 2\%$ and $\pm 1\%$ respectively. The results of 5 ml and 10 ml dispenses are given in figure 6. The results show that the readings are well within the specification.

SUMMARY

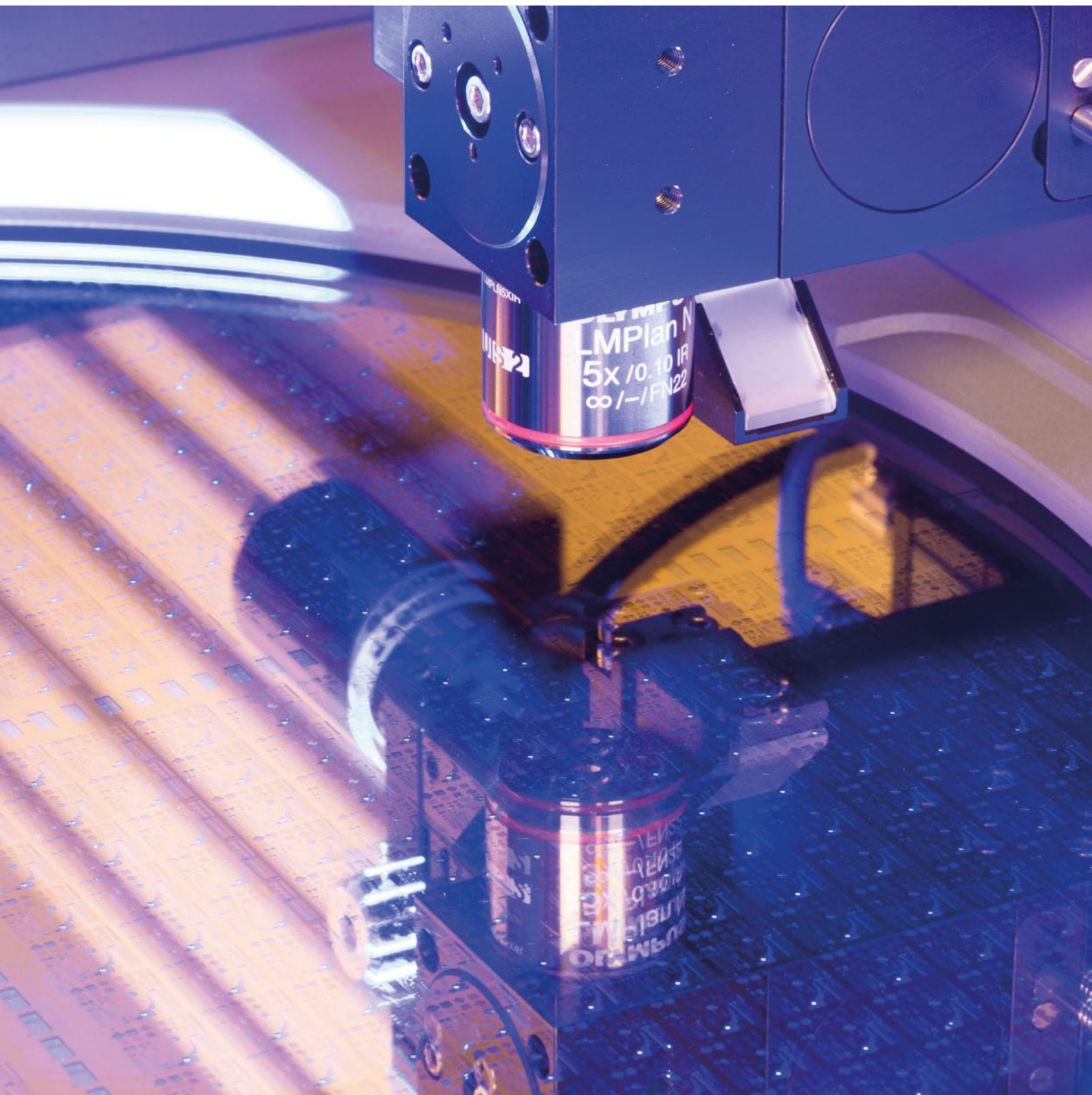
The SUSS dispense system is designed with focus on performance and easy operation. It can be used for resist volumes between 5 ml and 25 ml with $\pm 2\%$ dispense volume accuracy and $\pm 1\%$ repeatability. The system features great possibilities of monitoring and controlling the dispense profile at the point of dispense in real time. Since the system allows various optimizations such as optimization of start and end of dispense, the entire dispense profile can be adjusted for a specific process. This helps the user to adapt the system to various range of viscosities and optimize the dispense for a specific process requirement.

Acknowledgement

I am very thankful to Dr. Oliver Treichel for giving me an opportunity to work under him in this project. In his guidance, which helped me to accomplish the given task. Also I am very much thankful to Kader Mekias and Bjoern Boeckle for being very supportive and friendly throughout the project work. It was the project from Oliver and Kader and I am part of the team. Finally thank you Gary Choquette for giving me the opportunity to address the project on behalf of our team.

Dinesh Vijayaraghavan graduated in Electronics and communications engineering from Anna University, Chennai, India in 2012 and he holds a M. Sc. degree in Sensor systems Technology from the University of Applied Science Karlsruhe in 2015. He was with SUSS MicroTec from 2014 until now and works as Electronics Test Engineer. He is mainly focused on handling various types of sensors for different applications.





UV-LED LAMP HOUSE – LIGHT SOURCE OF THE FUTURE

Bettina Kothe SUSS MicroTec Lithography GmbH, Schleissheimer Str. 90, 85748 Garching, Germany

The new, innovative UV-LED lamp house concept of SUSS MicroTec combines high efficiency and flexibility with eco-friendliness and reduced complexity and represents a trend-setting alternative to common lamp houses.

It supports full process capability for today's lithography users and enables tomorrow's process technologies.

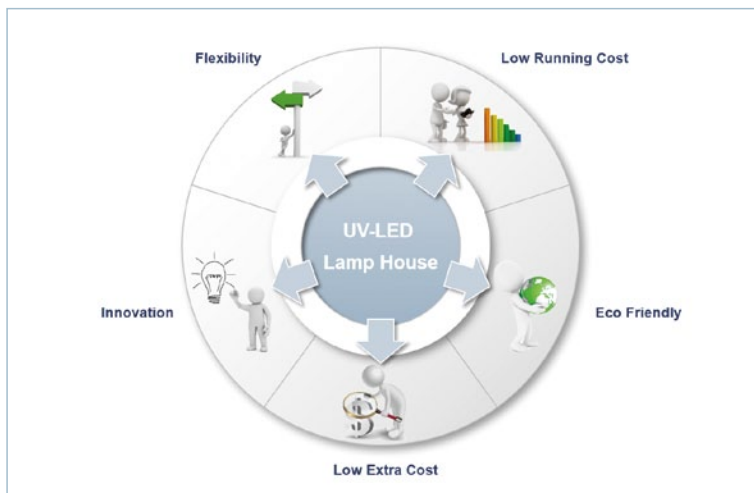


Figure 1 Key features of the UV-LED lamp house

One key element in semiconductor lithography is the exposure UV light.

The demand for an exposure with high intensity and good uniformity all over the substrate surface as well as the emission of a suitable spectral range are major challenges facing the development of light sources and defraction reducing optics for mask aligners.

Exposure of photosensitive resists requires very sophisticated light sources and only a few are suitable for this highly specialized task. Since many years the commonly used light source is a mercury short-arc lamp (Hg lamp). It provides the proper wave length ranges combined with high

intensity. It is well-proven and serves the market for exposure tools in the semiconductor industry.

On the other hand the use of these lamps is associated with multiple challenges and risks.

Limited life time, high maintenance intensity, use of harmful mercury and the high operating pressure of the lamp are only a few factors making the use of these lamps cost-intensive, ecologically sensitive and safety-at-work mandatory.

But what are alternatives?

In the past years the development of LEDs has made good progress and therefore it found its way into everyday life. LEDs are durable, versatile, "green" and economic. Also the development of UV-LEDs driven mainly by industrial applications has advanced recently.

So why not use in a lamp house?

SUSS MicroTec has made an important step into the future by developing a new UV-LED lamp house.

TECHNICAL FACTS

The newly developed lamp house uses a state-of-the-art UV-LED light source including the latest technologies. The LED arrays provides a several wavelengths spectrum suitable for today's advanced processes and resists.

The additional flexibility enables new processes and easier operation and maintenance of the equipment.

The used UV-LEDs deliver a similar spectral range as common Hg lamps. They provide comparable intensity and uniformity for the main Hg spectral lines 365 nm (i-line), 405 nm (h-line) and 436 nm (g-line). The variability however is considerably

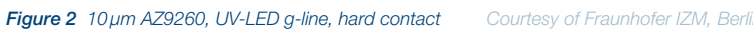
induced errors (e.g. forgotten filters) are reduced

Optics to achieve optimum results

COMPATIBILITY

process stability dent prevention Environmental friendly disposa

for the shutter function is required



Courtesy of Fraunhofer IZM, Berlin



Courtesy of Fraunhofer IZM, Berlin

CONCLUSIONS

Especially concerning safety requirements the UV-LED lamp house offers tremendous advantages. Besides protection against UV light no special precautions are necessary for this kind of light source.

The UV-LED light source follows the world-wide need for eco-friendly and energy-saving behavior. It supports European initiatives to reduce use of hazardous material and high power consumption.

COST-OF-OWNERSHIP

The low energy consumption and the long life time of the UV-LED light source combined with marginal maintenance and disposal costs create a positive cost-of-ownership balance for our customers.

Slightly higher acquisitions cost is compensated by significantly lower running cost and the absence of service and maintenance times.

Figure 4 shows a typical cost-of-ownership balance of a classical Hg lamp house (blue) in comparison with the UV-LED light source (yellow).

After a depreciation time of 8 years the running cost for the UV-LED lamp house will decrease dramatically and will tend to zero while the use of an Hg lamp house will produce yearly cost of at least 2.500€ for power consumption, lamp exchange and maintenance.

The UV-LED lamp house is currently available for manual Mask Aligners SUSS MA/BA8 Gen3 and SUSS MA/BA6 Gen3. It is combined with the highly specialized SUSS MO Exposure Optics for optimum uniformity and resolution results.

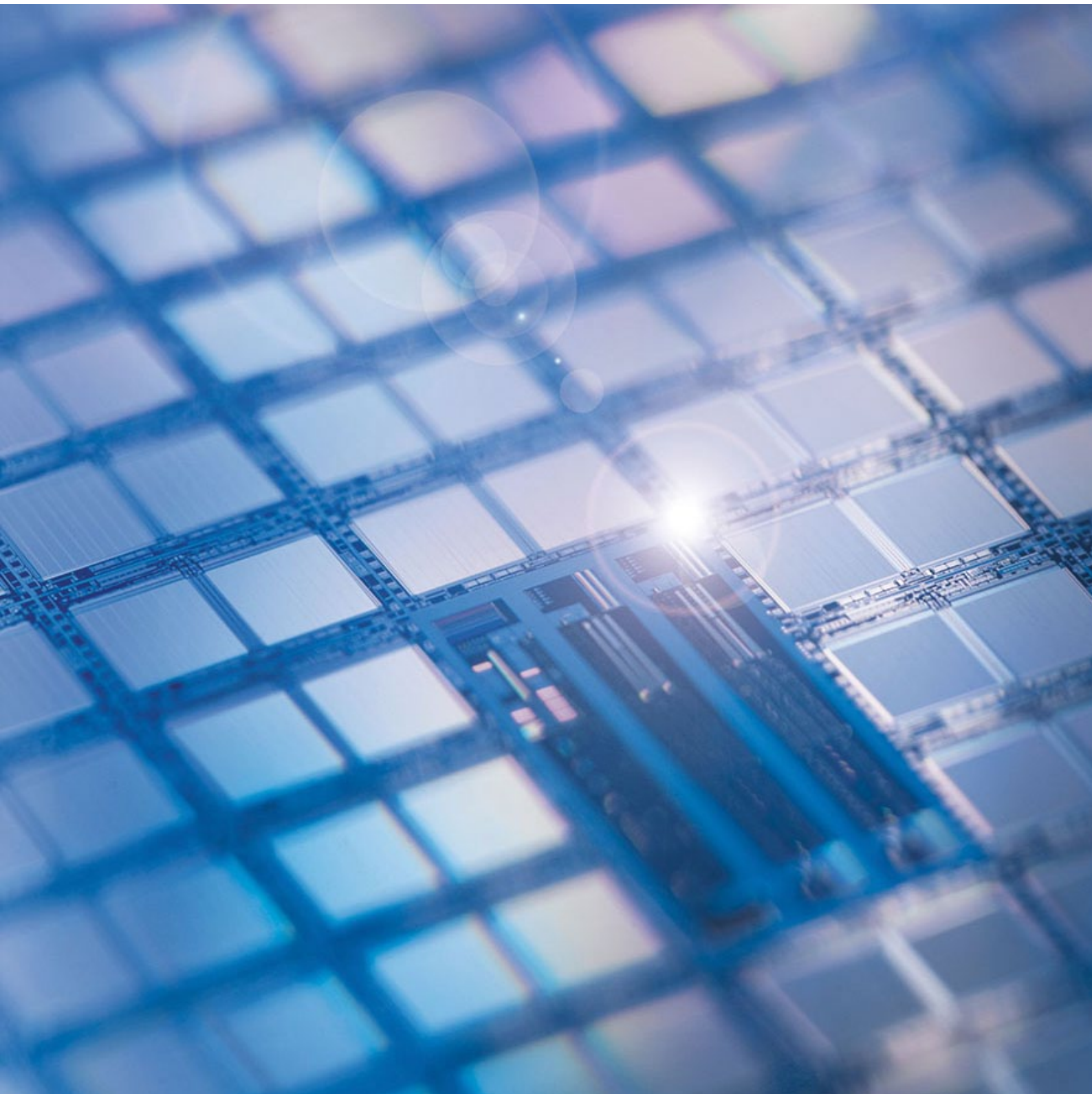
More products are planned to be equipped with the UV-LED lamp house in the future.



Figure 4 Comparison of cost between Hg lamp house and UV-LED lamp house

Bettina Kothe studied Photo Engineering in Köln with a specialization in Physical Optics. 1982 she started at Karl Süss KG as a research engineer. She was project engineer for Automatic Alignment and for the development of the first manual Mask Aligner MA6. For some years she joined the Marketing Department as Product Manager Mask Aligner. Since 2000 she is responsible for Technical Documentation at SUSS MicroTec Lithography GmbH, Garching.

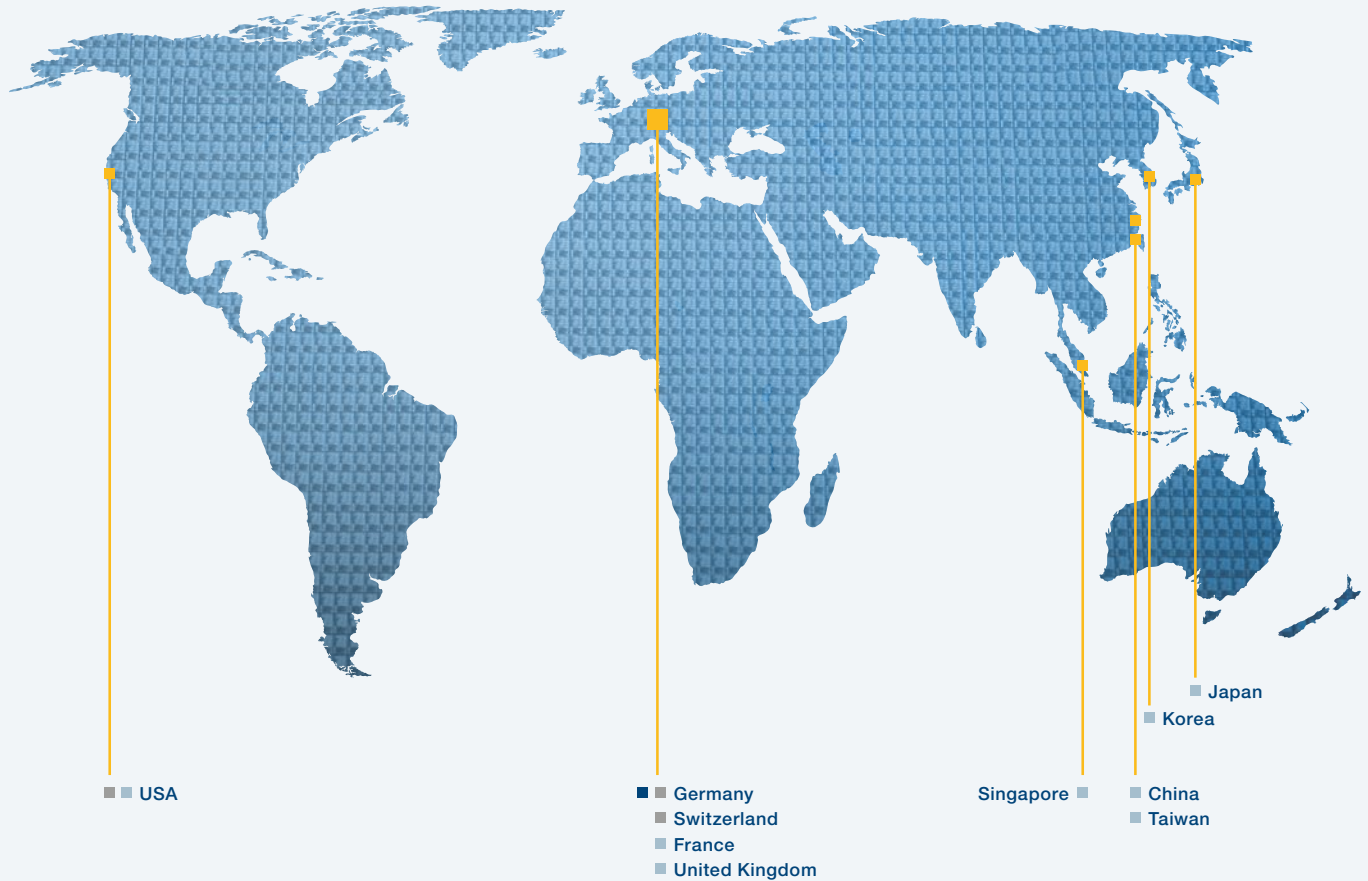




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