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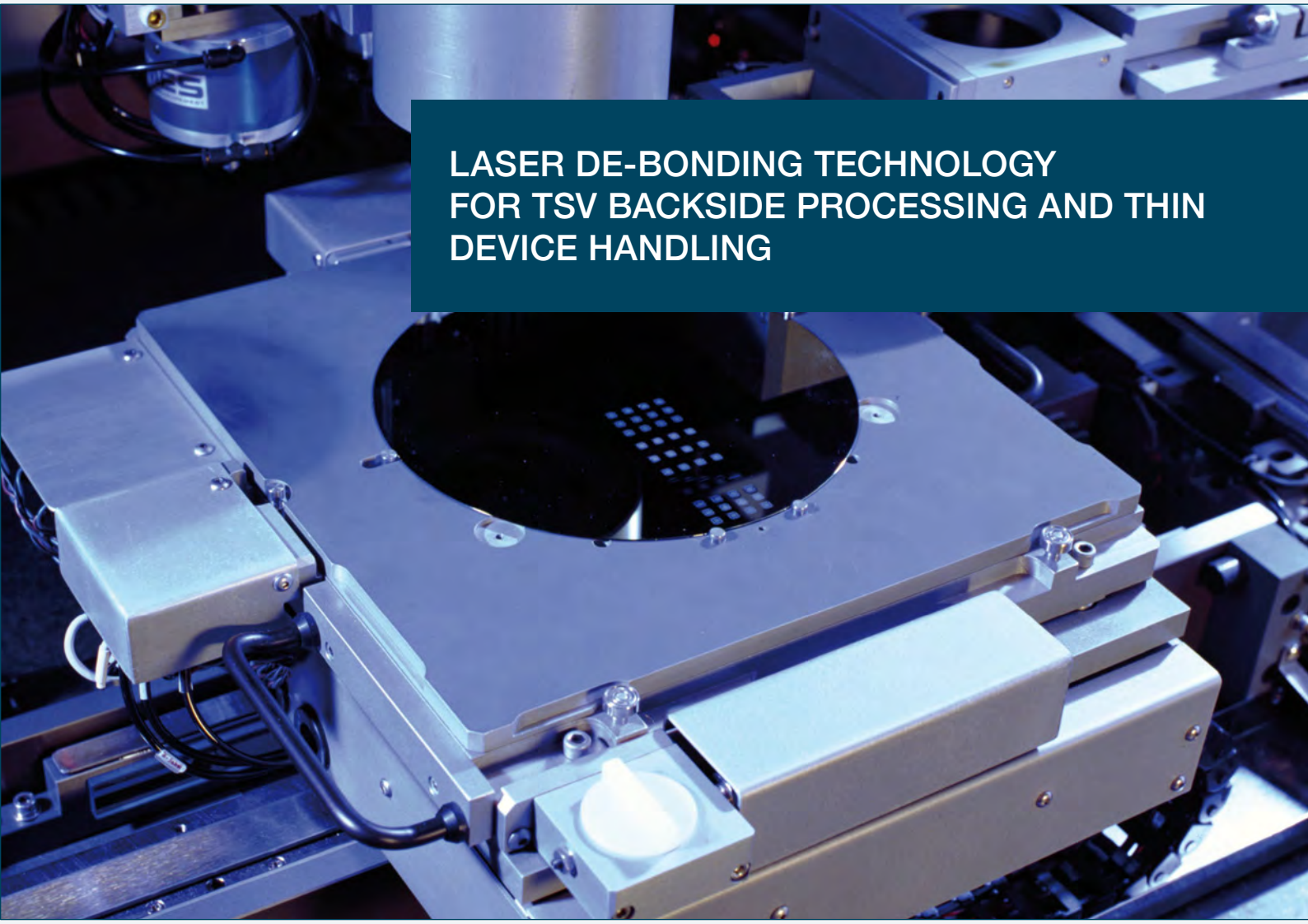

LASER DE-BONDING TECHNOLOGY FOR TSV BACKSIDE PROCESSING AND THIN DEVICE HANDLING

Partners for Technology Leadership

Ordered Arrays of Nanoporous Gold Nanoparticles

In the Spotlight

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+ EDITORIAL

Frank Averdung
President & CEO
SÜSS MicroTec AG

Looking back at 2012, we saw a challenging year for the semiconductor industry. In addition to the cyclical downturn the worries about the global macro economy created a climate of uncertainty resulting in a softening of the business. On the positive side the demand for smartphones, tablets, ultrabooks and other high-tech consumer devices kept growing providing a positive outlook for the years to come.

Despite of the unfavorable industry climate, SUSS MicroTec managed to expand the company. With the acquisition of Tamarack Scientific and its integration into the SUSS MicroTec group, the lithography division has significantly extended the portfolio of exposure systems. SUSS MicroTec is the only company that can offer the semiconductor backend market lithography solutions ranging from proximity exposure over UV projection and laser ablation to nanoimprint.

Intense interaction with our customers and business partners is crucial to us. Understanding their challenges and applying this knowledge in the development of next generation technology is the foundation for mutual success. 3D Integration and other mid-end processing technologies are gaining importance and have developed into a strategically important business for many global players. In November we hosted the Asia Technology Forum 2012 to present and discuss ideas and solutions regarding the current technological trends and requirements of the semiconductor market. Customers and cooperation partners from industry leading companies and renowned research institutes joined us including representatives from STATS ChipPAC, Industrial Technology Research Institute (ITRI), Shanghai Institute of Microsystem and Information Technology, Brewer Science, Fraunhofer IZM Berlin, GenISys, HD MicroSystems, Yole Développement and PVA TePla.

You will find topics of the Asia Technology Forum reflected in some of the articles in this issue, e.g. a thorough overview about existing materials and methods for temporary bonding as well as temporary de-bonding, presented by experts in this field. Furthermore we review new insights into technologies for wafer level packaging in LED manufacturing.

In 2012 SUSS MicroTec has become partner of the „BlueECOmpetence“ initiative of the VDMA (Association of German Machine and Plant Engineering). We joined this initiative because sustainability is increasingly gaining importance in the industrial sector. As a company we regard environmental protection, health and safety of the society as well as the wellbeing of every individual as an important part of our corporate social responsibility. We include economic, environmental and social aspects into our decisions.

For 2013 the market research institute Gartner predicts a stabilization of investments into semiconductor equipment with an upturn to follow in 2014.
On this positive note I wish you a successful year 2013.

POLYIMIDE BASED TEMPORARY WAFER BONDING TECHNOLOGY FOR HIGH TEMPERATURE COMPLIANT TSV BACKSIDE PROCESSING AND THIN DEVICE HANDLING

K. Zoschke, T. Fischer, M. Töpper, T. Fritzsch, H. Oppermann, T. Braun, Fraunhofer Institute for Reliability and Microintegration - IZM, Gustav-Meyer-Allee 25, 13355 Berlin, Germany
O. Ehrmann, K.-D. Lang, Technical University of Berlin, Gustav-Meyer-Allee 25, 13355 Berlin
Toshiaki Itabashi, Hitachi Chemical DuPont MicroSystems Ltd., 1-4-25, Kohraku, Bunkyo-ku, Tokyo, 112-0004 JAPAN
Melvin P. Zussman, HD MicroSystems, Dupont Experimental Station, PO Box 80334, Wilmington, DE 19880-0334, USA
Matthew Souter, Tamarack Scientific, 220 Klug Circle, Corona, CA, 92880 USA

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ABSTRACT

Temporary wafer bonding for thin wafer processing is one of the key technologies of 3D system integration. In this context we introduce the polyimide material HD3007 which is suitable for temporary bonding of silicon wafers to carrier wafers by using a thermo compression process. Coating and bonding processes for 200 mm and 150 mm wafers with and without topography as well as two de-bonding concepts which are based on laser assisted and solvent assisted release processes are presented.

Based on tests with temporary bonded 200 mm wafers, we found a very high compatibility of the bonded compound wafers with standard WLP process equipment and work flows suitable for backside processing of "via first" TSV wafers. Processes like silicon back grinding to a remaining thickness of 60 µm, dry etching, wet etching, CMP, PVD, spin coating of resists and polymers, lithography, electro plating and polymer curing were evaluated and are described in detail. Even at high temperatures up to 300 °C and vacuum levels up to 10-4 mbar, the temporary bond layer was stable and no delamination occurred. 60 µm thin wafers could be processed and de-bonded without any problems using both release methods. De-bonding times of less than a couple minutes can be realized with laser assisted de-bonding and several minutes with a solvent based release. Compared to glues of other temporary handling systems, the proposed material offers the highest temperature budget for thin wafer backside processing as well as fast and easy de-bonding at room temperature.

1. INTRODUCTION – REQUIREMENTS IN TEMPORARY WAFER BONDING TECHNOLOGY

The fabrication of ultra-flat devices and stacked architectures is becoming more important than ever. Thus, technologies for extreme wafer thinning, thin wafer handling and thin wafer backside processing as well as assembly strategies for thin components are imperative to enable three-dimensional system architectures based on through silicon vias (TSVs) and stacked ICs. [1, 2, 3]

Today, due to technological and economic reasons typical TSV depths are in the range of less

than 100 µm with declining tendency. Thus, the fabrication flow of such devices involves thinning of the wafers in order to match their thickness to the TSV depths. After thinning, the wafers need to be further processed to connect the TSVs with routing and contact structures which is highly sophisticated and challenging since wafers with less than 100 µm thickness cannot be handled using standard semiconductor fabrication and handling equipment. To enable processing of the thin wafers they need to be mechanically stiffened by temporary carriers, which can be easily released after the processing is finished. Based on the broad variety of different boundary conditions for thin wafer processing like process type, wafer type to be processed and final device application, there are a lot of different requirements which temporary carrier solutions need to fulfil. In order to reveal these different requirements, Figure 1 shows two generalized work flows of thin wafer processing.[4, 5]

In step 1, the device wafer is bonded onto the carrier wafer creating a compound wafer. The bonding process needs to be compatible with the properties of the device wafer like surface topography, surface material, restrictions in process temperature etc. Most important is that the temporary adhesive planarizes the topography of the device wafer and that a void free bond interface can be established.

Step 2 involves the thinning and subsequent backside processing of the device wafer. Depending on the particular application, a lot of different processes can be necessary to create the backside structure. In the case of typical TSV backside preparation, besides back grinding, processes like CMP, dry etching, CVD, lithography, PVD, wet etching and electro plating are performed. Thus, it is absolutely mandatory that the compound wafer is fully compatible with all these processes and remains stable even under severe process conditions such as high temperature, high vacuum and immersion into solvents or acids.[6, 7]

Step 3 includes the de-bonding of the carrier wafer from the processed thin device wafer. The de-bonding process should be fast and as gentle as possible for the device wafer. Residues from the temporary adhesive should by easily removable from the device wafer without long and severe cleaning procedures.

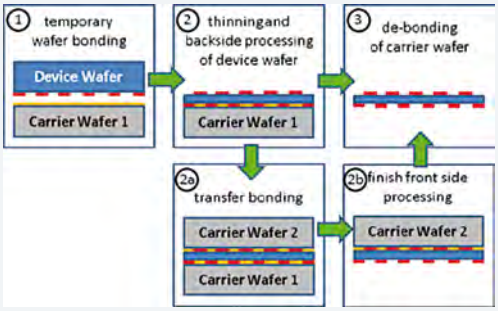


Figure 1. Generalized work flows for wafer thinning and thin wafer processing

In some process scenarios it is required that the processing ends at the topside of the wafer (step 2b). Therefore, a wafer flipping is required which is realized by transfer bonding and shown in step 2a. Based on that, the temporary bonding and de-bonding concept should enable that a second support wafer can be bonded onto the backside of the device wafer and that the first support wafer can be subsequently removed from the front side.

In recent years, some different thin wafer handling and temporary wafer bonding approaches haven been proposed which fulfil more or less the above mentioned requirements and which all have their specific pros and cons. Usually, not all requirements can be fulfilled by one and the same approach, but is seems to be especially hard to combine high temperature stability with broad process compatibility and fast and easy de-bonding capability. With respect to this, we propose a new temporary bonding technology based on polyimide adhesive HD3007 from HD Microsystems which is a competitive alternative to the existing approaches.[8-12]

The coating and bonding process are discussed in section 2 of this manuscript. Two different de-bonding concepts are discussed in sections 3 and 4. In section 5 we present an evaluation where HD3007 bonded compound wafers were processed according to a typical TSV backside preparation scheme.

The proposed material can also be used for the preparation and flip chip assembly of thin ICs. Corresponding evaluations are discussed in section 6.

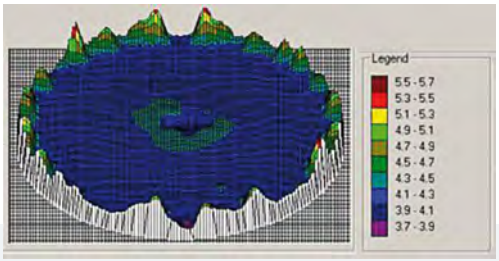


Figure 2. Thickness deviation of cured HD3007 film at 200 mm wafer

Finally, we present a modified version of the material which can planarize higher surface topographies. The corresponding evaluations and results are presented in section 7.

2. TEMPORARY WAFER BONDING USING HD3007

All discussed evaluations in this chapter were performed on 200 mm wafers. The material HD3007 is a solution of a polyamic acid in butyrolactone/PGMEA with a liquid viscosity is 9-11 Ps. The solution contains 24-26 % non-volatile contents. The cure condition is 250 °C-300 °C for 60 min. The cured films have a glass transition temperature of 180 °C and a CTE of 50 ppm/K. The weight loss after 10 min at 350 °C accounts for 0.2 %. [13-16]

Firstly the coating was optimized using a fully automated coater system ACS200 from SUSS MicroTec. In the final process we used a center dispense of the liquid material followed by a spread spin at 1000 rpm for 10 s. After spread spin, the material was spun off at 1400 rpm for 60 s. After a two-step prebake at 90 °C for 90 s and 120 °C for 90 s the material was cured for 60 min at 290 °C under nitrogen atmosphere. Figure 2 shows a typical thickness distribution of a cured HD3007 film on a 200 mm wafer. Excluding the edge bead, the film thickness has a mean value of 4.1 µm with a deviation of +/- 0.4 µm. The edge bead zone has a width of 5 mm with a maximum increase of the film thickness of 7 µm at the rear edge.

After the coating optimization was finished the wafer to wafer bonding tests were performed using a fully automated wafer to wafer bonder from EVG. In these tests the coated silicon wafers were bonded to 500 µm thick glass wafers of type Schott B33.

For handling inside the machine, the wafers were placed onto a rigid bond tool with the coated silicon wafer as bottom wafer and the glass wafer as top wafer. Three distance holders of 200 µm thickness were used to ensure a separation gap between the two wafers before the bonding sequence was started whereas the bonding sequence is defined as a set of recipe commands performed inside a bond chamber after the bond tool with the wafers was loaded into the bond chamber.

For the first trials we alternated three main parameters of the bonding sequence which are bond temperature, bond pressure and bond time within a range of three set points each. Temperature was alternated between 200 °C, 275 °C and 350 °C, pressure was alternated between 0.07 MPa, 0.14 MPa and 0.22 MPa and time was alternated between 10 min, 35 min and 60 min. The value 0.22 MPa represents the maximum pressure of the used bond chamber by using 200 mm wafers.

After the bond chamber had been closed, the bond tool remained for 8 min on the bottom chuck of the bond chamber which was preheated to 125 °C. This was done to enable the bond tool and wafers to heat up and drive out water from the HD3007 film. Then, the chamber was evacuated to a vacuum level better than 1*10-3 mbar and the temperature of the bottom heater was increased to the corresponding bonding temperature of the particular experiment. After the temperature had been reached, the separation flags were moved out between the wafers so that the surfaces could touch each other and the corresponding bond force was applied for the specified bonding time.

Based on these first screening tests, we found that HD3007 could be well bonded at 350 °C independent from the chosen bond force and bond time of the test matrix. The samples bonded at 200 °C showed severe bond defects, whereas the samples bonded at 275 °C displayed only a few bonding defects. In later experiments with a finer mesh between the evaluated process conditions, we found bonding processes working from 275 °C by using a pressure of 0.22 MPa and a bonding time between 1 and 10 minutes. It was also found that the prebake inside the bond chamber could be skipped if the chamber is immediately evacuated after

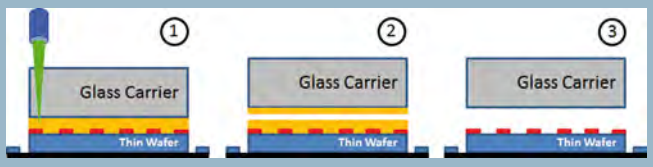


Figure 4. Principle workflow of laser induced de-bonding

the wafers were loaded. Figure 3 shows some plots of the major bond parameters of typical bonding processes for HD3007.
After bonding process optimization, some tests regarding the characterization of the bond strengths were performed. First tests by insertion of a razor blade between the two wafers showed that the bond interface appears to be very strong. Later, die shear tests were performed. However, at room temperature HD3007 shear failure never occurred since the silicon or glass always failed due to fractures before. A repetition of the test at approximately 150 °C showed shear strength of the adhesive of 40 MPa.

3. LASER INDUCED DE-BONDING OF HD3007

A de-bonding of the silicon and glass carrier wafer can be obtained by irradiation of the HD3007 bond layer through the glass wafer using a 248 nm excimer laser. The absorption spectrum of HD3007 shows, that wavelengths <248 nm are fully absorbed within a 200 nm thick film of HD3007. Thus, above a certain value of energy fluence the material is decomposed within this zone so that the bond layer is opened. Due to that, the de-bonding zone is always located 200 nm behind the glass wafer surface and never closer to the customer wafer.

Results show no adverse effects of the excimer laser debond process. The de-bonding mechanism itself is not dependent on the thickness or thickness deviation of the HD3007 bond layer. Figure 4 shows the principle workflow of the excimer laser induced de-bonding approach.
The de-bonding tests were performed with 200 mm wafers at Tamarack Scientific (USA) using its M42X high speed excimer laser system featuring an x-y moving stage and on-the-fly laser processing as shown in Figure 5. The compound wafers were either mounted onto a film frame carrier or directly chucked with the glass side up onto the stage which drove the wafer under the laser beam (picture 1 in Figure 4). The movement of the stage was controlled a way that the exposed laser spots overlap each other by ~50 µm. With an appropriately sized laser, a complete 200 mm wafer could be laser irradiated in < 30 s. After the laser irradiation, the glass wafer could be easily removed from the silicon wafer by using some vacuum tweezers (picture 2 in Figure 4).

After excimer laser detach, both the device and carrier wafer need to be cleaned to remove the remaining HD3007 film, which is roughly 200 nm thick at the glass side and in the range of several micrometers at the silicon side (picture 3 in Figure 4). For the cleaning procedure we used EKC865TM remover which is an excellent stripping agent for HD3007 and has a proven compatibility with metals and cured polymers. By immersion of the wafer into a 60 °C warm remover bath, the remaining 4-5 µm thick HD3007 layers could be removed within less that 30 s. Even the 200 nm thin layers on the glass wafers could be removed by this method.

4. SOLVENT BASED DE-BONDING OF HD3007

Figure 6 shows the principle workflow of solvent based de-bonding. To enable a fully solvent based release process, perforated carrier wafers are required. Due to that, a suitable remover can dissolve the glue directly at the bond interface and release the carrier from the thin wafer. For the release process the compound wafers are mounted on a film frame with the perforated carrier facing up (picture 1 in Figure 6). Following, the sample is immersed into a tank with tempered EKC865TM remover to dissolve the HD3007 bond layer (picture 2 in Figure 6). For the evaluations we used bath temperatures between 60 °C, and

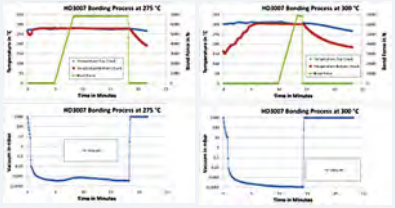


Figure 3. Two optimized processes regimes for HD3007 wafer to wafer bonding at 275 °C and 300 °C


Figure 5. setup of laser de-bonding with 248 nm UV excimer laser and x-y moving stage

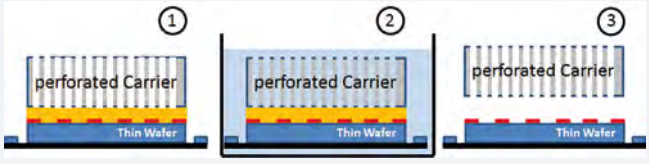


Figure 6. Principle workflow of solvent based de-bonding

80 °C and obtained a detach time for the carrier between 16.5 min and 6.5 min. After the release was done, a further cleaning and rinse process was performed to remove the remaining glue residues from both carrier and device wafer (picture 3 in Figure 6).

In the described experiments perforated glass carrier wafers by Schott Advanced Optics (Germany) were used. The used wafers had a thickness of 500 µm and perforations all over the whole wafer area. The perforations had round shape with a diameter of up to 370 µm and a pitch of 500 µm. Figure 7 shows an example of a bonded compound wafer composed of a silicon wafer and a perforated carrier wafer. The perforated carrier wafer is facing up. As can be seen in the picture, the holes are distributed over the entire surface of the carrier wafer except in a 5 mm wide edge exclusion zone. Due to this edge zone, the HD3007 cannot properly be dissolved here which prevents a full wafer release. To solve this issue, we had to cut away the edge zone for our experiments. But to make this a feasible approach for industrial use, the edge zone should shrink to a width of 1 mm which could be bridged by solvent diffusion along the bond interface. Due to the reduced surface area of the perforated glass carrier wafers which is approximately 50 % of the regular wafer surface the bond pressure during wafer bonding was also reduced by the same percentage. Apart from this change the optimized bond processes for HD3007 could be used as described above.

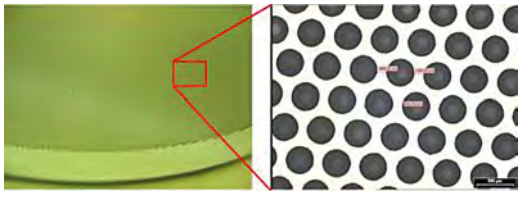


Figure 7. Perforated glass carrier wafer bonded to silicon wafer

5. EVALUATION OF HD3007 TEMPORARY BONDING FOR WAFER THINNING AND PROCESSING OF THIN WAFERS

After the evaluation and optimization of wafer to wafer bonding and de-bonding had been finished, we ran setup lots to evaluate the whole process chain including wafer thinning and backside processing. All experiments were done using 200 mm monitor wafers without TSVs or front side topography. In a first step, the silicon wafers were bonded onto perforated and non-perforated glass carrier wafers by using the process described above. Then the silicon wafers were thinned and subsequently processed based on a standard TSV backside processing scheme as shown in Figure 8. After support wafer bonding (Figure 8/ picture 1), the silicon wafers were back ground to a target thickness value of 70 µm using a DISCO wafer grinder. Following, a silicon dry etch was performed to remove additional 10 µm from the silicon using an advanced silicon etcher from SPTS. So a final silicon thickness of 60 µm was reached with a TTV of around 5 µm (Figure 8/ picture 2) which corresponds to the TTV of the carrier wafers themselves.
In a next step, a 1 µm thick PECVD oxide was deposited onto the backside of the thin silicon wafers (Figure 8/ picture 3). For oxide deposition we

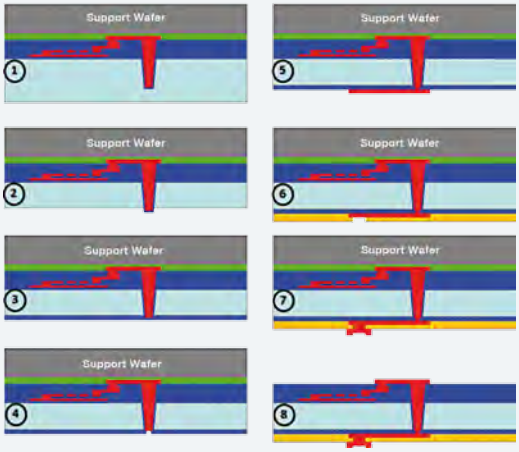


Figure 8. Process flow for TSV backside processing

used both a low temperature PECVD process with 140 °C as well as a deposition process with 300 °C. Even at a process temperature of 300 °C, no fails or deterioration in the temporary bond layers between carrier and silicon wafers could be observed.
In a next step, the deposited oxide was structured by oxide dry etching using a resist mask. This step usually opens the oxide inside the TSV plug diameter. To create the resist mask, a photo resist (AZ series) was spin coated, baked and exposed using fully automated lithography equipment from SUSS MicroTec. The resist development was done by immersion into a developer tank. For etching of the 1 µm thick oxide resist an advanced oxide etcher from SPTS was used. After the oxide was structured, the photo resist was removed by a combination of O2 plasma ash and wet stripping. An example of the created oxide openings is shown in picture 1 of Figure 9. The sample condition corresponds to the schematic drawing in Figure 8 / picture 4.
After the isolation oxide had been deposited and structured, the redistribution layer was fabricated by semi additive technology using copper electro plating (Figure 8/ picture 5). In a first step a seed layer was sputtered onto the thin wafer backside using standard DC magnetron sputtering. In order to define the routing structure a further lithography was done using AZ photo resist as described above. The copper deposition was done with a sulfuric plating bath and a fountain plater setup using a fully automated electro plating tool from Semitool. Picture 2 in Figure 9 shows an example of the created copper redistribution structure.

In the next process sequence (Figure 8 / picture 6), an isolation layer was deposited and structured to cover and passivate the copper routing. For that, a polymer precursor was spin coated onto the wafer and subsequently structured by lithography and puddle development using fully automated lithography equipment. The polymer was cured

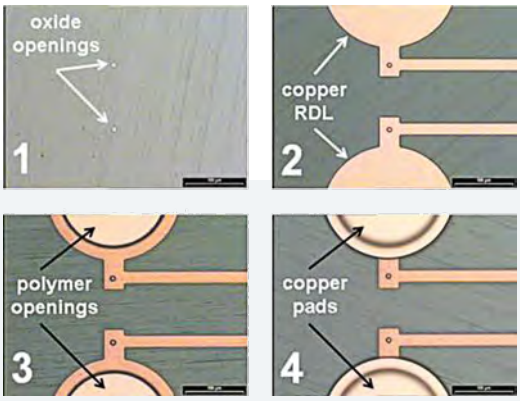


Figure 9. Thin silicon wafer after different steps of backside processing

for 90 min at 250 °C. Picture 3 in Figure 9 shows an example of the created copper redistribution structure with polymer passivation. The polymer openings are located on top of the large copper pads.
As a final step of the backside processing test, thick copper pads were fabricated as UBM for a subsequent assembly (Figure 8/ picture 7). The used process steps correspond to those used for the copper RDL processing. An example of the final processed structures including copper UBM pads is shown in picture 4 of Figure 9.
Figure 10 shows two cross sectional views of a thin wafer with the processed thin film structures mounted on non-perforated or perforated carrier wafers. In the case of the perforated carrier wafer, which is shown in the right picture, a slope underneath the thin silicon indicates the border between hole area and support area of the perforated carrier.
After completion of the backside processing, the bond layers were inspected carefully. After passing the whole process sequence of backside processing, no delamination or fails could be observed in the HD3007 temporary bonding layers.

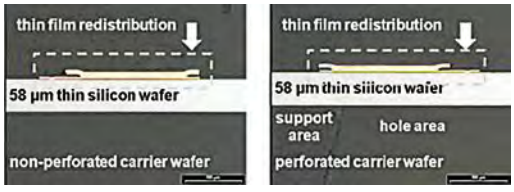


Figure 10. Cross sectional view of processed thin wafers mounted at non-perforated (left) and perforated (right) carrier wafers

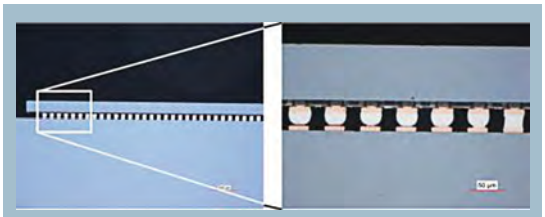


Figure 11. Cross cut of assembled thin IC with open contacts in chip peripheral area

As a final test in this experiment, the de-bonding of the carrier wafers was performed. For that, we used the setup for laser and solvent based de-bonding as described above. The compound wafers were mounted with the side of the thin wafer on film frame carriers. Based on the initial experiments, non-perforated and perforated carrier wafers could be easily removed from the thin wafers. After subsequent cleaning of remaining residues, we obtained thin single side processed wafers mounted on film frame.

6. EVALUATION OF HD3007 TEMPORARY BONDING FOR THIN WAFER BUMPING AND ASSEMBLY OF THIN ICS

Many applications require thin ICs to be assembled in standard flip chip technology by pick & place and reflow. But due to the decreasing silicon thickness, bow effects induced by the CTE mismatch between the ICs BEOL layers and the bulk silicon lead to severe bending of the devices during reflow soldering. Due to the missing stiffening effect of the bulk, silicon of thinned ICs, these bending effects become more severe with decreasing silicon thickness. Figure 11 shows an example of an assembly issue that occurred with 100 µm thin CMOS chips. The chips were fabricated at 200 mm CMOS 130 nm technology having a 22 µm thick BEOL stack comprising 8 routing layers. As preparation for flip chip assembly, the wafers were bumped with AgSn solder on copper UBM and subsequently thinned and diced. The applied bump height is 25 µm/bump pitch is 50 µm. As can be seen in the picture due to the bending effects during reflow soldering, the peripheral bumps were not touching their corresponding landing pads at the substrate side. As a consequence, contacts in the peripheral chip area could not be closed and remained electrically open.

To overcome this bending issue, the thin ICs need to be stiffened during the reflow cycle. Therefore, a special process sequence was developed which enables bumping and thinning of IC wafers including subsequent dicing and flip chip assembly by using a temporary chip level support. The corresponding process flow is shown in Figure 12. The process evaluation was performed with the same CMOS wafer material as already described above. The surface topography of these wafers was 0.8 µm-1 µm and the initial wafer thickness was 725 µm (picture 1/ Figure 12).

In a first step, the thick IC wafer was bonded with the active side to a temporary carrier wafer (picture 2/ Figure 12). Following, the IC wafer was back ground to thicknesses in the range of 90 µm-50 µm using a DISCO wafer grinder. In order to provide a stress relief of the mechanically back ground silicon, another 8-10 µm silicon were removed by dry etching using an advanced silicon etcher form SPTS (picture 3/ Figure 12).

Then, as the wafer had reached its target thickness a transfer bonding was performed. For that, glass wafers were prepared with HD3007 coating and cure and subsequently bonded onto the backside of the IC wafer using the 275 °C bonding process as already shown in Figure 3 (picture 4/ Figure 12). Now, the carrier wafer was released from the front side of the IC wafer. After that process, we had created a compound wafer composed of glass support wafer and thin IC wafer with active side facing up (picture 5/ Figure 12).

Following, an AgSn bumping process was done

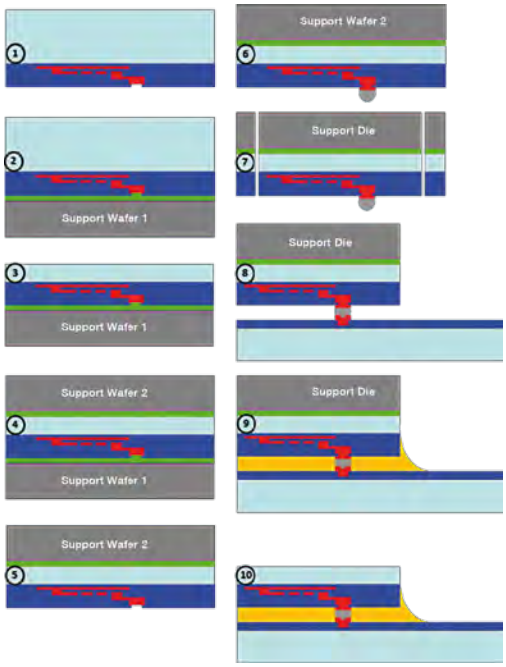


Figure 12. Process flow for preparation and flip chip assembly of thin ICs

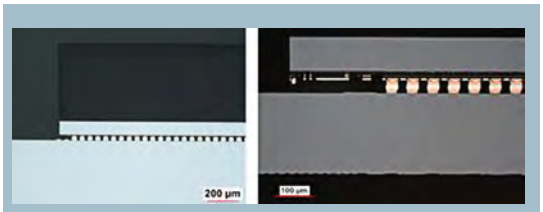


Figure 13. Assembled thin IC before glass carrier release (left) and after glass carrier release (right)

on the active side of the thin IC wafer. Due to the high thermal stability of the HD3007 glue, the bumping process could be done without changing the standard process including sputtering, lithography, electro plating, resist removal, differential etching and solder reflow (picture 6/ Figure 12). Now the sandwich of thin bumped wafer and bonded glass carrier wafer is diced which transforms the carrier wafer into carrier dice located at the backside of each individual thin bumped IC (picture 7/ Figure 12). Due to the stiffening effect of the carrier dice, the thin ICs could be easily assembled by using a standard pick/place and reflow procedure (picture 8/ Figure 12). After IC assembly and under filling, the HD3007 bond layer was exposed through the glass carrier dices and the carriers are removed from the backside of the thin ICs (picture 10/ Figure 12).

Figure 13 shows cross cuts of an assembled thin IC. The left picture shows the condition after reflow assembly. Here, the support chip is still present at the backside of the thin IC. The right picture shows the condition after release of the support die. As can be seen in the pictures, because of the stiffening effect of the support die during the reflow assembly even the peripheral contacts are closed now.

7. EVALUATION OF NEW MATERIAL FORMULATION HD3007HS FOR HIGH TOPOGRAPHY COMPLIANCE

To overcome the thickness limitation of the regular HD3007 material, which is 4-5 µm with single side coating and 8-10 µm if both wafers are coated, a new material version for higher topography compliance was evaluated. The new material is named HD3007HS and gives approximately 30 µm adhesive thickness with one single coating process. All experiments were performed with 150 mm wafers.

For the coating we used a fully automated coating tool from SUSS MicroTec with a Gyrset coater. After a spiral dispense a spread spin was done at 1200 rpm for 4 s followed by a main spin at 1300 rpm for 30 s with closed cover. After a prebake of 100 s at 90 °C and 200 s at 120 °C a 1 mm wide edge bead removal was done using NMP. After NMP spin off and final bake, the wafers were cured for 4 hour at 200 °C. After cure, that film has a mean thickness of 28-30 µm with a thickness deviation of +/-1.5 µm. With this coating process we evaluated the topography planarization properties of the material. For this, we prepared wafers with copper topography of different heights between 5 and 40 µm. As pattern we have chosen a typical IO pad array design with 90 µm pad diameters and 300 µm spacing in between. The results of this evaluation are shown in the diagram in Figure 14 where the degree of planarization (DOP) is shown as a function of the topography height. The DOP is calculated by subtracting the ratio of adhesive thickness increase over topography and the topography height from 1. So the DOP will be 100 %, if there is no adhesive thickness increase on top of topography compared to the surrounding area. The DOP would be 0 %, if the adhesive thickness increased on top of topography by the same value as the topography height. As can be seen in the diagram, up to a topography height of 15-20 µm, the DOP is in the range of 80 %. With higher topography, the DOP drops steadily down to 40 % at 40 µm topography height. The diagram shows furthermore that there is no significant difference between the behavior of the DOP at wafer center and edge.

The measurements were taken at the wafer center and wafer rim (15 mm from edge) for each evaluated topography thickness. For that, we did cross cuts after HD3007HS coating and cure and measured the corresponding thickness values by using an optical microscope. For better contrast, the wafers were sputtered with a thin metal film before cross cut preparation. Figure 15 shows two examples of taken cross cuts for the evaluation of the planarization properties. The left picture shows a 20 µm high

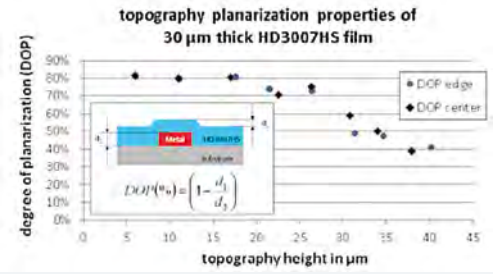


Figure 14. Planarization properties of 30 µm thick HD3007HS films

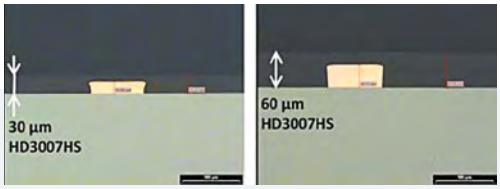


Figure 16. Cross cuts of HD3007HS bonded wafers with topography

topography and the right picture a 40 µm high topography coated with HD3007HS. The left picture represents a DOP of 75 % and the right picture a DOP of 41 %.

After the coating process was optimized and topography planarization properties were determined, we started to evaluate the bonding performance of the new material. All bonding experiments were performed with non-perforated 150 mm glass wafers. On blank wafers without topography we found that the already established bonding processes are also working with the new material. By using the wafers with topography, we found bond defects around the topography, when the topography was higher than 20 µm. To enable the bonding of wafers with higher topography, we coated the glass support wafer with the same coating recipe to gain a further 28-30 µm adhesive thickness.

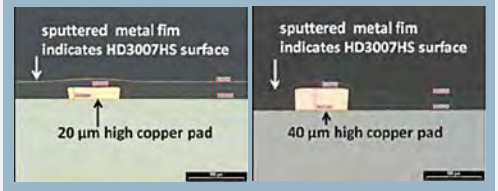


Figure 15. Cross cuts of HD3007HS coated topography

With the additional coating also at the glass wafers, we could bond even the wafers with 40 µm topography without any topography related bonding defects. Figure 16 shows cross sectional views of wafers with topography bonded with HD3007HS. The left picture shows 20 µm topography at the bond interface. Here, a single coating was used giving a 30 µm thick adhesive bond interface. The right picture shows 40 µm topography at the bond interface. To establish this bond, the glass wafer was also coated with HD3007HS which results in a 60 µm thick bond interface.
Figure 17 shows the optimized bond process for the HD3007HS wafer to wafer bonding. The bond tool with the clamped wafer is load into the chamber with top and bottom chuck preheated to 250 °C. After a 3 min wait which is required to enable the bond tool with the wafers to heat up the chamber is pumped down to a vacuum value better than 1*10-3 mbar. Now, the force of 7 kN is applied for 5 min. In order to shorten the overall process time, the cooling inside the bond chamber was skipped. This process is well suited for bonding wafers with HD3007HS coating at both wafers. For wafers with coating only at the silicon side, we recommend a slightly higher bond temperature in the range of 275 °C.

After bonding, the topography wafers were back ground to a target thickness of 100 µm. The measured TTV values were in the range between 5-8 µm. Furthermore, the wafers were exposed to a similar backside processing as described in section 5 and subsequently de-bonded by laser release. All processes could be run without any restrictions. Due to the thicker adhesive layer, the removal time of the remaining HD3007HS after excimer laser release was increased. When using EKC remover at 70 °C, it took 4 min to clear off the 30 µm thick films residue free.

CONCLUSION

HD3007 was successfully evaluated as an adhesive material for temporary wafer to wafer bonding. The material can be applied in a thickness of 5-10 µm and bonded in a broad process window at temperatures between 275 °C and 350 °C by using pressures between 0.07 and 0.22 MPa. As carrier wafers non-perforated and perforated glass wafers were used which enable a laser induced or solvent based de-bonding. Both de-bonding methods are working forceless and very fast. For the laser induced de-bonding, which is done at room temperature, we obtained a de-bonding time of less than 1 min per wafer. For the solvent based de-bonding, a minimum

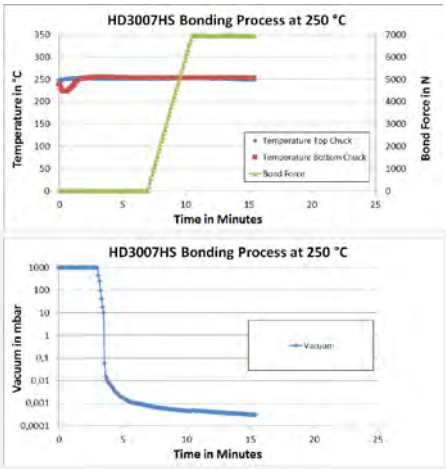
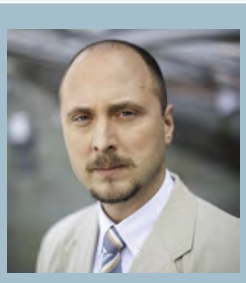


Figure 17. Optimized bond processes for HD3007HS

de-bonding time of 6.5 min could be shown at elevated solvent temperature of 80 °C. To be compliant with higher topographies at the bond interface HD3007HS was evaluated which can be applied with 30 µm thickness in one coating step. A single coating of the material can be used to bond topographies with up to 20 µm height. With an additional coating at the carrier wafer topographies of up to 40 µm height can be bonded.

The bonded compound wafers are fully compatible to standard equipment and processes used for 3D wafer level packaging such as wafer thinning and thin wafer backside processing for through silicon via fabrication. In detail, the bonded wafers passed processes as back grinding, CMP, dry etching, PECVD oxide deposition, sputtering, lithography, electro plating, wet etching and thermal cure without weakening of the bond interface.



Kai Zoschke received his degree in Microsystems Technology from the University of Applied Sciences in Berlin. In 2001 he joined the Technical University of Berlin and worked as Research Engineer in the Berlin Center of Advanced Packaging. Since 2005 he is with Fraunhofer Institut (IZM) in Berlin. He works as process development engineer and group manager in the field of Wafer Level Packaging with special focus on High Density and 3D Integration as well as Wafer to Wafer Bonding. Until now he has authored and co-authored more than 40 technical publications in that research area.

Matt Souter graduated in 1992 from CSULB in California with a BS in Mechanical Engineering. He joined Tamarack Scientific in 2001 and has been active in the role of VP of Sales and Marketing for both the Laser Ablation and Photolithography product lines. Much of his focus as of late, has been in the research and development of alternative patterning techniques using Excimer laser ablation as a means to not only meet next generation Advanced Packaging requirements, but also address a means to lower manufacturing costs. Matt has recently authored an exciting new laser process for the removal of metal seed layers in lieu of standard processing approaches, addressing both technical limitations as well as a reduction in manufacturing costs. This process is currently patent pending. With the recent acquisition, he currently works as Global Sales Director and Laser System Product Manager for SUSS MicroTec.

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ORDERED ARRAYS OF NANOPOROUS GOLD NANOPARTICLES

Dong Wang, Peter Schaaf Chair Materials for Electronics, Institute of Materials Engineering and Institute of Micro- and Nanotechnologies MacroNano®, Ilmenau University of Technology, POB 10 05 65, 98684 Ilmenau, Germany
Ran Ji SUSS MicroTec Lithography GmbH, Schleissheimer Str. 90, 85748 Garching, Germany
Arne Albrecht Center for Micro- and Nanotechnologies, Ilmenau University of Technology, POB 10 05 65, 98684 Ilmenau, Germany

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ABSTRACT

A combination of a "top-down" approach (substrate conformal imprint lithography) and two "bottom-up" approaches (dewetting and dealloying) enables fabrication of perfectly ordered 2-dimensional arrays of nanoporous gold nanoparticles. The dewetting of Au/Ag bi-layers on the periodically pre-patterned substrates leads to the formation of an array of Au-Ag alloy nanoparticles. The array of alloy nanoparticles is transformed into an array of nanoporous gold nanoparticles by a following dealloying step. Large areas of this new type of material arrangement can be realized with this technique. In addition, this technique allows for the control of particle size, particle spacing, and ligament size (or pore size) by varying the period of the structure, total metal layer thickness, and the thickness ratio of the as-deposited bi-layers.

INTRODUCTION

Metallic nanoparticle arrays are attracting more and more attention due to their potential applications in plasmonics[1,2], magnetic memories[3], DNA detection[4], and catalytic nanowire growth[5]. Nanoporous gold is very interesting for application in catalysis[6,7], for sensors[8], for actuators[9,10], and as electrodes for electrochemical supercapacitors[11]. This is due to the unique structural, mechanical and chemical properties of this material[7,12]. Nanoporous gold, already synthesized in the form of nanoparticles, possesses a much higher surface-to-volume ratio than bulk nanoporous gold films and gold nanoparticles[13]. These nanoporous gold nanoparticles are expected to broaden the range of applications for both gold nanoparticles and nanoporous gold due to their two-level nanostructures (porosity of around 10 nm and particle size of a few hundreds nanometers).

Solid-state dewetting of metal films is a simple "bottom-up" approach to fabricate nanoparticles[14,15]. The dewetting of metal films is driven by reducing the surface energy of the film and the interface energy between the film and the substrate, and occurs by diffusion even well below the melting temperature of the film[15]. In addition, alloy nanoparticles can be fabricated using dewetting of metallic bi-layers[13,16]. By combining both, "top-down" approaches (such as lithography) and "bottom-up" approaches, the ordered array of metallic nanoparticles can be fabricated[15,17-19]. The surface of the substrate is pre-patterned into periodic structures using laser interference lithography[15]. focused ion beam (FIB)[17], or substrate conformal imprint lithography (SCIL)[19]. During the dewetting of metal films onto pre-patterned substrates, the periodic structure of the pre-patterned substrates modulates the local excess chemical potential by the local curvature or by limiting the diffusion paths. This leads to the formation of the 2D nanoparticle arrays with well-defined particle size and particle spacing. Dealloying is a "bottom-up" approach to fabricate nanoporous gold by selectively removing or leaching the element Ag from the Au-Ag alloy in an Ag-corrosive environment[20-22]. In this paper, perfectly ordered arrays of nanoporous gold nanoparticles are fabricated using a combination of a "top-down" approach (SCIL) and two "bottom-up" approaches (dewetting and dealloying).

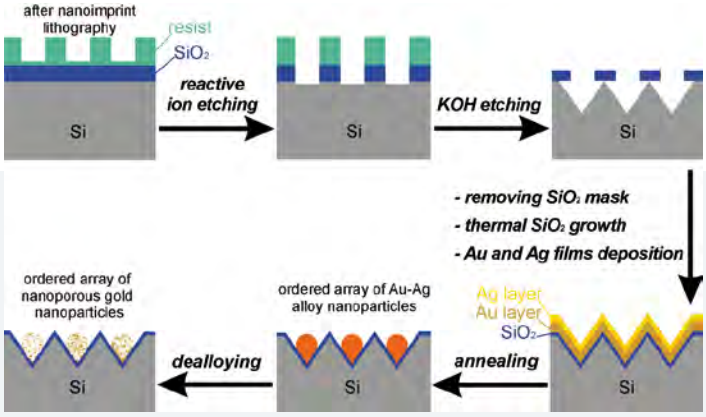

Figure 1. Schematics of the fabrication process for an ordered array of nanoporous gold nanoparticles.

RESULTS AND DISCUSSION

The fabrication process is schematically presented in Figure 1. The surface of a (100) Si wafer was patterned into a periodic array of pyramidal pits (Figure S1) using SCIL, reactive ion etching (RIE), and KOH etching. The spatial period of these pits is 520 nm. 200 nm SiO_2 was thermally grown on the Si wafer, and then an array of holes was defined using SCIL. SCIL was developed by Philips Research and SUSS MicroTec as a new nanoimprint lithography technique which combines the advantages of both UV nanoimprint lithography techniques with a rigid stamp for best resolution and with a soft stamp for large-area patterning[23]. The imprinted structure was then transferred through the SiO_2 layer with RIE. The SiO_2 pattern with the array of holes acted as mask during the anisotropic etching of Si in a KOH solution, and the Si surface was patterned into a periodic array of pyramidal pits. After removing the SiO_2 mask, about 20 nm of SiO_2 was then again thermally grown on the structured Si surface to avoid the reaction between the subsequently deposited metal films and the Si substrate. Au/Ag bi-layers with different layer thicknesses (10 nm/20 nm, 10 nm/25 nm, 10 nm/30 nm, 15 nm/25 nm, and 15 nm/30 nm) were deposited onto the pre-patterned substrates using e-beam evaporation, and then annealed at 700°C in Ar for 15 min to induce dewetting. This temperature is well below the solidus temperature of the Au-Ag system, i.e. the dewetting is solid-state dewetting. By that, perfectly ordered arrays of Au-Ag alloy nanoparticles are first formed on the pre-patterned substrates. Subsequently, dealloying by submerging the samples in a HNO_3 solution results in the transformation of the Au-Ag alloy nanoparticles into the nanoporous gold nanoparticles, due to the dissolution of Ag out of the alloy. As the final result, a well-defined ordered array of nano-porous gold nanoparticles is obtained.

The dewetting of the bi-layers on the pre-patterned substrate with 20 nm thermal SiO_2 was even performed via annealing at 800 °C and 900 °C. However, some Si or silicide grown particles were observed and remain after de-alloying, and this will be investigated in more detail in the future. In addition, reference samples with 15 nm Au/20 nm Ag bi-layers deposited onto a flat Si substrate with 100 nm thick thermally grown SiO_2 layer was annealed at 900 °C in Ar for 15 min and then dealloyed for comparison. Dewetting on a pre-patterned substrate takes place at a lower annealing temperature[24], and higher temperature (900 °C) is required for the dewetting on a flat substrate to form particles.

Excess local chemical potential can be introduced by the pre-patterned structure according to the Gibbs-Thomson relation, $\Delta\mu = \kappa\gamma\Omega$, where $\Delta\mu$ is the local excess chemical potential, κ the local curvature, γ surface energy, and Ω atomic volume. There is an excess positive chemical potential at peaks or ridges due to the positive local curvature and an excess negative chemical potential at pit valleys due to the negative local curvature. Consequently, there is an additional driving force for the diffusion of the metal atoms from the peaks to the valleys during dewetting on the pre-patterned substrate, leading to the formation of the ordered array of nanoparticles. However, in addition to the curvature driven diffusion, the capillary driven diffusion (dominating process for the dewetting on a flat substrate[24]) and grain growth are additional two important processes during dewetting, making the formation of the ordered nanoparticle arrays thickness dependent[19]. For example, the Au-Ag alloy nanoparticles are irregularly distributed after dewetting 10 nm Au/20 nm Ag bi-layers on the pre-patterned substrate (Figure S2). This is probably due to insufficient total layer thick-

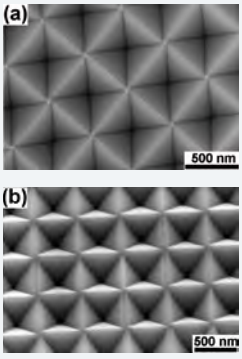

Figure S1. SEM images of the pre-patterned substrate showing the periodic array of pyramidal pits: (a) plan view, and (b) at tilt of 25°.

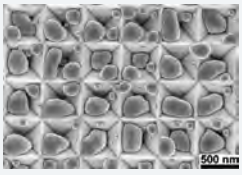

Figure S2. SEM image of the Au-Ag alloy nanoparticles dewetted from 10 nm Au/20 nm Ag bi-layers on the pre-patterned substrate via annealing at 700 °C in Ar for 15 min.

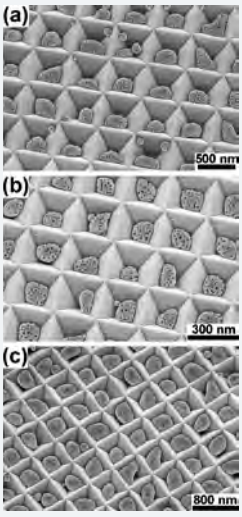

Figure S3. SEM images (at tilt of 25°) of arrays of nanoporous gold nanoparticles induced via annealing at 700 °C in Ar for 15 min and then dealloying from: (a) 10 nm Au/25 nm Ag bi-layers, (b) 10 nm Au/30 nm Ag bi-layers, and (c) 15 nm Au/25 nm Ag bi-layers.

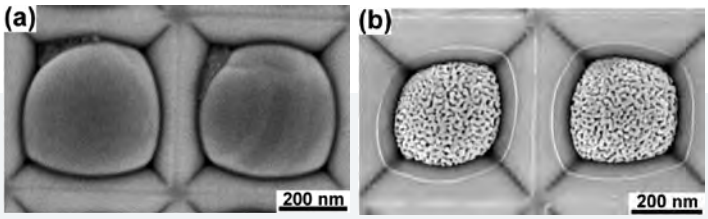

Figure 2. SEM micrographs of samples before and after dealloying: (a) ordered array of Au-Ag alloy nanoparticles dewetted from the 15 nm Au/30 nm Ag bi-layers, and (b) ordered array of nanoporous gold nanoparticles formed after the following dealloying.

ness. As the total layer thickness is increased adequately (Au/Ag: 10 nm/25 nm, 10 nm/30 nm, 15 nm/25 nm, and 15 nm/30 nm), the dewetting on the pre-patterned substrate can lead to the formation of the ordered arrays of the nanoparticles. Additionally, it is possible to control the particle size and spacing by varying the structural parameters (period and depth) of the pre-patterned structure and the layer thickness[19].

Subsequently, dealloying of the ordered arrays of the Au-Ag alloy nanoparticles can result in the formation of ordered arrays of nanoporous gold nanoparticles. Figure 2 shows the SEM images of the ordered array of Au-Ag alloy nanoparticles dewetted from 15 nm Au/30 nm Ag bi-layers and the obtained ordered array of nanoporous gold particles after dealloying. The arrays of the nanoporous gold nanoparticles induced from the 10 nm Au/25 nm Ag, 10 nm Au/30 nm Ag, and 15 nm Au/25 nm Ag bi-layers are still not perfect and even two particles in a single pit can be observed (Figure S3). A perfectly ordered array of nanoporous gold nanoparticles was obtained from the 15 nm Au/30 nm Au bi-layers and there is only one nanoporous gold nanoparticle in every pit. Figure 3a and c display the perfectly ordered array of nanoporous gold nanoparticles in a large area, and the porosity of the particles can be seen more clearly in the corresponding magnified SEM images (Figure 3b and d). In Figure 2b, Figure 3b and d, the white circular lines outside of the particles can be identified as the previous contours of the dewetted Au-Ag alloy nanoparticles before dealloying. This clearly hints to shrinkage of the particles by dealloying. In a previous work, 29 % volume shrinkage of the nanoparticles is reported after dealloying[13].

The surface morphology of the nanoporous gold particles on the pre-patterned substrates changes with the thickness ratio of the as-deposited bi-layers. Au and Ag are fully miscible, thus the Au concentration in the formed Au-Ag alloy nanoparticles can be roughly calculated based on the layer thickness ratio. It is 29 at-% for the 10 nm Au/25 nm Ag bi-layers, 25 at-% for the 10 nm Au/30 nm Ag bi-layers, 38 at-% for the 15 nm Au/25 nm Ag bi-layers, and 34 at-% for the 15 nm Au/30 nm Ag bi-layers. The average ligament size $<\theta>$ is plotted as a function of the Au concentration, as shown in Figure 4. $<\theta>$ decreases from 25 nm (for the particles induced from the 10 nm Au/30 nm Ag bi-layers) to 9 nm (for the particles induced from the 15 nm Au/25 nm Ag bi-layers) with increasing Au con-

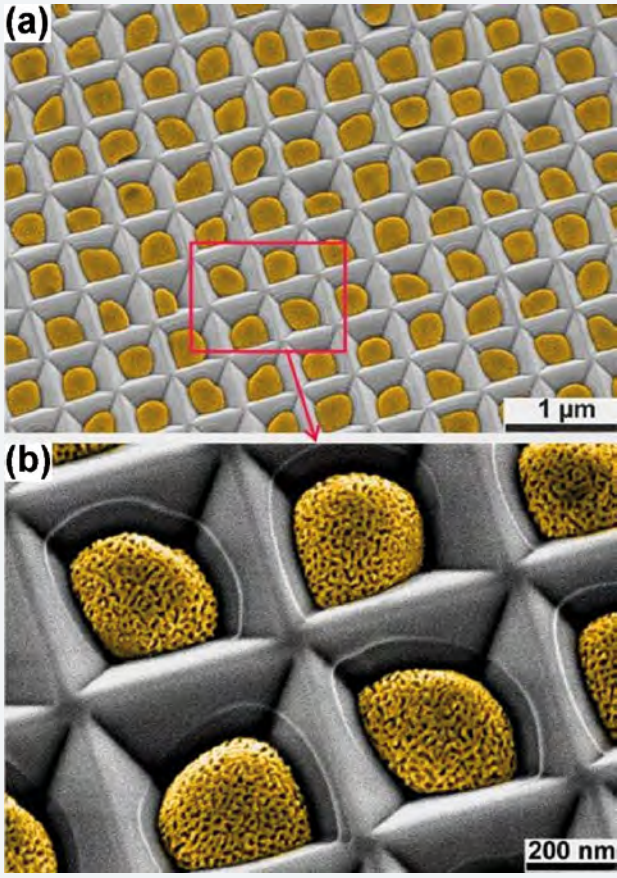

Figure 3. SEM images (false color) at 25° tilt of the perfectly ordered array of the nanoporous gold nanoparticles formed from the 15 nm Au/30 nm Ag bi-layers.

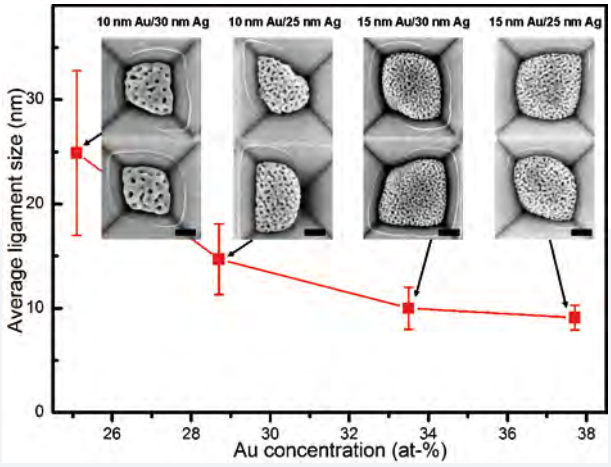

Figure 4. Plot of the average ligament size as a function of the Au concentration of alloy nanoparticles. Error bars are representing the standard deviation. Insets show the corresponding SEM images. Scale bars in the insets are 100 nm.

centration. As Au concentration approaches above 34 at-%, the ligament size seems to approach a lower saturation value of $<\theta>$=10 nm. Therefore, the ligament size (or pore size) of the nanoporous nanoparticles can be controlled by varying the layer thickness ratio of the as-deposited Au/Ag bi-layers. The size shrinkage decreases with increasing Au concentration, as observed from the contours (white circular lines) of the original Au-Ag alloy nanoparticles and those of the nanoporous gold nanoparticles (inset SEM images in Figure 4).

Figure 5 shows the comparing information of both, the array of nanoporous gold nanoparticles induced from the 15 nm Au/30 nm Ag bi-layers on the pre-patterned substrate and the irregularly distributed nanoporous gold nanoparticles induced from the 15 nm Au/20 nm Ag bi-layers on the flat substrate. Figure 5a and b are the SEM images, Figure 5c and d are histograms of the particles distribution, and the mean particle size $<m>$ is determined. Figure 5e and f are the plots of radially averaged autocorrelation. The radially averaged autocorrelation is calculated from the autocorrelation or pair correlation as a function of radial distance.

The first minimum of this function shows the information about mean particle size $<m'>$, and the subsequent first maximum denotes the characteristic particle spacing s. There is a small difference between $<m>$ and $<m'>$ due to the different determination methods.

Normally, the mean particle size or diameter $<m>$, width of the particle size distribution $<\lambda_p>$, and the characteristic particle spacing s increase with increasing film thickness for the dewetted nanoparticles on flat substrates[19]. However, the pre-patterned substrates with nanostructures lead to an obvious reduction of the particles size and spacing[19]. Although the total bi-layers thickness of the as-deposited bi-layers for the ordered array of nanoporous gold nanoparticles is clearly larger than that for the nanoporous gold nanoparticles on the flat substrate, it is seen that the mean particle diameter (323 nm) and characteristic particle spacing (538 nm) of the ordered array of nanoporous gold nanoparticles are much smaller than those (639 nm and 1377 nm) of the nanoporous gold nanoparticles induced on the flat substrate. The array of nanoporous gold nanoparticles

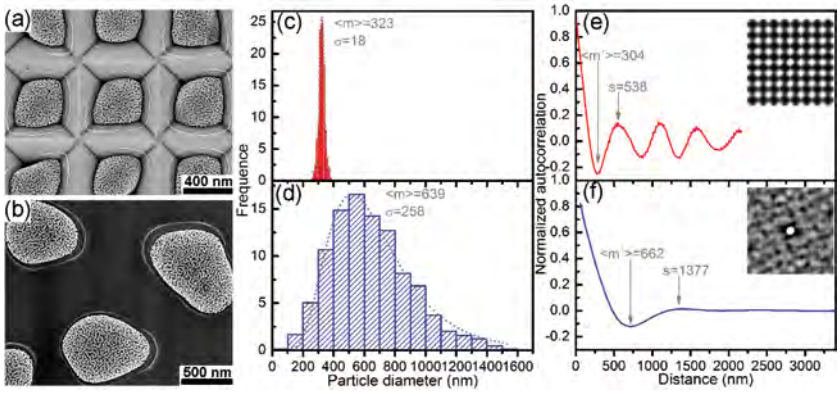

Figure 5. Information of the ordered array of the nanoporous gold nanoparticles formed from the 15 nm Au/30 nm Ag multilayers on the pre-patterned substrate (a, c, and e) and the irregularly distributed nanoporous gold nanoparticles formed from the 15 nm Au/20 nm Ag bi-layers the on the flat substrate (b, d, and f). (a, b) SEM images, (c, d) histograms of the particle diameter distributions, and (e, f) plots of radially averaged autocorrelation. Fitting curves (log-normal function) are superimposed on the histograms. The values $<m>$ or $<m'>$ and σ indicate the mean particle diameter and its standard deviation, and s denotes the characteristic particle spacing (all in nm). Insets in (e) and (f) show the corresponding autocorrelation images.

on the pre-patterned substrate possesses a much smaller width of the particle size distribution comparing to the nanoporous gold nanoparticles induced on the flat substrate, i.e., the particles on the pre-patterned substrate are much more uniform and almost perfectly ordered. The characteristic particle spacing (538 nm) of the array of the nanoporous gold nanoparticles corresponds nearly to the spatial period (520 nm) of the pits of the pre-patterned substrate, and the small deviation is probably due to the uncertainty of the radially averaged autocorrelation. Comparing the radially averaged autocorrelation of the nanoporous gold nanoparticles on the flat substrate, the plot of the array of the nanoporous gold nanoparticles on the pre-patterned substrate shows a regularly waved shape, denoting the high regularity of the nanoparticle array, which is well confirmed by the autocorrelation image (inset in Figure 5e).

CONCLUSIONS

In summary, a combination of a "top-down" approach and "bottom-up" approaches is used to fabricate perfectly ordered arrays of nanoporous gold nanoparticles, which cannot be produced using "top-down" or "bottom-up" techniques alone. By using the SCIL technique, large surface areas can be pre-patterned into uniform periodic nanostructures, and correspondingly, large areas of well-ordered arrays of nanoporous gold nanoparticles can be fabricated. In addition, it is possible to control the characteristics of both particles (particle size and spacing) and porosity (ligament size) by varying the structural parameters of the pre-patterned structure, total layer thickness, and the layer thickness ratio of as-deposited Au/Ag bi-layers. This regular arrangement of nanoporous gold nanoparticles with three-level nanostructures (ligament size of tens nanometers, particle size of a few hundreds nanometers, and well-defined particle size and spacing) is expected to broaden the application areas of both the nanoparticles and nanoporous materials.

EXPERIMENTAL

The surface of a (100) Si wafer was structured into periodic array of pyramidal pits using SCIL, reactive ion etching (RIE, Oxford Plasmalab 100), and KOH etching. Before application of the resist for SCIL, 200 nm SiO_2 was thermally grown on the Si wafer. A pattern with array of holes was defined using SCIL, and then transferred through the SiO_2 layer with RIE. The SiO_2 pattern with holes array acted as mask during the anisotropic etching of Si in a 40 wt-% KOH solution at 60 °C, and periodic array of pyramidal pits was formed. Then, the SiO_2 mask was removed using a 7 wt-% HF solution. About 20 nm SiO_2 was then thermally grown. Au/Ag bi-layers were deposited on the substrates using e-beam evaporation, and then annealed at 700 °C in Ar for 15 min to induce dewetting. Then, dealloying was performed by submerging the samples in a 65 wt-% HNO_3 solution at 21 °C for 5 min. A reference sample (15 nm Au/20 nm Ag bi-layers on a flat SiO_2/Si substrate) was processed by an annealing at 900 °C in Ar for 15 min and then submerging in a 65 wt-% HNO_3 solution at 21 °C for 5 min. The SiO_2 thickness of the reference sample is 100 nm. The samples were investigated using an ultrahigh resolution scanning electron microscope (FE-SEM, Hitachi S-4800). Particle diameters were recalculated as circular diameters and measured by thresholding the image contrast in the SEM images and counting pixels. The average ligament size, which is defined as the equivalent diameters of ligaments in the nanoporous gold nanoparticles, were determined manually by identifying a minimum of 20 ligaments, measuring across the shortest distance of each ligament and then averaging. The radially averaged autocorrelation is calculated from the autocorrelation (also known as pair correlation) of pixels of a converted binary image as a function of their radial distance. In the binary images, the areas of particles and background can be best identified.

Dr. Dong Wang studied chemical engineering at Wuhan University of Technology in China and received his B.Sc. in 2000, and studied materials science further at RWTH Aachen in Germany and received his M.Sc in 2004. Then, he conducted his doctoral research at research Center Karlsruhe. After receiving his Ph.D. in 2007, he moved to Hannover to pursue a post-doc at Hannover University. In 2010, he accepted a staff scientist position at Ilmenau University of Technology (TU Ilmenau). His research interest lies atnanostructured materials.

Professor Dr. Peter Schaaf studied material physics at Saarland University, Saarbrücken. After graduating to Diplom-Physiker in 1988 he continued doctoral research at Saarland University in Materials Science. He earned his doctoral degree in 1991 with honors. After that, he moved to Göttingen University for a PostDoc position in 1992. In 1995, he got an assistant professorship and was promoted to associate professor there in 1999. In 2008 he accepted a full professor position at Ilmenau University of Technology (TU Ilmenau). Currently, he is director of the Institute of Materials Engineering and vice-dean of the Department of Electrical Engineering and Information Technology.

As Application Engineer Nanoimprint at SUSS MicroTec since 2008 Ran Ji is responsible for the development and improvement of nanoimprint processes. He has been working in the field of nano-fabrication and nanoimprint for over 8 years and is highly experienced in processes, stamp fabrications and machines of nanoimprint techniques.

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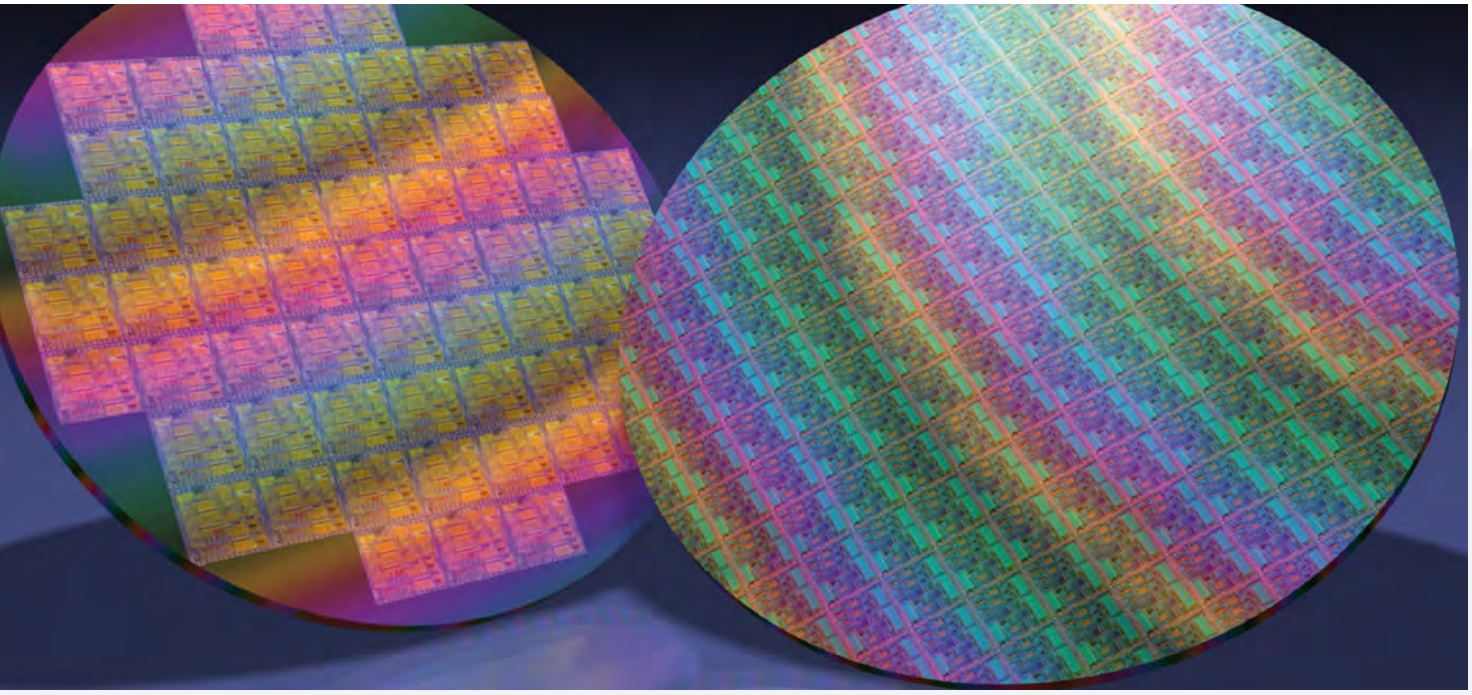
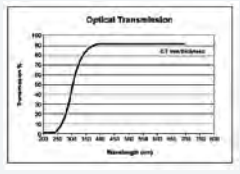
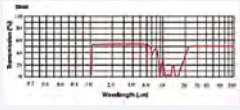


TEMPORARY BONDING AND DEBONDING - AN OVERVIEW OF TODAY'S MATERIALS AND METHODS

Chris Rosenthal, SUSS MicroTec Inc., 430 Indio Way, Sunnyvale, CA 94085, USA





Carrier wafers are an integral part of the temporary bonding process and their selection dictates what type of bonding and debonding methods can be employed. Photosetting adhesives require a carrier wafer that is transparent at the wavelength of light needed for curing – most common being UV radiation. Furthermore, if laser ablation is used for debonding, like the original 3M Wafer Support System, the carrier wafer must allow laser light to pass through to weaken the adhesive bond sufficiently to enable carrier wafer removal.

Mechanical Properties	Corning Glass	Silicon
Density (g/cm^3)	2.38	2.33
Young's Modulus (GPa)	73.6	129.5 [100]
Knoop Hardness (kg/mm^2)	453	1150
CTE (0-300 °C, x10-7/ °C)	31.7	31.5

Figure 1. Comparison of the physical properties of Silicon vs. Glass. [1]

Size of the carrier wafer also needs to be carefully considered.

The typical choices are a carrier wafer that is equal to or slightly greater in diameter to the device wafer; however, if the device wafer undergoes edge trimming to reduce the likelihood of cracking and chipping during backgrinding, the effect will be the same as attaching an oversized carrier. Since the device wafer is very thin and fragile at the edges after back grinding there is a handling advantage with an oversized carrier as it serves as a bumper.

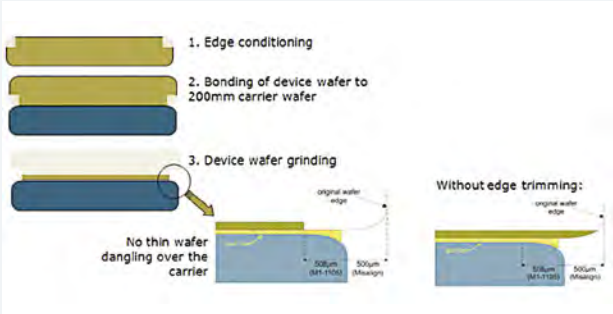
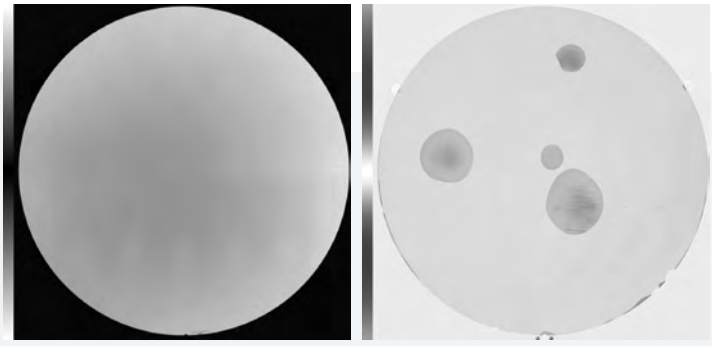


Figure 2. Edge conditioning (trimming) reduces wafer diameter after back grinding.[2]



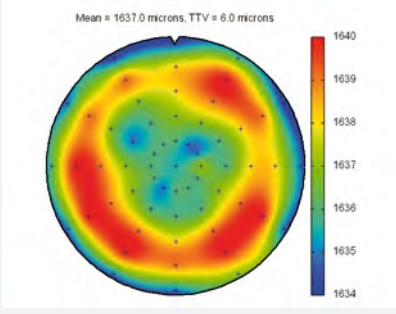
Example 1. Scanning Acoustic Microscope (SAM) scan of bonded wafers with and without voids.

The choice of carrier wafer also influences what inspection techniques can be used in subsequent process steps such as bonding. After the wafers have been bonded the bond quality needs to be confirmed. There are several options available including scanning acoustic microscopy (Example 1) or full field optical inspection such as the Spark system by Nanometrix. Since very small voids can potentially lead to delamination under high vacuum or during high temperature processing, the detection limit needed depends on the bond strength of the adhesive to the various substrate interfaces. There is a delicate balance between the need for strong enough adhesion to prevent bubbles from growing and weak enough adhesion to permit debonding at the end of processing.

After determining that you have a void free well bonded wafer to carrier pair, the last important item to check is the Total Thickness Variation (TTV) of your bonded pair. TTV control in the low single digit micron range is needed primarily for the final Thru Silicon Via reveal process. If there is a great deal of variation in thickness the high spots will be ground down too much and more importantly the low spots may not be ground down enough to expose the tops of the vias. Although some thickness variation can be overcome by sophisticated grinding equipment, it is best to bond the wafers with as little TTV as possible. To achieve the best bonding performance in terms of TTV control low TTV coating is considered by many to be important; however, newer bonding techniques don't necessarily require good post adhesive coat TTV to achieve good post bond TTV. Furthermore, TTV can be affected by post bond processing so caution must be taken depending upon the adhesive properties and the processes it is subjected to.[3]

Now that we understand what we are trying to achieve - a void free low TTV bonded pair - how do we go about getting it and what other factors need to be considered? First and foremost is adhesive selection. There are many types of adhesives available today and more in various stages of making their way onto the market. In terms of their primary function, bonding, there are three mainstream classifications: thermocompression, thermoset and photoset. As the name implies, thermocompression adhesives bond using heat and pressure; however, what differentiates them from other adhesives is their ability to "flow" or be reset by applying more heat or pressure. Thermoset adhesives, on the other hand, can use the same bonder as thermocompression adhesives, but once the adhesive is set it cannot be reworked - as the crosslinking/reactive groups have been activated and the process cannot be undone. Photoset adhesives are similar in that once the polymerization has occurred it cannot be reversed.

It is often very helpful to put together a matrix to sort out which adhesive(s) qualify on paper – such as cost vs. thermal stability[4]. Other notable qualities to be considered are; chemical resistance, vacuum stability, bonding speed, debond throughput, and final clean requirements. Thermal stability can be established with thermal gravimetric analysis (TGA) and thermal desorption spectroscopy (TDS). To what degree the adhesives need to be thermally stable is a function of the adhesion strength and process



Example 2. Typical TTV mapping result display format.

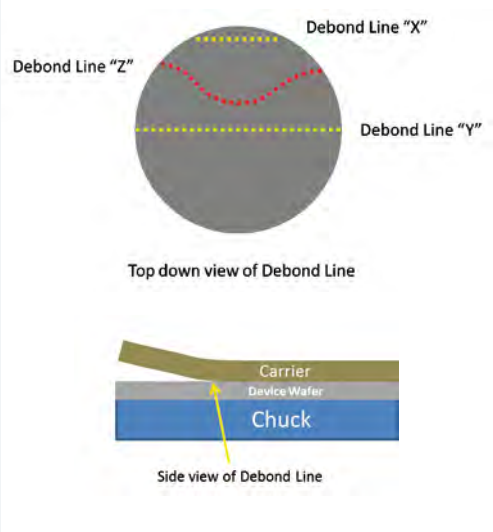
conditions. Some adhesives are very chemically inert, which is great for resisting chemical attack during photolitho or etch processes, but it also means that residue from these adhesives is very difficult to chemically rinse or dissolve away as is sometimes needed during the final cleaning process to ensure the device wafer's surface is clean enough for soldering or compression bonding - the next big processing challenge in fabricating both homogeneous and heterogeneous 3DIC's. However, some very chemically resistant adhesives make films that can be easily removed by peeling techniques and this could eliminate the need for costly and hazardous chemical stripping baths. As you can see careful thought and compromise is needed during the adhesive selection process.

Once the adhesive has been selected the bonding process and recipe need to be sorted out. Bonding is typically achieved with light, heat and pressure, singly or in combination. Anything that minimizes movement and stress on the wafers during bonding will help produce the best results. Let's examine why. First, in order to minimize void formation during bonding it is best to bond inside a vacuum chamber. Of course, the chamber does not provide a perfect vacuum and a small amount of gas could be trapped at the bond interface; however, current bond chambers are able to pump down enough to reduce the voids to below detection levels of the metrology equipment. A side benefit to bonding in a vacuum is it also helps draw out any volatile solvents remaining in the adhesive films that could outgas and cause delamination in downstream processing. The bond chamber also has to keep the wafers centered and rotationally aligned (notch aligned) during the bonding process until the adhesive has set and can restrict movement. The difference between success and failure is a matter of a few microns or tenths of a degree of rotation.

The device and carrier wafers are now being held firmly in place inside the vacuum chamber ready for bonding. The best strategy for putting the two wafers together depends on the state of the adhesive – liquid, gel or solid. Certain adhesives require a significant amount of pressure to achieve good bond strength; whereas, others might squeeze out contaminating the chuck/bond chamber and possibly become bonded to the chuck – not very desirable in a high volume manufacturing environment since cleanup will stop everything. For this reason the bonding force needs to variable - from very low force for liquids to very high force for solids (pseudo solids). Another critical factor is CTE mismatch. Bonding usually takes place at a predetermined steady state temperature. However, for throughput reasons, the bonded pair is not extracted from the bond chamber at room temperature and the differences in CTE of the adhesive, device wafer and carrier wafer will all add stress to the bond while they are cooling. Furthermore, if the cooling process is not done in a controlled manner thermal gradients can also contribute to stress. These types of stresses can manifest themselves in bow, warp and increased TTV – all very undesirable. Temporary wafer bonding for the purposes of 3DIC manufacturing is very challenging and requires a significant amount of materials and equipment engineering to be successful.

As with bonding, the debonding method is largely dictated by the adhesive. Thermal slide debonding has been around for a while and utilizes thermo plastics that soften when heated. Unfortunately, heating is required for processing too so this method's utility is severely limited by thermal budget. Chemical dissolution is an almost stress free process, but it takes a considerable amount of time and requires the use of expensive perforated carriers and lots of solvent. Laser ablation to remove the carrier wafer has been successfully used in production, but prohibits the use of Silicon carrier wafers which are inexpensive and have perfectly matched CTE to

Silicon device wafers. The most recent innovation in separating the thinned bonded wafers from the carrier is room temperature mechanical lift off debonding. The reason this debonding technique is superior is most easily explained by looking at Example 3. By forming a straight debond line across the wafer you minimize the force needed for separation. The debond line length is directly proportional to the amount of force needed for debonding. By peeling the carrier from the device wafer utilizing a straight debond line you get the most efficient debond wave front and thus the least amount of force applied - regardless of the type of adhesive used for bonding. Furthermore, by securing the device wafer to a chuck using a film frame, and only applying force to the carrier wafer during the debond process, the delicate device wafer is subjected to the absolute least amount of stress during carrier separation and is left ready for transport to the final process.



Example 3. The debonding wave front lines "X" and "Y" (yellow dashed lines) are shortest possible. The debond wave line "Z" (red dashed line) represents a non-optimal uncontrolled debond line.

Once the carrier wafer has been removed the final requirement is to clean the device wafer surface that was exposed to the adhesive. Any residue remaining after debonding can interfere with downstream assembly processing such as soldering and thermal compression bonding. Since the wafer is very fragile at this point it needs to be supported and the best method is to use tape on film frame. Since cleaning solvents can also attack the supporting tapes it is important to protect the tape if solvents are used for final cleaning. Fortunately tape manufacturers are developing new tapes specifically for this application and special efforts to protect the tape may become obsolete.

Pressure to bring 3DIC's to market is building and temporary bonding is one of the key elements to enabling low cost high yielding process integration schemes. With the new class of room temperature mechanically lift off adhesives and the latest generation of lift off debonding equipment the path to high volume manufacturing of 3DIC's is well in sight. It won't be long now until these fabulously efficient high performance 3DIC packages are found in many of your favorite consumer electronic devices.

THE AUTHOR

Chris Rosenthal's 15 years of experience in the semiconductor industry range from test and burn-in sockets to extreme front-end photolithography.
His interest in 3DIC, temporary bonding/debonding in particular, started over 5 years ago and since then he has been actively pursuing a universal solution to the challenges associated with thin wafer processing and handling.

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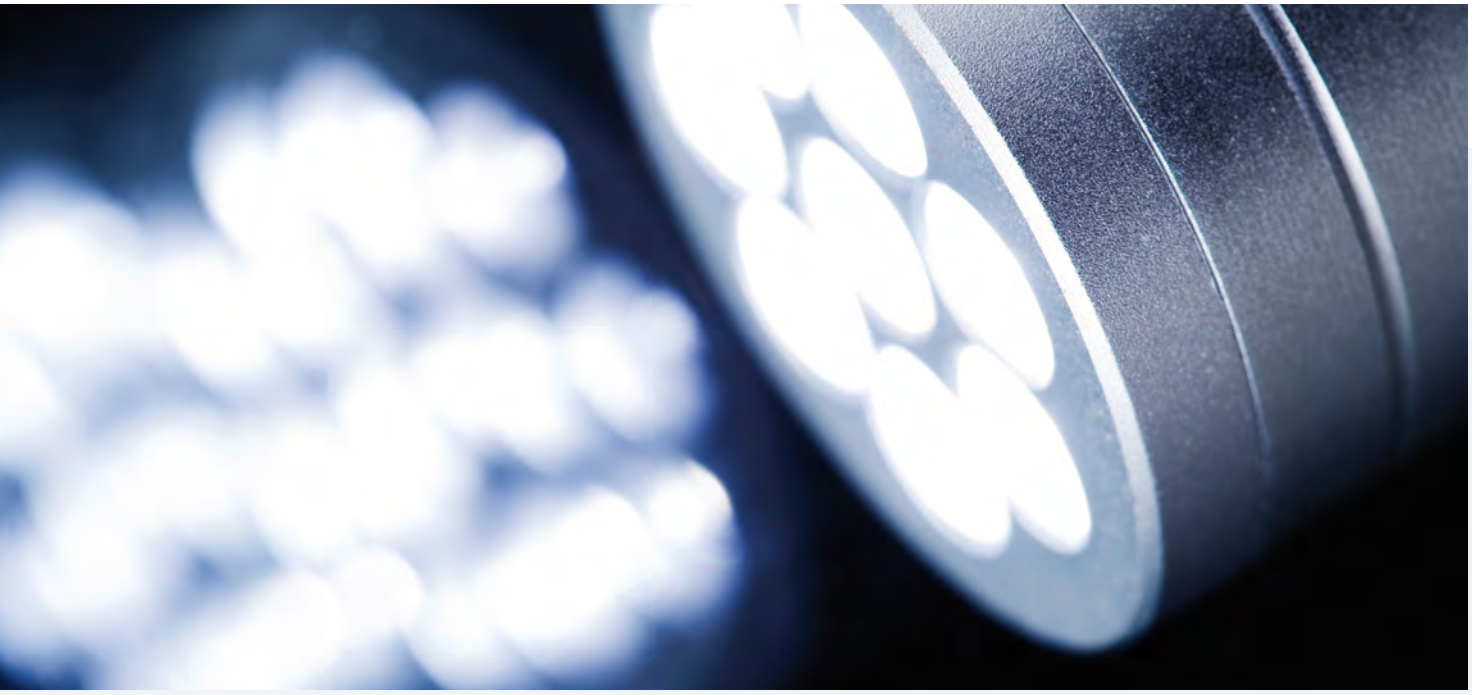

LED WAFER LEVEL PACKAGING – MOTIVATION, CHALLENGES AND SOLUTIONS TO MEET FUTURE COST TARGETS

Michael Hornung, SUSS MicroTec Lithography GmbH, Schleissheimer Str. 90, 85748 Garching, Germany

Since LED became an attractive alternative for general lighting, the market demand for higher brightness, higher efficiency and lower costs was the motivation for improving the LED technology.

Whereas an increase in brightness and efficiency is mostly a question of the LED chip design, a reduction of the costs is in the focus of the manufacturing technology. As Haitz stated in 2000, the cost per lumen falls by a factor of 10 every decade. This, later referred to as Haitz's law[1], is considered the LED counterpart to Moore's law, which states that the number of transistors in a given integrated circuit (IC) doubles every 18 to 24 months. Both laws rely on the process optimization in the production of semiconductor devices. However, at the IC industry it is recognized that an increase in the number of transistors come along with higher costs as manufacturing processes then have to meet higher requirements. These performance related expenses need to be compensated to keep the overall costs low. Several factors could be key to success, e.g. the introduction of standards, the integration of several functions to minimize the number of process steps or the increase of the wafer size from >2" to 300 mm or even 450 mm in the near future.

The most perceived approach to lower LED manufacturing costs is a wafer size increase, with the idea to process as many devices as possible at the same time. This was also a reason for introducing wafer level packaging (WLP) in order to avoid packaging processes on die level. Today, WLP is a standard manufacturing process for the IC industry, but the technology also already found its path into other applications like wafer level cameras where opto wafers and device wafers are mounted together on wafer level to reduce costs significantly. Looking into the

LED manufacturing process today, most steps are on die level after chip singularization. Therefore costs are dominated by the huge number of dies often mounting to several thousand dies on one wafer. It is obvious that WLP is clearly beneficial for LED packaging and it is also the path to success for LED adoption in mass markets like general lighting. A few LED manufacturers already work on WLP for LED. However, there are different boundary conditions to adopt WLP of LEDs. In example there is limited usability of WLP processes on the LED device wafer directly. The final processed LED chips need to be singularized and placed on another board or wafer for further packaging (chip to wafer packaging)[2]. Nevertheless, this fan-out principle gives additional opportunities. First of all, it allows a fast transition to larger wafer sizes like substrates for further substrate level processing. Moreover, it also allows the implementation and integration of additional functionalities to the LED chip module, e.g. electrical connects, Zener-Diode, mirrors or optics drivers (Fig. 1), that further can improve the performance of die and package. Nonetheless, a key aspect for adopting WLP in LED manufacturing is to benefit from the know-how of existing packaging manufacturing technology, processes and from the experience of the equipment suppliers in this industry. SUSS MicroTec, a leading supplier of equipment for WLP for many years, offers a broad solution portfolio. Its mask aligners, coat/develop systems and wafer bonders serve not only the IC wafer level packaging industry but also WLP applications in the field of MEMS, CMOS image sensors and wafer level cameras. For example, a fully automated lithography cluster (Fig. 2) enables wafer processing with highest reliability and lowest operator intervention for the full lithography process. However, automation is just one factor. Furthermore the equipment needs to be tailored to match the requirements of WLP applications. Existing concepts for state-of-the-art LED packages (Fig. 3) combine

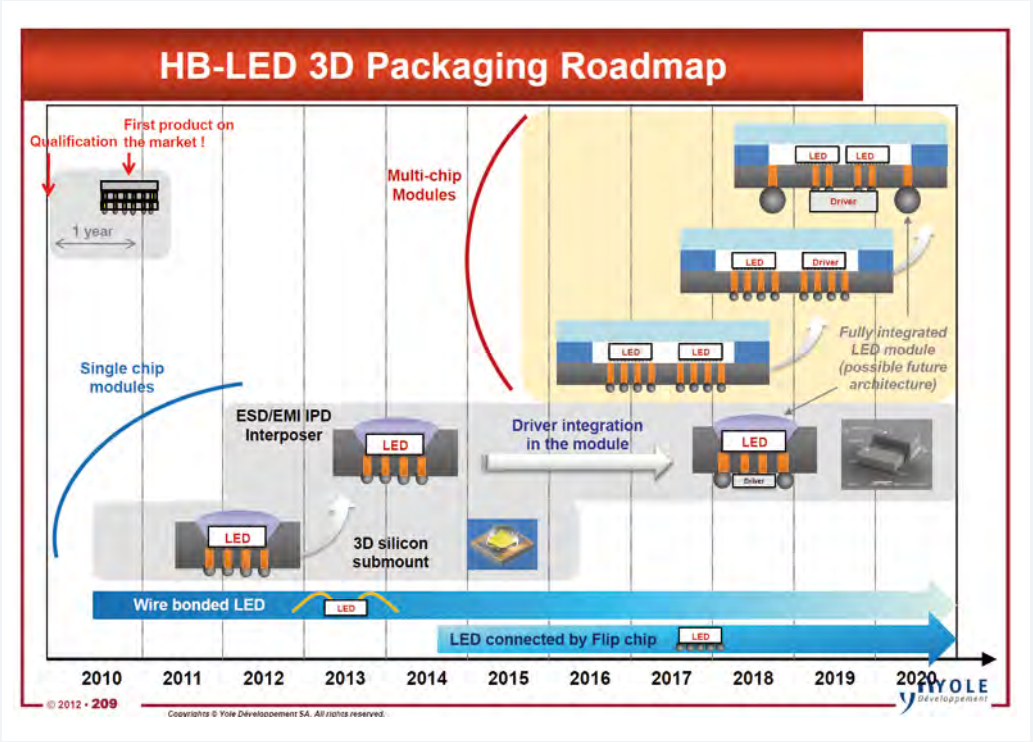

Figure 1. HB-LED 3D packaging roadmap[2]

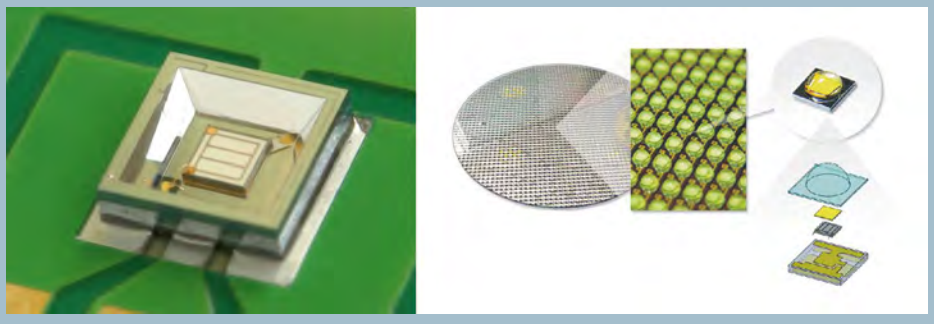

Figure 3. Design concepts for state-of-the-art LED packages based on wafer level packaging technology from Hymite (left) and VisEra (right).

several features. The embedded design with thin silicon membranes at the bottom optimizes the thermal contact and therefore minimizes the thermal resistance. Through Silicon Vias (TSV) provide the electrical contact to the SMD mount and inclined, mirrored sidewalls increase the package reflectivity and improve light efficiency. However, the high topography of such concepts often reaches several hundred of microns and requires innovative lithography techniques and semiconductor manufacturing experiences. Not only the formation of the TSV at the bottom of the cavities are challenging, also patterning of the interconnections from top to the bottom need special equipment and process solutions. Dedicated mask aligner lithography is considered the best to overcome the need for extreme large depth of focus for the exposure process.

For example, SUSS Mask Aligners used in this application are equipped with the SUSS MO Exposure Optics which allows an optimal adaptation of the mask aligner illumination system to the process requirements for best pattern fidelity and highest resolution over severe topography. The innovative illumination system uses two subsequent microlens-based Köhler integrators. The second Köhler integrator is located in the Fourier plane of the first. The new illumination system uncouples the illumination light from the light source and provides excellent uniformity of the light irradiance and the angular spectrum. Spatial filtering allows to freely shape the angular spectrum to minimize diffraction effects at large exposure gaps that can be found when exposing polymers in trenches, groves and vias. In addition telecentric illumination and the ability to precisely control the illumination enables the introduction of resolution enhancement technologies like customized illumination, optical proximity correction and source-mask optimization in mask aligner lithography[3]. In addition, perfect patterning on topographies up to several hundred microns requires conformal resist coating over the whole topography (Fig. 4). Here SUSS MicroTec's proprietary AltaSpray coating technology comes into play; a unique resist deposition method that is capable of producing

Figure 2. SUSS MicroTec LithoFab200. The fully integrated cluster for coating, baking, exposing and developing of substrates from 2" to 200mm is specifically designed for volume production.

Figure 4. 50µm and 150µm L/S in conformal coated AZ 4999 across 200µm deep etched trenches. Exposed on a SUSS MicroTec Mask Aligner with dedicated illumination optics.

highly uniform resist films on different 3D microstructures. The AltaSpray technology is capable of coating 90° corners, KOH etched cavities, Through Silicon Vias or lenses with topographies ranging from a few micron to 600 µm or more. The ability to produce conformal resist coatings on severe topography makes them the ideal choice for Wafer Level Packaging applications like 3D image sensor packaging, MEMS and LED.

Nonetheless, these patterning processes are only the first step. They are used for patterning processes of the silicon package. After the placement of the LED dies to the packaging substrate or wafer, the overall packaging process continues on wafer level with phosphor deposition and lens molding. Finally LED manufacturing could benefit from existing technologies as used for Wafer-Level Camera (WLC) manufacturing. For WLC either all components are manufactured on 8" wafer, the opto-wafers are mounted onto the CMOS wafer, or alternatively the lenses are molded directly on the device wafer on wafer level[4]. The tool of choice for this application is the SUSS MicroTec Imprint Lithography Equipment (SMILE). SMILE allows the imprint replication of structures in the micron to millimeter scale on up to 200 mm diameter areas. SMILE uses soft stamps to perform either an imprint process into a puddle dispensed polymer or a transfer process of material that was previously microdispensed into individual micro molds. In both cases the material is typically cross-linked by UV exposure after pattern shaping.

In the last years, the manufacturing cost reduction of LED devices was mainly accomplished by increased equipment throughput, lower Capex, yield improvements and a higher degree of automation using dedicated tools for LED manufacturing. Further significant cost reduction is expected by the adoption of WLP approaches that are already field proven in other industry applications like IC and MEMS WLP.
SUSS MicroTec offers a wide product portfolio of high quality equipment which provides tailor made solutions and processes to meet the specific requirements of tomorrows LED WLP designs.

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Michael Hornung is Technical Marketing Manager at SUSS MicroTec Lithography based in Garching, Germany. During his career at SUSS MicroTec he passed further functions. He was project manager in R&D, responsible for the (nano) imprint technology and other new technologies for mask aligners. He also worked as application engineer for a while and led the application group at SUSS MicroTec for two years.
Before he joined SUSS MicroTec he was project manager at CERN in Geneva, Switzerland, working at the inner detector for the ATLAS project.
Michael Hornung holds a Ph.D. degree in Natural Science from the University of Freiburg, Germany and an MBA from the University of Applied Science of Ludwigsburg, Germany.

SPRAY COATING NEGATIVE TONE RESISTS

Kento Kaneko, SUSS MicroTec Lithography GmbH, Schleissheimer Str. 90, 85748 Garching, Germany

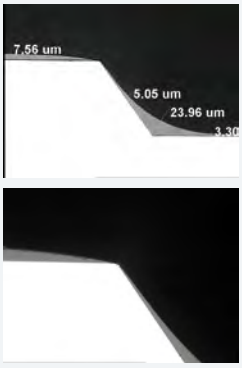


Figure 1. Microscope pictures after spray coat, soft bake at 95 °C for 180 sec (conventional process parameters). No resist coverage at corner, very thin resist around corner, very thick resist at bottom corner. Sample: Etched by KOH, depth 100 µm, top opening 800 µm, trench length 10000 µm.

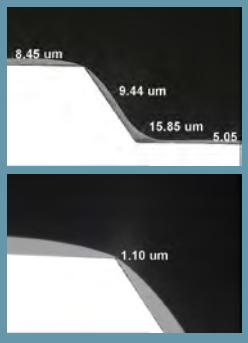


Figure 2. Microscope pictures after spray coat, exposure, post exposure bake with at 95 °C for 180 sec (inverted process). Resist maintained at corner: 1.1 µm after baking step. Resist thickness at bottom is reduced by approximately 33 % compared to the conventional process. Same sample as in Figure 1.

1. INTRODUCTION

Spray coating is an essential coating technology for depositing resists across deeply etched structures, such as a MEMS device etched deeper than 100 µm. Conventional spin coating has limitations when processing structured wafers with severe topography. Spin coated resist often fills the entire structure. This leads to difficulties in the following lithography steps. Thus, industry requires a method to apply resist conformally. Spray coating technology is an effective method for performing conformal coating over deep etched structures.

In view of conformal coating, positive tone resist is desirable, as already adopted for many applications such as etch mask or electroplating. An important property of positive tone resists – such a DNQ/Novolak resist - is the comparably high glass transition temperature that is above the soft bake temperature. During soft bake the resist thickness changes depending on corner angle and location. Typically the resists thickness reduces at the top corner and increases at the bottom corner. However, when using positive acting resists, reasonable conformal coating can be achieved. The negative tone resist is a UV plastic material that is hardened during UV exposure. Unlike the previous case, during the soft bake step, the resist becomes soft and surface tension deteriorates the conformality of the resist layer. Often only a very thin residual resist coverage or no resist at all is observed on the top corner after soft bake. For these reasons, industry preferably adopts positive tone spray resists. Nevertheless, using negative tone resists is still important for some specific applications. Examples are the SU8 resist from MicroChem/ Nippon Kayaku and the THB 151N resist from JSR. SU8 is often used as a permanent resist structure and THB151N is an important plating resist.

2. PERMANENT LAYER (SU8)

Conformal coating with SU8 is frequently requested for many MEMS applications. SU8 has very unique properties, making it excellent dry etch resistant and enabling high aspect ratio imaging. Several process evaluations have been made using different topographic structures.

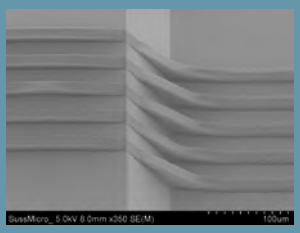
2.1 SPRAY COATING

2.1.1 POPPING DEFECTS

Bubble popping defects are observed during the soft bake step when diluted SU8-50 is spray coated as a layer thicker than 5 µm. Multiple coatings are thus required to apply a SU8-50 layer thicker than 5µm. This problem was solved by changing to the SU8-3000 Series. SU8-3050 allows, without popping defect, reaching already on a single coat, more than 20 µm of resist thickness. This is due to the fact that theSU8-3000 series contains Cyclopentanone, while the SU8 series contains gamma-Butyrolactone. Since the boiling point of Cyclopentanone is 131 °C and the boiling point of gamma-Butyrolactone is 205 °C, using a lower boiling point solvent might help to reduce the stress accumulation during the soft bake step and therefore helps to avoid popping defect.

2.1.2 CONFORMAL COATING

To achieve conformal coating, many tests have been done by changing spray coating parameters. However, SU8-3050 flows to the bottom of the topography, leaving the top corner exposed after the soft baking step, as shown in Figure 1. This phenomenon is observed with different series (SU8 2000 / KMPR series). Surface tension generated during the soft bake step acts so that the thickest part (bottom corner) pulls resist from all other the regions. The glass transition temperature of unexposed SU8 film (60 °C) is lower than soft bake temperature (95 °C). Thus,



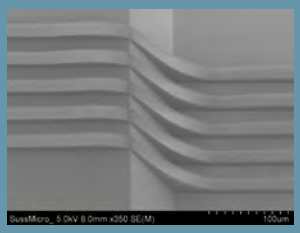
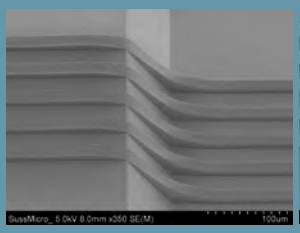


Figure 3. SEM pictures after develop, 30µm Line and space pattern.
Left: Conventional process sequence. No resist at top corner and very thin around sidewall and bottom.
Right: Invert process sequence. Resist covers top corner.



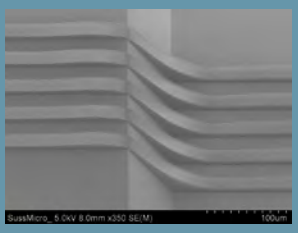


Figure 4. SEM pictures after develop, 30µm Line and space pattern.
Left: 100mJ/cm²
Right: 250mJ/cm²

SU8 becomes liquid and it is pulled into the bottom corner during soft bake by the surface tension. As shown in Figure 1, the thickness of the resist at the bottom corner is significantly thicker than at any other location. Changing the spray coating process parameter is not an efficient approach.

For this reason, SU8-3050 needs to be UV processed before thermal processing step. Process sequence is modified as below: Exposed SU8-3050 layer becomes harder by cross linking during post exposure bake. This prevents the SU8-3050 layer from flowing into the bottom corner while maintaining the coverage at the top corner. Figure 2 shows images of the inverted process. Approximately 1.1µm resist is observed on the corner after post exposure bake at 95°C for 180 seconds.

Conventional: Spray Coating --> Soft Bake --> Exposure --> Post Exposure Bake

Invert: Spray Coating --> Exposure --> Post Exposure Bake

2.2 LITHOGRAPHY

Lithography test is done to verify that inverting the process steps has no influence on the lithography property. The process is then qualified by comparing its results to the ones from the conventional process. Figure 3 shows two SEM images from both processes after development. No influence is observed such as poor adhesion, worse resolution or requiring a different develop time as compared to the conventional process. During the exposure step, the SU8-3050 layer surface is sticky since it is not soft baked. Therefore, a contact between mask and coated wafer must be minimized in order to avoid mask and coated wafers sticking to each other. The SUSS MicroTec global WEC or NCGS (Non Contact Gap Setting) options are therefore in this case ideal. The exposure energy affects the resist thickness at the top corner. As shown in Figure 4, there is hardly any resist on top corner when exposing with a dose of 100mJ/cm². Resist coverage, however, becomes sufficient when exposing with a dose of 250mJ/cm². Higher exposure dose is thus critical in order to initiate a more effective cross linking.

Process detail:

- Resist: Diluted SU8-3050
- Spray coating: Arm speed 120mm/sec./ Chuck Temp. 60°C/ Nitrogen 0.1MPa
- Exposure: SUSS MA/BA 6 Gen2 / LGO optics / 250mJ/cm²
- Soft/Post Exposure Bake: SUSS HP8 TT/ 95°C for 180sec
- Develop: Immersion develop with PGMEA 180 seconds and IPA rinse.

3. BUMP MOLD RESIST (THB 151N)

THB 151N is used as bump mold for solder bump application in the advanced package technology. The same phenomenon as for the SU8 resists is also observed in this case.

3.1 SPRAY COATING

The same evaluation performed as for the SU8 resist, comparing standard and inverted process sequence, was carried out in the THB 151N case. As shown in Figure 5, the inverted process helps to keep the resist on corners after the soft bake.

4. CONCLUSION

Inverting the process sequence is an efficient approach and allows spray coating any resist with a glass transition temperature lower than its soft bake temperature. Exposure initiates cross linking and changes the material properties, helping to minimize the resist deformation due to the surface tension during the soft bake step. Process optimization is strongly dependent on the structure design, i.e. a smaller process window is expected with vertical etched topography.

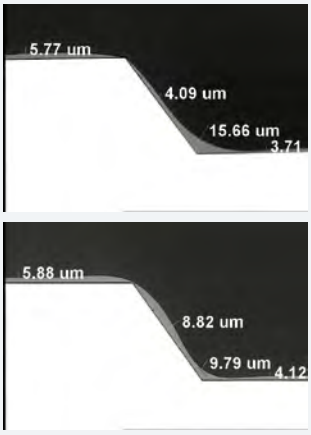


Figure 5. Microscope pictures comparing the conventional and the inverted process sequences
Top: Conventional process sequence
Bottom: Inverted process sequence
Soft bake: Suss HP8 TT / 90°C for 180sec.
Sample: Etched by KOH, depth 100µm, top opening 800µm,trench length 1000µm

THE AUTHOR

Kento Kaneko
2000 March: Graduated university, studied Applied Mechanics
2000 Apr – 2006 Aug: Act as product specialist and application engineer at SMT KK. (SUSS Japan)
2006 Sep – Current: Work as application engineer, focus on spray coating.

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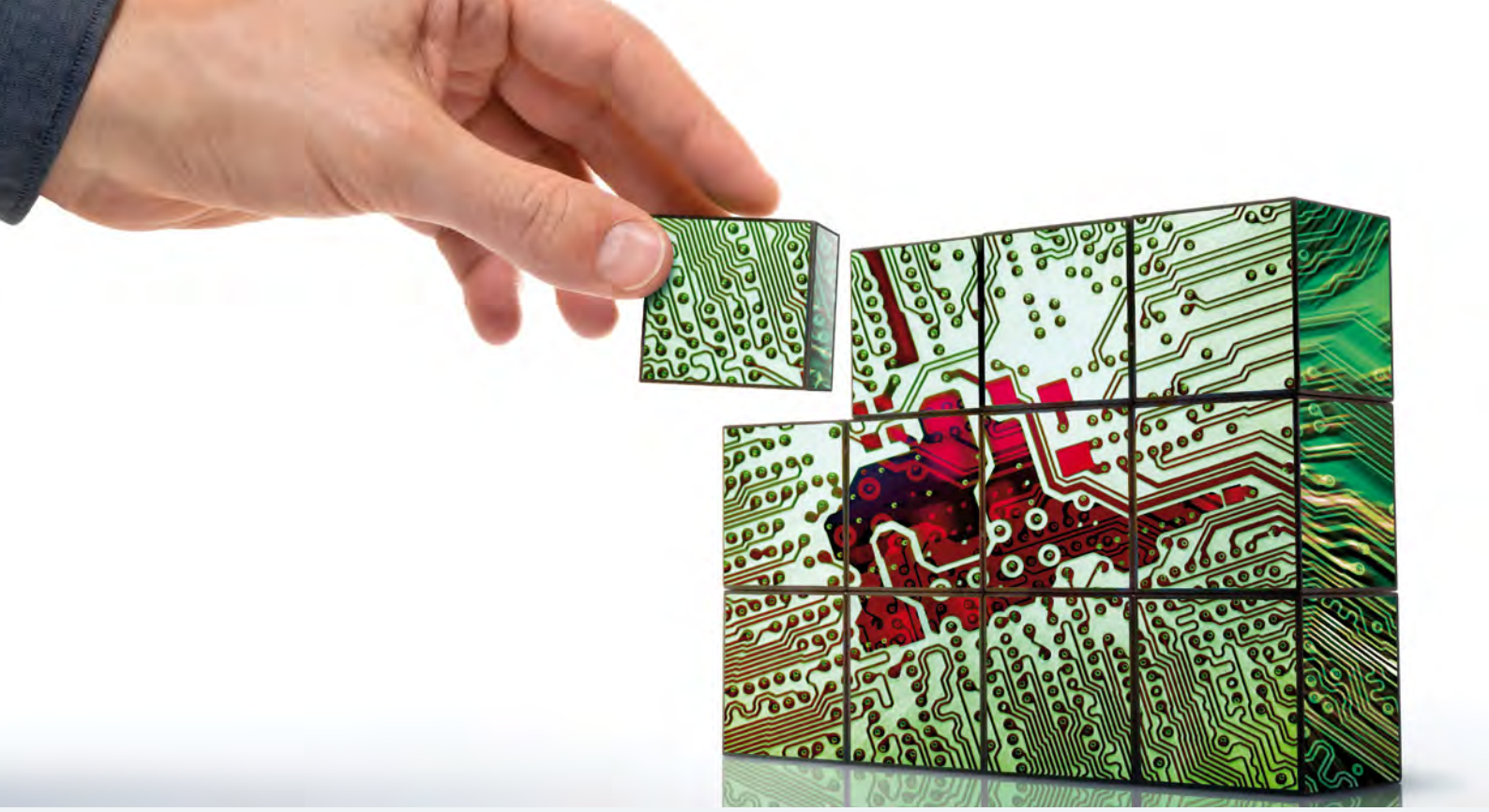

SUSS MICROTEC HOSTED ASIA TECHNOLOGY FORUM

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SUSS MicroTec hosted the Technology Forum in Asia that focused on the latest developments in Advanced Packaging, materials, manufacturing technologies and market trends in 3DIC and Wafer Level Packaging. The event took place on three separate dates at three main industry centers, first in Singapore, followed by the events in Hsinchu, and Shanghai.

Yole Développement's Taiwan CTO, Pascal Viaud, moderated the events and presented Yole's latest analysis on 3D TSV technologies and 3D market trends. "It was a pleasure to moderate this great event. The forum gathered leading companies from across the industry as well as world-renowned research institutes sharing insights and exchanging experience. Especially with 2013 being expected to be the key turning point for the true 3DIC technology implementation in significant volume, the forum attendees were eager to hear all about the latest developments and advances from the experts." Industry leading OSAT (Outsourced Assembly and Test) STATS ChipPAC as well as the research institutes ITRI (Industrial Technology Research Institute) and SIMIT (Shanghai Institute of Microsystem and Information Technology) shared an overview of their current status on the development of 3D Integration. SUSS MicroTec presented latest achievements and developments in Temporary Wafer Bonding and Debonding, Lithography and Laser Processing.

"Semiconductor mid-end processing technologies like 3D Integration and Advanced Packaging are gaining importance and have come into the strategic focus of many global players. We hosted the Asia Technology Forum to present our solutions and discuss the remaining technological challenges with customers and cooperation partners", says Frank P. Averdung, President and CEO of SUSS MicroTec "Understanding the obstacles and applying this knowledge to the development of next generation production solutions is prerequisite for the industry's success."
The forum featured representatives from Industrial Technology Research Institute, Shanghai Institute of Microsystem and Information Technology, STATS ChipPAC, Yole Développement, Fraunhofer IZM Berlin, GenISys, HD MicroSystems, Brewer Science and PVA TePla.

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	IMAPS Device Packaging	Scottsdale, AZ, USA	Mar 11 - 14
	MIG MEMS Executive Congress EU	Amsterdam, Netherlands	Mar 12
	The Optical Fiber Communication Conference	Anaheim, CA, USA	Mar 17 - 21
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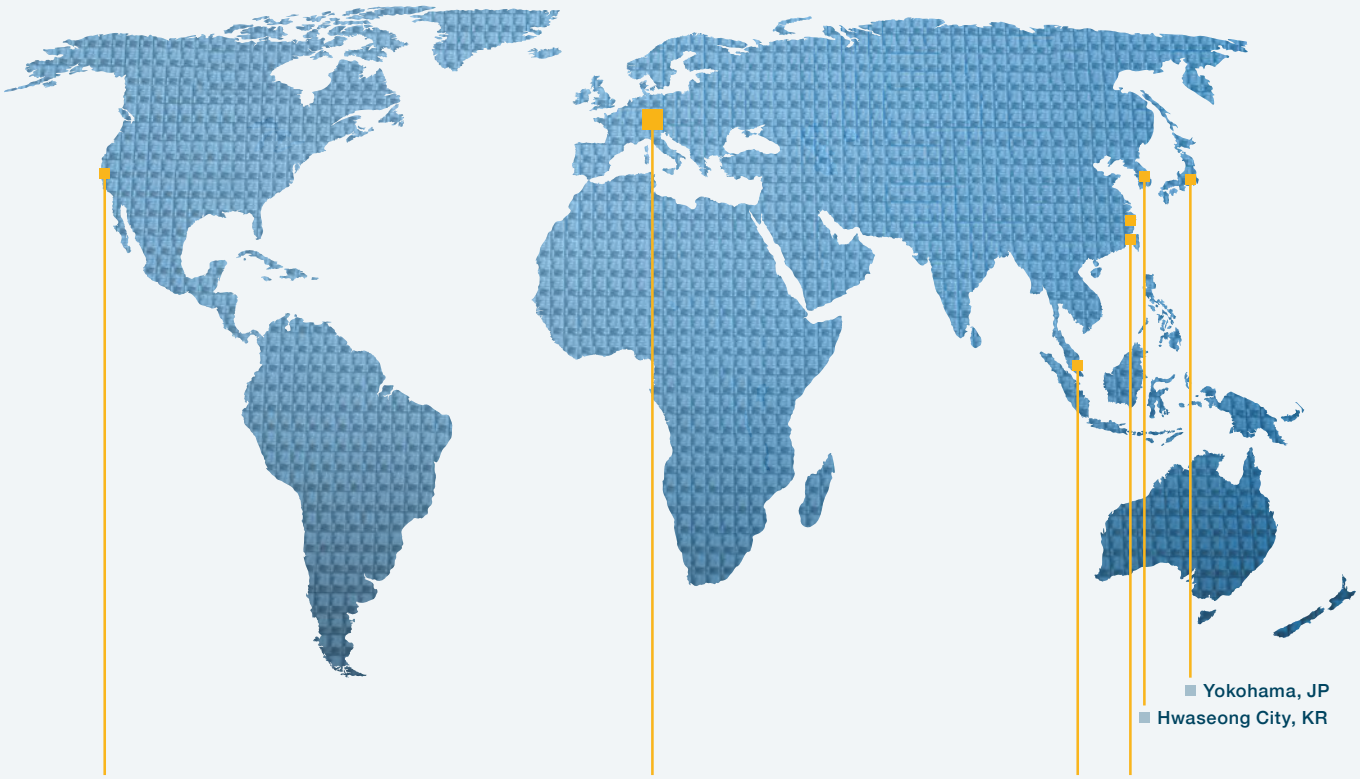

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Schleissheimer Str. 90
85748 Garching
Germany
info@suss.com

Chairman:
Dr. Stefan Reineck

Executive Board:
Frank Averdung (CEO)
Michael Knopp (CFO)

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