SUSS report+

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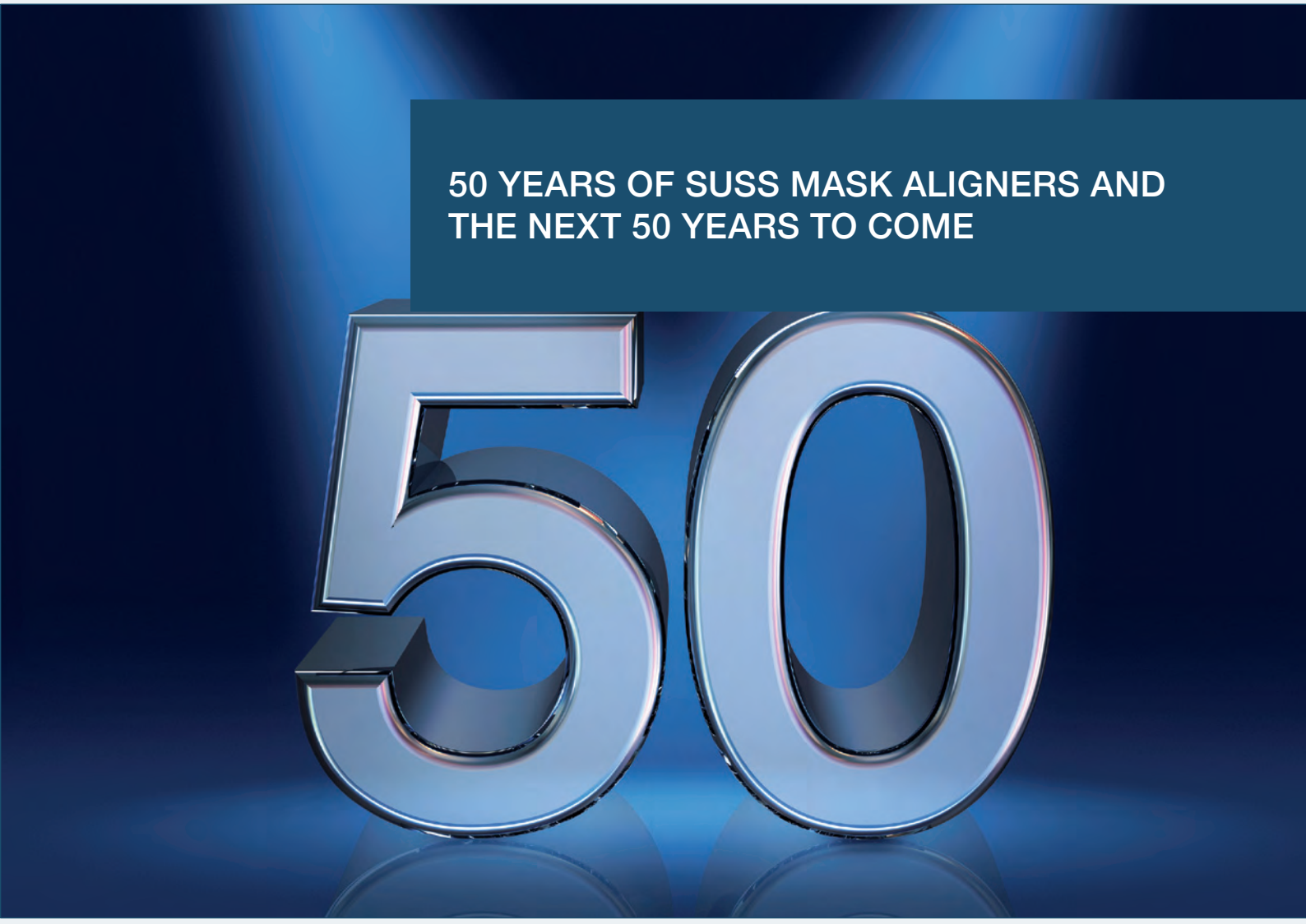

50 YEARS OF SUSS MASK ALIGNERS AND THE NEXT 50 YEARS TO COME

Partners for Technology Leadership

3D Topography Mask Aligner Lithography Simulation

In the Spotlight

MPT Coating Service Now Available from Compugraphics Jena GmbH

SÜSS MicroTec

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Frank P. Averdung
President & CEO
SÜSS MicroTec AG

This year SUSS MicroTec celebrates a very special anniversary. Fifty years ago the first SUSS mask aligner was shipped to a customer who started then the production of integrated circuits.
It's an opportunity to look back:
Hardly any industry has developed as rapidly, produced so many innovations, and thereby influenced our daily life as fundamentally as the electronics industry. Especially remarkable is the development of the semiconductor sector, which laid the foundation for the internet, mobile communications, the digital lifestyle and much more.

In the mid-20th century, a new semiconductor component – the transistor – allowed to control current through an electrical signal. It became the fundamental building block of modern electronic devices. Soon after various components such as capacitors, resistors, and transistors could be combined on a single substrate, creating an integrated circuit. This was the breakthrough for the modern electronics industry.
From then on, these integrated circuits have experienced rapid progress. Today billions of transistors can fit on a few square millimeters forming high performance chip of which each has more computing power than the entire moon mission in the sixties.

With its highly successful mask aligner product line SUSS MicroTec has been playing a major role in the semiconductor manufacturing industry since its beginnings in the 1960s. Offering superior exposure results with precise and at the same time also robust and reliable systems the SUSS MicroTec mask aligner has become the production work horse for the industry. It is the core of our brand renowned for accuracy and reliability.
With its lithography expertise SUSS MicroTec has enabled essential processing steps for mid and back end lithography for the last 50 years.

Looking ahead it is obvious that mankind will continue to demand even faster computers, more powerful cellular telephones, and more complex electronic devices.
The mask aligner will remain the product of choice as a reliable and mature solution for full-field lithography. With new manufacturing requirements emerging alternative technologies like UV projection lithography or laser ablation will complement proximity exposure.
Through the acquisition of Tamarack Scientific in March 2012 - which is now SUSS MicroTec Photonic Systems - SUSS MicroTec has firmly established itself as the leading provider of comprehensive mid- and backend exposure solutions.

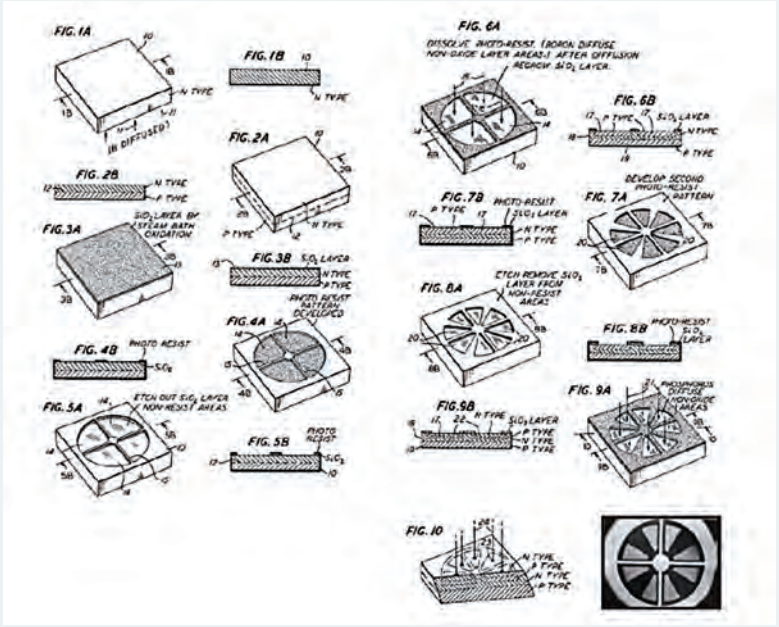
In this issue of the SUSS report you`ll read about innovative tools and solutions that highlight the essential role of lithography in the semiconductor industry … back then, now and in the future.

50 YEARS SUSS MASK ALIGNER

Ralph Zoberbier SUSS MicroTec Lithography GmbH, Schleissheimer Str. 90, 85748 Garching, Germany

This year we are celebrating the 50th anniversary of the SUSS mask aligner. Hardly anybody ever imagined that this type of photolithography equipment that was introduced many decades ago still has its place in today's manufacturing and research facilities in the semiconductor and related industry.

Today it is the most common thing to surf the internet with a 3G smart phone, we are driving cars with hundreds of sensors and we are watching movies at home on huge high definition flat screen TVs. So what is the role of a mask aligner in today's electronic industry? Even though the mask aligner disappeared from frontend semiconductor applications, it is widely used to efficiently pattern advanced chip packages such as Wafer Level Packaging of memory or processing units, various LEDs, power devices or MEMS (Micro Electro Mechanical Systems) structures needed to build the devices or systems used in high-tech devices. In addition, thousands of engineers and students are working everyday on mask aligners during their education and industrial research.



Detailed process flow for the manufacturing of a stepping transistor from Jules Andrus' US patent 3,122,817, filed on August 15, 1957. Two photoengraving steps were applied to build the device consisting of four PNPN switches arranged in the four quadrants of a circle. A photograph of the resulting stepping transistor, taken by Lucian D'Asaro, a member of Ian Ross' group at Bell Labs is shown in the lower right corner

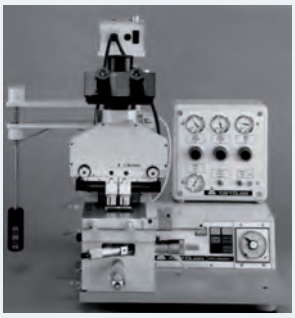
Until today the mask aligner lived through continuous changes in the industry and respective applications. Its career began at a time when smart engineers invented their first semiconductor devices. We were in the middle to late 1950s when the first initiatives with groundbreaking achievements were undertaken.

One of the very first devices was developed and manufactured at Bell Labs. Two photo-engraving steps were used to build a device consisting of four PNPN switches. This invention was quickly published and patented and shortly afterwards photolithography became public knowledge. It is considered as one of the inventions that introduced photolithography to the semiconductor industry.

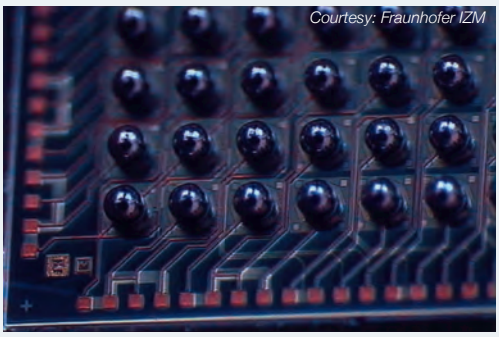
With the need of a mass production capable process, specific photolithography equipment was required by the industry. Already existing systems from the printed circuit board industry could not be adopted as they were designed to pattern features in the millimeter range and that is why the semiconductor industry needed to develop its own photolithography tools. The tool of choice was the so-called mask aligner, which uses UV light to shadow print a mask pattern onto a substrate which has been coated with a

photosensitive resist.
Kulicke & Soffa was one of the first mask aligner suppliers in the market and quickly captured the main market share in the early 1960s. Back then a small Bavarian company called Karl Süss, now SUSS MicroTec, which was founded in 1949, worked as sales representative for Leitz Microscopes. Their portfolio consisted of a variety of supplementary equipment, such as light sources, precision cross tables, micrometer screws, other mechanical and optical parts. At that time, the semiconductor industry could not get equipment off the shelf and Karl Süss was often asked to modify and adapt Leitz parts to the specific needs of this prospering industry.

Finally in 1963, 50 years ago, Karl Süss was asked by SIEMENS to build an exposure system consisting of an exposure lamp, microscope and cross table. The first SUSS mask aligner was born!
Since then the SUSS mask aligner changed a lot in design and capabilities driven by ever changing application requirements and customers, even though the core technology remained the same. The system of the 1960s was named MJB, which is Masken-Justier-Belichter, the German term for the Mask Aligner. The systems were designed to expose 1"-2" substrates, which was the common wafer size of those years.
Besides research, mask aligners were mainly used to manufacture discrete devices and at a later stage integrated circuits (IC) and its transistors. However the semiconductor industry moved quickly to higher resolution requirements. The mask aligner with its imaging capability limited to resolutions down to approx.1µm, ran out of steam and was replaced by early projection lithography tools. Whenever a main application like frontend semiconductor lithography moved out of the process window of the mask aligner one quickly was predicting the death of the mask aligner. Many of the main mask aligner manufactures like CANON discontinued their product lines. However, Karl Süss continued to develop and enhance its systems. Finally, new industry segments and applications were developed which needed cost efficient lithography processes. SUSS mask aligners were introduced to those semiconductor related applications and ensured a continuous growth of the company in these niche markets. When personal computers became a household item during the 80s, the demand for logic and memory chips exploded. Answering the growing demands of the industry, Karl Süss expanded the semiconductor mask aligner portfolio with fully automated machines as a logical step. At that time the company introduced their first fully automatic production mask aligner MA150, which replaced the former semi-automatic systems MA45 and MA56. The new system was designed to process substrates and wafers at high speed with no operator intervention which required computer aided pattern recognition and automated wafer handling. Still equipped with a similar exposure technology like an MJB, the system quickly became the workhorse of specific applications in this industry. Among others, it was used for mass production of early microsystems like read/write heads used on hard disk drives and print heads for inkjet printers.



Karl Süss MJB3 manual Mask Aligner



Courtesy: Fraunhofer IZM

In the 1990s a new and innovative semiconductor backend technology was developed and introduced to the market – the Wafer Level Packaging. The semiconductor industry already

MJB3
R&D and small series mask aligner
up to 3" wafers

1960s

1960 1961 1962 1963 1964 1965 1966 1967 1968 1969

MA25
Doubleside mask aligner
up to 5" wafers

1970s

1970 1971 1972 1973 1974 1975 1976 1977 1978 1979

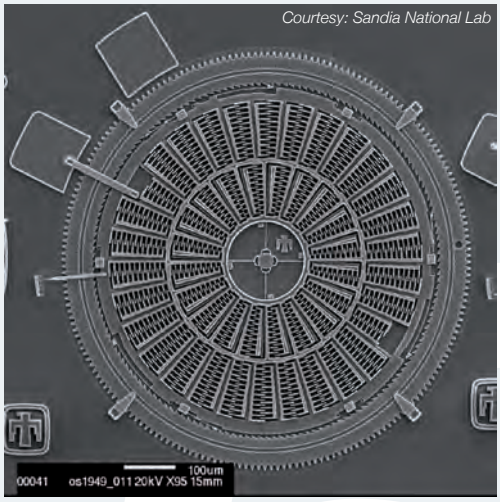
MA150
Production mask aligner
up to 150 mm wafers/substrates

1980s

1980 1981 1982 1983 1984 1985 1986 1987 1988

produced their ICs on 200mm wafers. Due to the complexity on the chips, innovative packaging technologies were needed to replace common wire bonding techniques. The high number and decreasing size of the bond contacts of the chips outpaced the limitations of the available wire bonding equipment and asked for advanced packaging technologies. Among others, at that time FlipChip technologies were developed, which required a cost efficient patterning of the solder contacts on the chip. With feature sizes of around 100-200 µm and the tremendous cost pressure in this segment, the use of the "old fashioned" mask aligner in the semiconductor back-end was a natural choice. Karl Süss quickly responded to the new industry trend with the development and launch of a 200 mm mask aligner – the MA200. With the successful market introduction the company became a leading supplier to IC manufacturers like INTEL and IBM. With the move of the industry to 300mm in the late 90s, SUSS MicroTec (now a publicly held company) developed and introduced the first 300mm mask aligner to the market – the MA300. Besides the wafer size transition from 150mm over 200mm to 300mm, the continuous pressure to improve productivity and yield led to several equipment enhancements. Novel pattern recognition techniques needed to be implemented and in addition frontend-like automation standards were introduced in the backend and its equipment. Still today the latest versions of the 200 and 300mm production mask aligner are widely used in the growing segment of Advanced Packaging and are considered as important key products of SUSS MicroTec. For many years now, SUSS MicroTec successfully defends its market position in this sector and is considered as one of the market leaders.

Starting back in the late 90s, two additional major applications impacted the development and change of the SUSS mask aligner product portfolio. MEMS and LED made the momentous move from the R&D level to industrial production.



Micro-Electro-Mechanical Systems, or commonly called MEMS, is a technology that in its most general form can be defined as miniaturized mechanical and electro-mechanical elements (i.e. devices and structures) that are made using the techniques of micro fabrication. Very similar semiconductor processes and adapted semiconductor equipment is used for the manufacturing. The MEMS device development is mainly driven by the demand of consumer electronics, automotive and medical applications. Companies like BOSCH, STMicroelectronics and HP are

MA200CC
Production mask aligner
up to 200 mm wafers

1990s

1989 1990 1991 1992 1993 1994 1995 1996 1997 1998 1999

MA300Plus
Production mask aligner
up to 300 mm wafers/substrates

2000

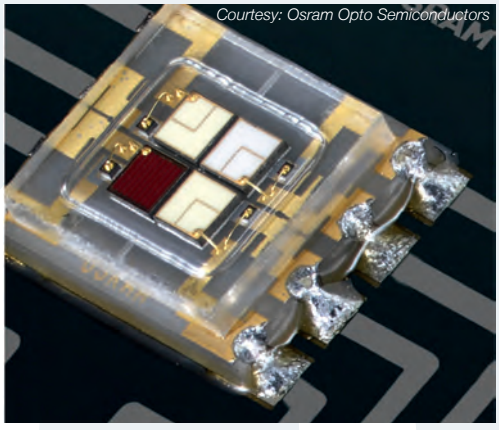
2000 2001 2002 2003 2004 2005 2006 2007 2008 2009

MA200Compact
Latest generation production mask
aligner up to 200 mm wafers/substrates

2010s

2010 2011 2012 2013

leading players who manufacture devices like accelerometers, gyroscopes and inkjet nozzles that are based on MEMS processes. Those devices saw tremendous growth. Mask aligner capabilities match many of the patterning requirements and are used in device manufacturing but also for MEMS packaging processes. Especially thick photoresist patterning and tricky substrate handling techniques, like edge handling, had to be developed and implemented into the mask aligners.


Courtesy: Osram Opto Semiconductors

Light-emitting diodes (LEDs) were a rapidly evolving technology. LEDs have been used for years in various applications like mobile appliances, LCD backlights and front or rear lamps in automotive applications. Today they are becoming viable for many general lighting applications, usually referred to solid-state lighting (SSL). The most relevant examples of LED lighting applications are indoor applications in commercial, industrial, and residential environments, outdoor applications like street and parking lights, and architectural and decorative lighting where LEDs were initially adopted because of their ability to emit the wide spectrum of colors. SUSS mask aligner have been used for patterning conductive layers in LEDs since the very beginning. A typical LED device consists of 3-9 different lithography layers and requires feature sizes of 3µm to several 10ths of microns. Fragile and warped wafer handling is a key element that is needed on a lithography tool in those applications. The early involvement of SUSS MicroTec in close cooperation with leading device manufacturers in the development and the final production was the reason for the company's outstanding market position. Today, SUSS MicroTec is the leading lithography equipment supplier and has installed more than 250 exposure systems for this application worldwide.

Over the last 50 years different generations of technicians and engineers at SUSS MicroTec gradually improved the mask aligner technology and finally created a high-tech product that delivers excellent and cost efficient lithography performance in various applications. The company introduced innovative technologies and improvements like diffraction reducing exposure optics, front-to-back side alignment, infrared alignment and source-mask optimization, based on SUSS MO exposure optics. Today SUSS MicroTec owns about 70% of the world-wide market of mask aligners and is considered the premium supplier when it comes to proximity and contact printing.

A toast on 50 years of SUSS mask aligner and the next 50 years to come!

THE AUTHOR

Ralph Zoberbier graduated in Precision Engineering and Microsystems Technology from the University of Applied Sciences in Nuremberg. He joined SUSS MicroTec in 2001 as R&D Project Manager and became International Product Management Aligner in 2005. Since 2010 he leads the Aligner Product Management team as Director Product Management. With the recent acquisition of Tamarack Scientific Inc. his area of expertise was extended by complementary projection lithography and laser process technology. In 2006 Ralph gained a MBA degree in Entrepreneurship at Louisville University, Kentucky

MPT COATING SERVICE NOW AVAILABLE FROM COMPUGRAPHICS JENA GMBH

Dr. Dietrich Tönnies, Liming Chai, SUSS MicroTec Lithography GmbH, Schleissheimer Str. 90, 85748 Garching, Germany

MPT™ Technology (Mask Protection Technology) was developed by Motorola Labs in the 1990s: In order to reduce the usually high mask cleaning frequency when exposing wafers by contact printing a thin film of a fluorinated hydrocarbon polymer is spin coated onto the photomask. Similar to a Teflon coating this fluorinated polymer reduces the surface energy of the mask making it more difficult for resist residues and particles to stick to it. The transparency of the mask for broadband or deep UV wavelength is not compromised and the film thickness of approximately 100 nm is small enough to ensure contact printing results comparable to unprotected photomasks.

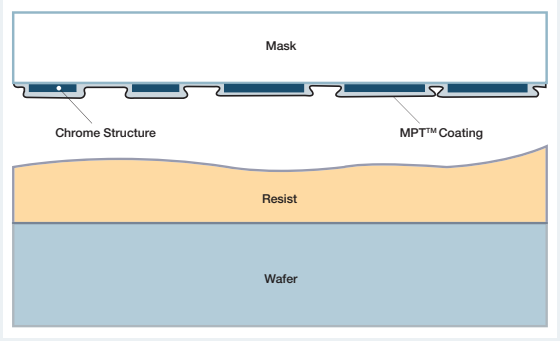


Figure 1. MPT™ Technology provides a low-surface-energy coating on the structured side of the mask. During contact exposure the affinity of resist or particles to stick to the mask is significantly reduced.

MPT™ Technology was originally licensed by Motorola to SUSS MicroTec with the agreement to allow customers to purchase MPT™ licenses or MPT™ coating services through SUSS MicroTec. With the sale of SUSS MicroTec's photomask division in October 2011 this agreement was transferred to Compugraphics. Advantage for potential users is that the MPT™ coating service – previously limited to the North American market – is now also available for the European market through Compugraphics Jena.

MPT™ Technology is primarily interesting for users of mask aligners who use contact exposure technology to print resist structures between approximately 3.0 and 0.5 µm. Without MPT™ coating a mask that is used for contact printing has to be cleaned frequently and – for the most demanding processes – even after each exposure. Frequent mask cleaning limits the lifetime of the mask and reduces the productivity of the exposure equipment. A protection coating, therefore, is highly desirable and the cost of the coating is easily justified by cost savings from the extension of mask lifetime.

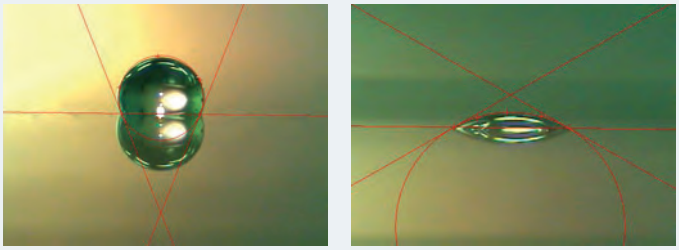


Figure 2. Left: DI water droplet with a contact angle of 111.7° on an MPT™ protected mask. Right: DI water droplet with a contact angle of 29.7° on an unprotected mask.

Mask without MPT™ protection after 100 HC prints

Mask with MPT™ protection after 100 HC prints

Figure 3: Optical microscopy images of an unprotected and an MPT™ protected 7-inch photomask after processing 100 wafers in hard contact (HC) mode (each image represents an inspection area of 0.628mm×0.468mm). For each mask 6 locations with the highest level of contamination were selected (not including the edge bead area). Without MPT™ protection large chunks of photoresist exceeding even 100µm in size were found on the photomask and contaminate chrome coated and the transparent areas. With MPT™ protection the mask stays significantly cleaner.

The MPT™ coating process in principle is simple. The MPT™ agent is filtered and is dispensed onto the mask. It is then spin coated to a final layer thickness of about 100nm. During a bake step special functional groups of the polymer molecule establish the bond to the mask. The effectiveness of the coating can be easily tested by contact angle measurements. With a properly processed mask contact angles above 100° are achieved compared to approximately 40° or even lower for an unprotected mask (Figure 2).

In order to prove the efficiency of the MPT™ coating an unprotected and a MPT™ protected mask were used for 100 consecutive hard contact exposures without cleaning the masks. Both masks were inspected by optical microscopy. Figure 3 shows the six most heavily contaminated areas of each mask. It is obvious that without MPT™ protection the mask was contaminated with large resist residues while the protection layer reduced the amount of resist that stuck to the mask by orders of magnitude.

There are, however, certain characteristics and limitations of MPT™ Technology that a user should be aware of. Mask cleaning is not eliminated but still necessary, although at a much lower frequency. Common mask cleaners have problems cleaning MPT™ coated masks because the cleaning agent will not wet the mask surface and will drop off from the mask easily. MPT™ protected masks have to be cleaned by immersing them into a solvent bath optionally supported by slightly brushing the mask.

MPT™ coatings are organic and less hard than the photomask. Thus they can be subject to wear especially if the wafers have sharp protruding elements or if particles are squeezed between mask and wafer. It can, therefore, be necessary to renew the MPT™ coating by stripping the old one and coat a new layer. All services including MPT™ coat, MPT™ strip and cleaning of an MPT™ coated mask are available from Compugraphics Jena GmbH.

THE AUTHORS

Dr. Dietrich Tönnies is head of the Applications Department and Demo Lab at SUSS MicroTec's headquarter in Garching, Germany. He joined SUSS in 1997 as Product Manager for Mask Aligners and for many years was responsible for developing the company's Advanced Packaging market.

Liming Chai graduated in 2007 from the University Dortmund with a Dipl.-Ing. degree in Microsystems Engineering. She started her career at Suss in July 2008 as clean room Engineering and worked a part of MPT™ (Mask Protection Technology) project.

SEQUENCE 1

AUTO-ALIGNMENT INSIGHTS

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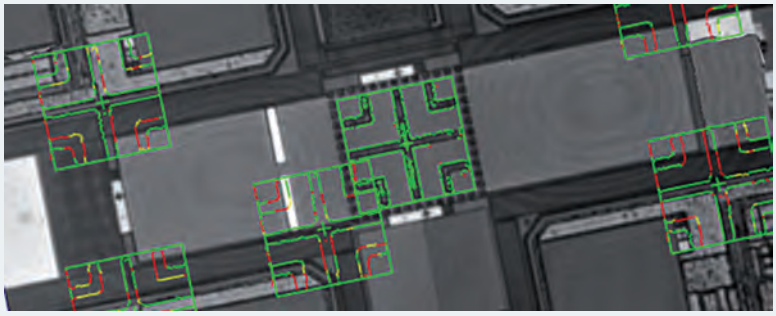
This article is the first part of a short series of articles focusing on pattern recognition and alignment in SUSS mask aligners. It is meant as a guideline especially for beginners in the field of pattern recognition, but even more experienced users might find one or the other aspect about pattern recognition which is new to him or her.



Almost all production steps in the manufacturing of semiconductor and MEMS devices need some sort of alignment of the new features to structures already placed on the substrate earlier. This is especially true for back end of line processes which are the main field of application of SUSS mask aligners.

Since according to Moore's law also backend processes are targeting ever smaller feature sizes the requirement on alignment accuracy saw a constant tightening in the last years. Nowadays, required alignment accuracies of 1 µm or even smaller are common, where it used to be several micrometers just a couple of years ago. While measurement of the pattern position with submicron accuracy in principle is not an issue for modern pattern recognition systems – they are capable to find positions of structures with accuracies far smaller than the pixel resolution of the image capturing system, down to several tens of nanometers – as often the devil is in the details. While alignment systems in the front end processing rely on fixed target geometries, in backend processing target variation is a lot bigger and the target quality often much worse. This can be caused by countless reasons, substrate surface condition and covering by insufficiently transmitting materials just being two examples.

The following overview will try to give some insight into the complexity of the task of creating reliable and accurate alignment pattern models under varying surface and surrounding conditions. It can be used as a quick guideline when starting alignment target training. However, for more complex challenges in target model training the reader is pointed to the extensive trainings offered by the SUSS training center and which are noted at the end of this article.

The first part of the series will cover general information about the pattern recognition system used in SUSS mask aligners and how changing the conditions of the grabbed image is influencing the pattern recognition process. The following parts will focus on rules and processes how to setup and optimize pattern in order to achieve good accuracy and reliability in the alignment process as well as on some application examples more detailed.

COGNEX PATMAX® VERSUS CNL

The alignment system in SUSS MicroTec mask aligners is based on the standard solution in the semiconductor market: the PatMax® geometric pattern recognition algorithm of Cognex.

In contrast to cross-correlation methods like CNL which directly compare the grey levels of the acquired images, the PatMax® system extracts geometrical infor-mation from the images to create edge models of the structures found in the image. Although grey values are also used for the identification of the edges inside of the image, geometrical pattern matching has several advantages over correlation matching.

1. Due to the restriction of the used information on geometrical data, the system is less sensitive to changes in brightness and contrast between the trained model and the actual scene presented to the system during a pattern search.

2. It is up to the user to decide which edges carry the position information and which edges are ignored.

3. Furthermore, flexible transformations of geometrical data, like scaling and rotation allow automatic or manual adaption to changing process conditions.

4. The model's edges are dis-played giving the user feedback on the model and the position and quality of its match with the targets.

THE MODEL OR PATTERN AND ITS MATCH WITH THE TARGET

Pattern matching algorithms operate with a target "model" or "pattern". The most common way to define target models is the model creation from a part of an image of the real world target. In case of PatMax®, the model is an "edge model", some matches of such a model with an image are shown in the title figure on page 10. The match in the center is supposed to deliver the highest score. Mismatches are represented with red lines indicating missing edges.

It is obvious, that especially during the target model training a high expertise has to be put into selecting well suited real world structures. A bad choice of the structure used for training e.g. a very small area will result in a trained target model which gives multiple and thus unreliable recognition results.

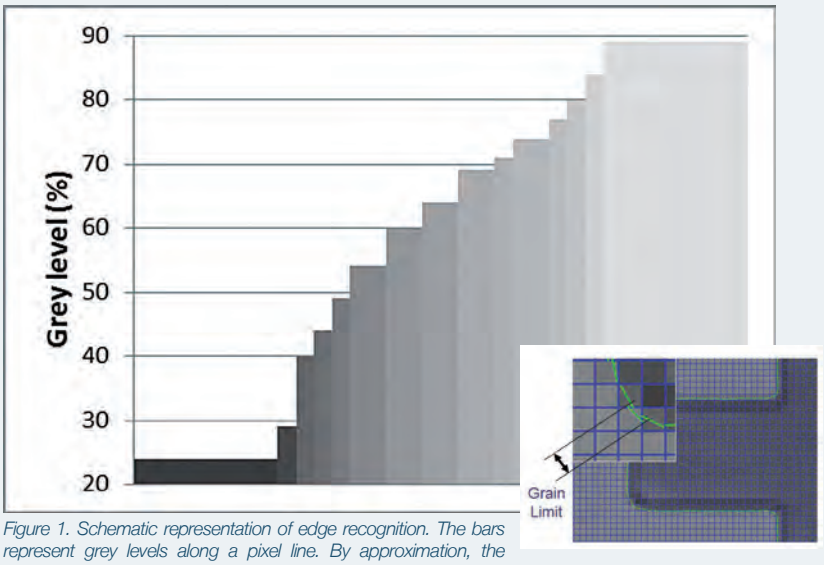


Figure 1. Schematic representation of edge recognition. The bars represent grey levels along a pixel line. By approximation, the discrete grey values are transferred into a continuous function. The position of the edge is found from a defined threshold level in the continuous data (here 50% of spanned grey range). Inlet: image of edges found in typcal mask aligner target

WHAT IS AN EDGE?

The extraction of geometries from the pixel images is performed by analyzing grey scale levels. If the grey level changes in a certain area surpass the limit "edge threshold" for the slope and "contrast threshold" for the height, then we have found an edge segment. For a schematic drawing see figure 1. The size of this vicinity is appointed by the grain limit control in the PatMax® software.

As the lateral position of the edge is determined from the approximated continuous data, it can be located with sub pixel accuracy. The direction of the edge segment is found using the grey levels of its neighborhood. This edge detection is performed on each scene during the actual pattern recognition, but also in case of pattern training from real world data.

Figure 2. Influence of illumination on target visibility. Microscopic images acquired with different illumination settings. a) undefined customer illumination, b) red LED, c) yellow filtered white LED (6000K), d) yellow filtered white light halogen (3200K)

SUB-PIXEL ACCURACY

In tests we proved a sub-pixel accuracy of below 1/40 pixel. That can be explained: A target which measures 50 µm yields 200 edge segments, whose positions and directions are averaged.

The advantage is that low power objectives can be used.

Example: A 5x objective and a camera may result in 1 µm/pixel magnification. But although the objective has only a 2 µm L/S resolution, the systems yields a 25 nm position resolution. Besides granting a large field of view low power objectives contribute to machine stability with their high depth of focus.

ILLUMINATION: KEY TO SUCCESS

The art in setting up reliable pattern recognition and therefore reliable alignment processes lies in balancing the need for flexibility to recognize varying targets with the need for uniqueness to reduce the amount of wrong findings.

The most important parameter to improve the reliability of pattern recognition is a proper definition of the illumination conditions. The illumination of the scene should fulfill a whole set of requirements:

1. It must be bright enough to keep any detector noise at a low level and to insure that even in the darkest areas real features are still discernible.

2. On the other hand the illumination should be low enough not to overexpose bright image areas and crossfade important details.

3. It must not create artifacts.

4. The contrast between edge and environment must be high enough to distinguish them from each other.

5. Avoid exposure of the photo resist.

That can be seen exemplarily on the SiO2-substrate in figure 2. Here, changing the illumination setup created anything from hardly discernible substrate structures over strong shadow artifacts and very weak contrasts to crispy images with very good structure representation. Parameters that can be varied for this adjustment in the SUSS mask aligners are the illumination method (reflected or transmitted light), light sources (halogen/LED), color filtering and collimation angles of the incident light (ring illumination).

It is easy enough to understand, that having sufficient contrast in the images to be analyzed by the pattern recognition is of crucial importance. This is especially true if the image is used as a template for creating the target model, as lower contrast always increases the risk to train features in the scene that are actually not part of the real target.

However, as the images in figure 2a) and 2b) demonstrate, illumination can also create virtual edges within the scene that can heavily interfere with the pattern recognition and consequently with the complete alignment process. Common reasons for such ghost edges or artifacts are reflections from the substrate surface interfering with geometries on the mask, which can be suppressed or at least greatly reduced by choosing larger imaging gaps. A second reason is the presence of interference artifacts within transparent layers on top of the structures on the substrate. Figure 2a) is a good example of the effect these interference artifacts can have on the observed images.

PROCESS VARIATIONS

The second serious influence on the reliability of the pattern recognition is, of course, the repeatability of the structures presented in the individual scenes. Due to process fluctuations, the target structures on the wafer can drastically vary from wafer to wafer. Figure 3 presents examples of structure variation between wafers

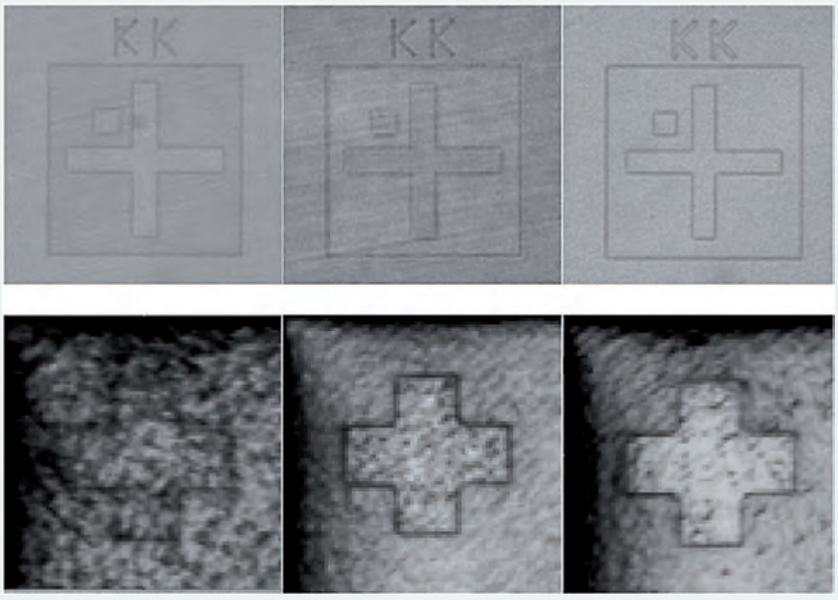


Figure 3. Two examples of screen shots of target variation in different scenes. Scrub marks (top row) and epilayers (bottom row) can introduce clutter and change contrast

caused by preceding process steps. The top row shows an example of back ground wafers. Here, due to the different degree of scrub marks, contrast and even polarity of the marks changes together with a varying level of clutter in the scenes. Also the bottom row, which shows targets on epilayers, presents a severe degree of variation. These variations are based on the varying reflectivity caused by the surface roughness. As can be seen in the image this even leads to reasonable changes in the identifiable edges.

As can be understood from these examples, the choice of suited scenes for the target training is of crucial importance. Selection of bad targets for the training (scenes with untypical information, bad contrast, untypical polarity and so on) will severely deteriorate the reliability of the pattern recognition process.

The next parts of the articles will therefore introduce guidelines on how to select good scenes for target training and procedures for testing and optimizing the trained target models.

Meanwhile, we would like to remind the reader of the extensive trainings that are offered by the SUSS MicroTec training department covering this subject. For information on trainings please be referred to the respective SUSS webpage: http://www.suss.com/en/customer-service/training.html and the contact information therein.

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EXTENDING THE RUTHENIUM CAPPING LAYER LIFE TIME OF EXTREME ULTRA-VIOLET LITHOGRAPHY PHOTOMASKS IN PHYSICAL FORCE CLEANING

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1. INTRODUCTION

Extreme Ultra-Violet Lithography (EUVL) is currently considered one of the most promising Next Generation Lithography (NGL) choices to extend shrinkage of transistor sizes. This is also reflected in the International Technology Roadmap for Semiconductors (ITRS).

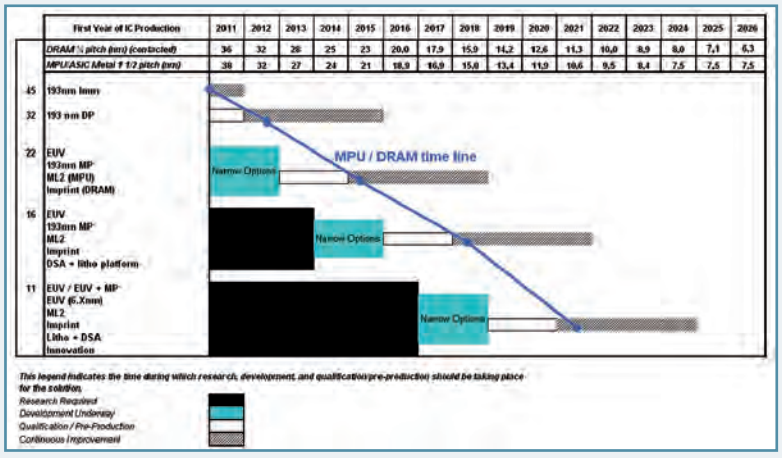


Figure 1. Lithography choices listed in the International Technology Roadmap for Semiconductors (ITRS, 2011)

EUVL works at an exposure wavelength of 13.5 nm, which is electromagnetic radiation absorbed at a high rate by nearly any solid material. Therefore, photomasks must be of reflective nature. This is accomplished by a Multi-layer structure deposited on top of a low-thermo expansion quartz substrate (LTEM substrate) (Figure 2).

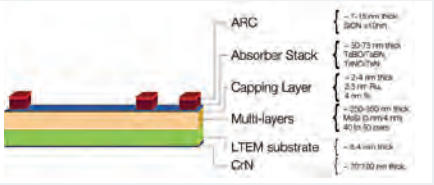


Figure 2. Structure of a EUVL Photomask (Source: SEMATECH)

Defect-free photomasks have always been a pre-requisite for high yields in Semiconductor device manufacturing. However, the fragile nature of the EUVL photomask multi-layer, is putting forward new requirements for photomask cleaning. SUSS MicroTec as the leading provider of advanced photomask cleaning equipment is addressing these new challenges systematically, collaborating with leading captive and merchant photomask manufactures, device manufacturers as well as Semiconductor Research Institutes.

The use of MegaSonic agitation is a widely used phenomenon for particle removal in photomask cleaning. For the advanced technology nodes the problem of damaged sub resolution assist features (SRAF) became highly prevalent in 193i optical masks. EUV masks do not have SRAF structures yet and the smaller feature aspect ratio and stronger material interface makes the pattern robust to withstand higher MegaSonic energy. However Ru capping layer pitting as a result of MegaSonic cavitation is making the use of acoustic cleaning questionable for EUVL reticles. Figure 3.a compares the number of added pits from a 1MHz MegaSonic system on different EUVL reticle layers and figure 3.b shows an SEM image of a typical pit generated by MegaSonic. Ru surface is more prone to

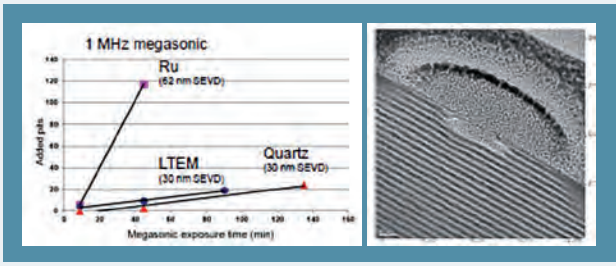


Figure 3. a) Plot showing Sematech's published data on a number of pits added on Ru, LTEM and Quartz substrates as a function of MegaSonic exposure time[2] b) SEM picture showing typical morphology of a Pit on an EUV mask surface[2]

a)

The Bubble Equation	$R\ddot{R}+\frac{3\dot{R}^2}{2}=\frac{1}{\rho}\left[\left(P_0+\frac{2\sigma}{R_0}-P_v\right)\left(\frac{R_0}{R}\right)^{\kappa}+P_v-\frac{2\sigma}{R}-\frac{4\mu\dot{R}}{R}-P_0-P_A\sin\omega t\right]$
Pressure Inside the Bubble	$P_i=P_0+\frac{2\sigma}{R_0}$
Cavitation Threshold	$P_v=P_0+\frac{8\sigma}{9}\left[\frac{3\sigma}{2\left(P_0+\frac{2\sigma}{R_0}\right)R_0^3}\right]^{\frac{1}{3}}$
Boundary Layer Thickness	$\delta_{ij}=0.16\left(\frac{\nu}{U_\infty x}\right)^{\frac{1}{7}}\cdot x$
Drag Force	$F_D=1.7009\,(3\pi\mu V d_p)$
Drag Moment	$M_D=0.9439934\,(2\pi\mu V d_p^2)$

b)

Property	Main Effect
Cavity Type (Vaporous or Gaseous)	• Cavitation Threshold
Gas Solubility	• Size of Cavity • Stability of Cavity
Gas Thermodynamic Properties	• Cp, Cv (Polytrophic index) • Size and Stability of Cavity
Media Thermodynamic Property	• Vaporous or Gaseous Bubbles
Media Viscosity	• Boundary Layer Thickness • Drag Force
Media Surface Tension	• Pressure Inside the Bubble • Cavitation Threshold

Table 1. a) The MegaSonic cavitation parameters and their dependence on media physical properties
b) The media properties and there effect on MegaSonic cavitation parameters [5, 14]

pitting as compared to LTEM and quartz[1, 2].

The acoustic energy transfer in MegaSonic systems can result into acoustic cavitation[3, 4]. Acoustic cavitation occurs due to the sinusoidal pressure variations that travel through the liquid along with the acoustic wave.

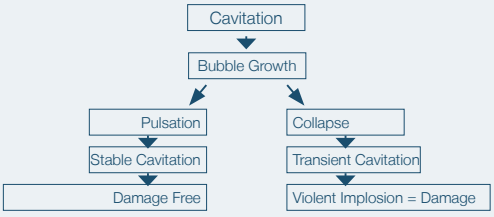


Figure 4. Schematic explaining the acoustic cavitation phenomenon created by MegaSonic energy in a liquid

During the low pressure component of the acoustic wave, small cavities form in the liquid which either compress or implode in the high pressure part of the propagating wave[5]. The presence of pulsating bubbles indicates stable cavitation. The implosion phenomenon is called transient cavitation (Figure 4).

Implosion of cavitating bubbles leads to localized high pressure and high temperature values which create shock waves in the liquid resulting not just in particle removal but also in feature damage and Ru pitting (Figure 5). In contrast, stable cavities can undergo large amplitude pulsations resulting into micro-streaming and such micro-streaming can lead to intense shear stresses along the boundary at the interface of cleaning media and photomask surface[6]. These shear stresses lead to drag forces and rolling moments on particles on the photomask surface which subsequently overcome the adhesion force between particle and surface[7]. Since there are no shock waves generated, the chances for Ru pitting reduce significantly (Figure 5). It is obvious that stable cavitation can resolve the issue of Ru pitting or pattern damage. The cavitation bubble behavior is dependent on physical properties of the cleaning media. Table 1.a shows different equations on multiple cavitation parameters and each of these equations constitute physical property parameters of the liquid media. Table 1.b lists the effect of different media properties on cavitation behavior. Therefore it would be logical to conclude that media and gas physical properties are the main variables that define cavitation behavior and subsequent cleaning effect. If an appropriate cleaning media with optimized physical properties is chosen, it is feasible to generate predominantly stable cavitation.

Earlier SUSS MicroTec Photomask Equipment (former HamaTech APE) has published extensive research on the MegaSonic phenomenon where SRAF damage free cleaning is demonstrated[8-13]. In this study we applied the MegaSonic knowledge gained while solving SRAF damage issue

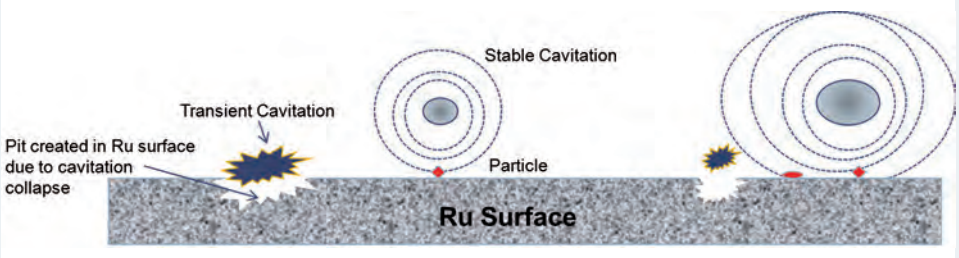


Figure 5. Schematic depicting the Ru pitting phenomenon as a result of transient cavitation events.

in 193i mask cleaning, to resolve the Ru pitting issue on the EUV mask cleaning. The gasses or vapours filled in the cavitation bubbles define the bubble wall movement or the pulsation of the bubble under propagating acoustic wave. This bubble wall movement defines the nature of the cavity, i.e. whether it would stay a stable pulsating bubble or whether it will collapse under acoustic pressure variations. The gas or vapour inside the bubble constitutes gaseous or vaporous state of the cleaning chemistry used during cleaning. Therefore it is important to analyse the effect of cleaning chemistry on pattern damage and Ru pitting. We correlate the effect of liquid cleaning media on SRAF feature damage and Ru pitting.

2. EXPERIMENTAL

2.1 PROCESS PARAMETERS

All the pattern damage and Ru pitting tests were performed using the SMT PE MaskTrackPro (MTPro) mask cleaning tool. The process parameters were automatically monitored and controlled with a standard recipe programmed on the MTPro tool. DI water used for the tests was de-gassed before it was supplied to the cleaning chemical distribution system. Chemicals (NH_4OH or H_2O_2) and gases (CO_2 or H_2) were added into the de-gassed water to prepare the respective cleaning media. The cleaning media tested are: SC1 (NH_4OH + H_2O_2+ DI), NH_4OH + H_2O, H_2O_2 + H_2O, H_2 + H_2O, and a new cleaning Chemical A. These cleaning media are tested at different MegaSonic power values.

2.2 CHARACTERIZATION

Pattern damage induced by different MegaSonic cleaning process conditions was analyzed using a pattern mask inspection tool. Ru pitting was analysed using high sensitivity blank inspection tool. PRE was tested on deposited SiN particles on blank substrates. Absorber CD is measured on an EUV patterned mask using a CD-SEM tool and an actinic EUV-reflectometer is used for EUV-R measurements.

2.3 MATERIALS & METHODS

Ru pitting was tested on Ru-multilayer blanks. Pattern damage was tested using optical Phase Shift Masks (PSM) with Sub Resolution Assist Feature (SRAF) size suited for advanced technology nodes. For this evaluation, an advanced mechanical feature of the MTPro was utilized, Focused Spot Cleaning (FSC)[15]. FSC allowed more than 20 different settings to be tested with only one test mask & Ru blank and a single inspection.

3. RESULTS & DISCUSSION

3.1 COMPARISON BETWEEN SC1 (NH_4OH + H_2O_2 + DI) & H_2-DI

Figures 6a & b compare the effect of SC1 and H_2-DI chemistries on pattern damage on 193i masks and Ru pitting on Ru blanks. It has been well known that H_2-DI if used at proper gas concentration shows lesser pattern damage than the SC1. NH_4OH has a very low boiling point (24.7°C, at 32%). Under acoustic conditions NH_4OH decomposes readily into NH_3 gas. H_2 gas has favourable cavitation properties as compared to NH_3 gas that fill the cavitation bubbles under MegaSonic. Moreover H_2 is intentionally dissolved into DI to create hydrogenated water, its bubbles provide cushioning effect for the acoustic energy transfer therefore pattern damage is reduced. A similar effect is observed on the Ru pitting. H_2-DI MegaSonic creates lesser pits on the Ru as compared to SC1.

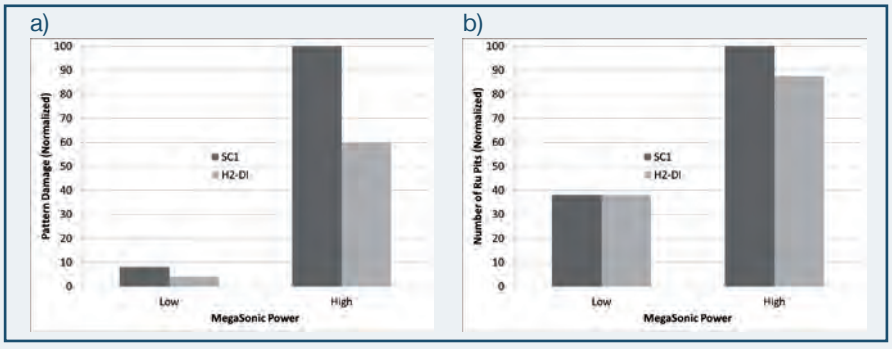
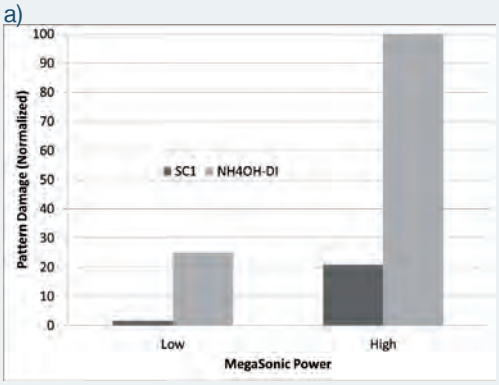


Figure 6. Comparison of cavitation and chemistry related effect of SC1 and H2-DI on a) pattern damage b) number of Ru pits.

a)



b)

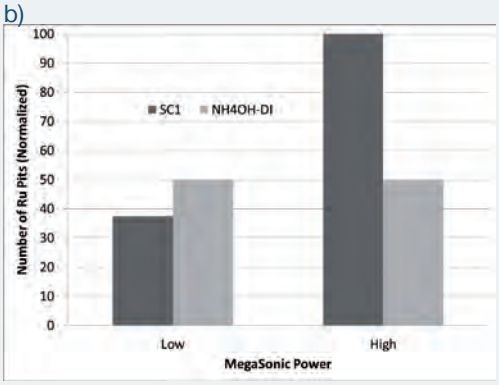


Figure 7. Comparison of cavitation and chemistry related effect of SC1 and NH4OH-DI on a) pattern damage b) number of Ru pits.

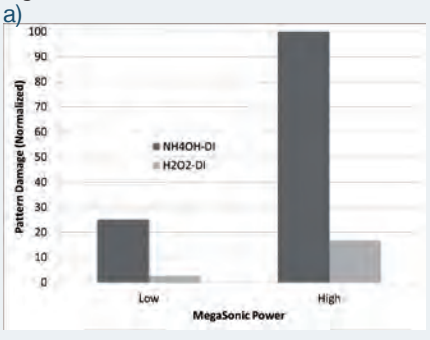
3.2 COMPARISON BETWEEN SC1 (NH_4OH + H_2O_2 + DI) & NH_4OH-DI

NH_4OH-DI shows much higher pattern damage than SC1 at both higher and lower MegaSonic power (Figure 7.a). However the number of pits produced from SC1 is higher than NH_4OH-DI at higher power (Figure 7.b). This discrepancy can be explained based on the physio-chemical phenomenon. SC1 is a mixture of NH_4OH-DI and H_2O_2 into DI-water. H_2O_2 is extremely oxidizing chemical and Ru surface is very prone to oxidation. H_2O_2 can react with Ru to form highly volatile Ru oxides (e.g. RuO_4). Therefore in case of MegaSonic SC1 treatment the cavitation damage is further enhanced by chemical reaction between H_2O_2 and Ru. At higher MegaSonic power the aggressiveness of the chemical attack increases because of stronger acoustic effects (localized pressure and temperature rise). This is why although the pattern damage is higher with ammonia; the number of pits added is higher with SC1. The pattern damage with SC1 is lower because some of the H_2O_2 can decompose into O_2 and O_2 in the cavitation bubbles has more favourable properties than the NH_3 gas. Decomposition of H_2O_2 ($2H_2O_2 \rightarrow 2H_2O + O2$) is thermodynamically favourable with a $\Delta H°$ of $-98.2\ kJ*mol^{-1}$ and a ΔS of $70.5\ J*mol^{-1}*K^{-1}$. High acoustic pressure and temperatures generated locally under the MegaSonic pressure waves may initiate such decomposition reaction.

3.3 COMPARISON BETWEEN NH_4OH - DI & H_2O_2-DI

To further verify the claims in section 3.2 above the pattern damage and Ru pitting comparison was made between the two main constituents of SC1, i.e. NH_4OH - DI & H_2O_2-DI (Figure 8.a & b). H_2O_2-DI alone has significantly lesser pattern damage than NH_4OH-DI alone. However as expected based on the discussion above the pitting was more severe with H_2O_2-DI at higher MegaSonic power. This confirms that H_2O_2's chemical reaction with Ru and significantly different cavitation properties of O_2 and NH_3 gas defines the pattern damage and Ru pitting behaviour. This also suggests that the process conditions that show lesser pattern damage do not necessarily produce lesser pitting on Ru surface. Physio-chemical effects of cleaning media used with MegaSonic have to be taken into account for effective process development.

a)



b)

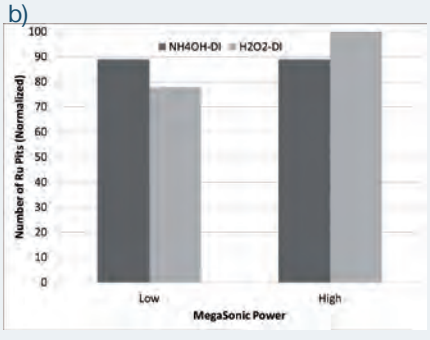


Figure 8. Comparison of the cavitation and chemistry related effect of NH_4OH-DI & H_2O_2-DI on a) pattern damage b) number of Ru pits

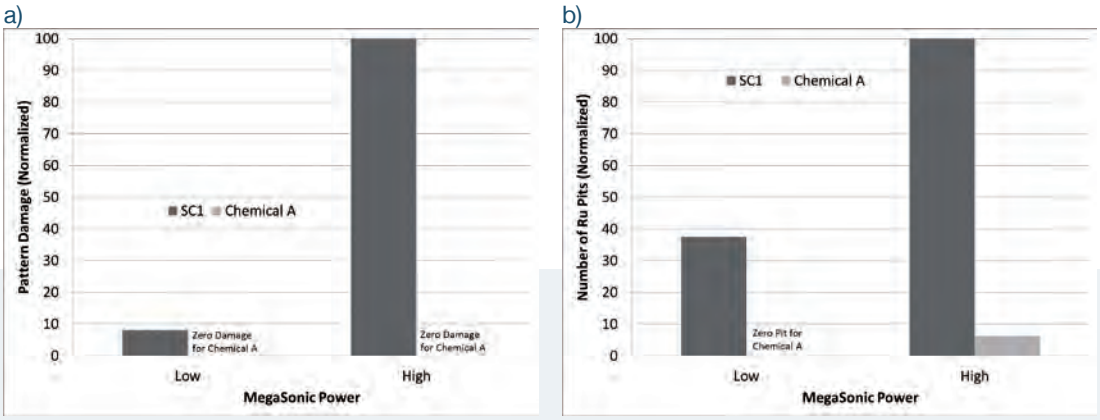


Figure 9. Comparison of the cavitation and chemistry related effect of SC1 and chemical A on a) pattern damage b) number of Ru pits.

3.4 COMPARISON OF SC1 ($NH_4OH + H_2O_2 + DI$) & NEW MEDIA (CHEMICAL A)

As discussed earlier in section 3.1 to 3.4, the chemical nature of the cleaning media defines the cavitation behaviour in MegaSonic and physio-chemical behaviour in Ru pitting. Considering this, we have developed a new chemistry "chemical A" which has highly favourable cavitation behaviour and negligible chemical side-effects. Figure 9.a & b compares the effects of SC1 and Chemical A on pattern damage and Ru pitting.

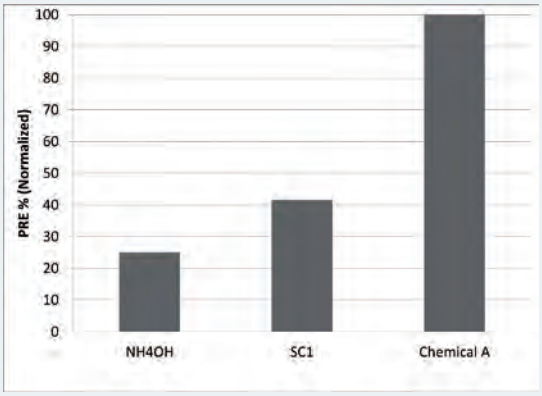


Figure 10. Particle Removal Efficiency (PRE) comparison between NH_4OH-DI, SC1 and Chemical A based Process of Record (POR).

Chemical A showed no pattern damage on any power level tested. Chemical A produced zero pits at lower MegaSonic power. At higher MegaSonic power, relatively insignificant number of pits is seen.

Since these tests were intentionally done at accelerated conditions, the MegaSonic process conditions were optimized further for zero Ru pit conditions using chemical A as part of the POR for mask cleaning.

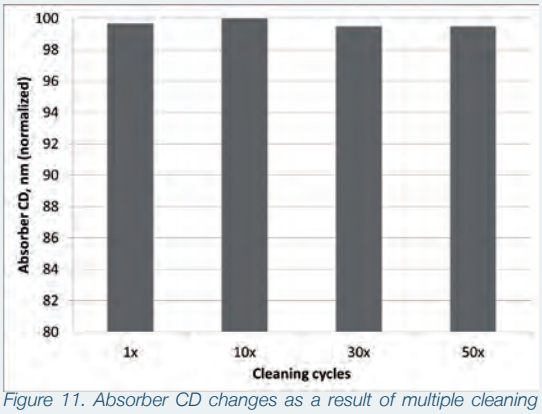


Figure 11. Absorber CD changes as a result of multiple cleaning cycles of Chemical A based Process of Record (POR).

3.5 PRE COMPARISON OF SC1 ($NH_4OH + H_2O_2 + DI$) & NEW MEDIA (CHEMICAL A) USING COMBINATION NOZZLE

A complete Process of Record (POR) based on Chemical A was developed for the cleaning of EUVL reticles. The Particle Removal Efficiency (PRE) was compared between POR's based on NH_4OH-DI, SC1 & Chemical A (Figure 10). The PRE was tested while implementing combination nozzle (new hardware feature from SUSS MicroTec Photomask Equipment). In this new feature the reticle substrate is exposed to MegaSonic beam rinse and droplet spray simultaneously. While acoustic energy from MegaSonic beam dislodges particles from deep trenches, spray droplets provide additional lateral forces through jetting. Chemical A based POR was identified to achieve ~60% higher PRE as compared to SC1 based POR. The PRE for SC1 based POR is ~15% higher than NH_4OH-DI based process. Chemical A based POR shows no pattern damage and zero Ru pitting and has the maximum particle removal efficiency (PRE).

3.6 ABSORBER CD SHIFT

Figure 11 shows the effect of multiple cleaning cycles on absorber CD (Critical Dimension) changes using Chemical A based POR. The normalized CD is compared and plotted after 1x, 10x, 30x and 50x cleaning cycles. A CD increase of 0.35 nm (.035 nm/clean) was observed after first 10x cycles. However for subsequent cleaning cycles the CD was again stabilized to the original values. The random CD increase after first 10x cleaning can be attributed to CD-SEM's tool measurement artifact[16].

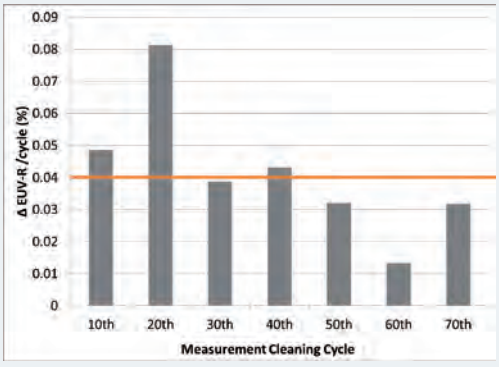


Figure 12. Plot showing effect of number of cleaning cycles on Ru-multilayer EUV- reflectivity

3.7 RU EUV-REFLECTIVITY

Since it is expected that an EUV reticle will be cleaned approximately 100 times in its lifetime, we tested Ru capping layer durability with chemical A based POR over 70x cleaning cycles. Figure 12 shows the effect of cleaning cycles on absolute EUV-reflectivity plotted every 10x consecutive cleaning cycles. The total change in absolute EUV-R after 70x cycles was found to be only 0.04% per clean (averaged over 70x cleans). An EUV-R increase was observed.

4. CONCLUSIONS

The process conditions that create pattern damage on 193i reticles do not necessarily create Ru pits on the EUVL reticles. Physio-chemical effects of cleaning media used with MegaSonic have to be taken into account for effective process development. The chemical nature of the cleaning media defines the cavitation behaviour in MegaSonic and physio-chemical behaviour in Ru pitting. Chemical A based POR shows no pattern damage and zero Ru pitting as compared to SC1 and NH_4OH-DI and has the maximum particle removal efficiency. This new process did not show any absorber CD shift over 50x clean and only showed an EUV-R change of 0.04% per cleaning cycle averaged over 70x cleans.

THE AUTHORS

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Uwe Dietze has been with SUSS MicroTec Photomask Equipment (formerly HamaTech APE) since 1990 in various functions of customer service, sales and management. He is holding a Bachelor of Science Degree in Mechanical Engineering and has gained 32 years of experience in photomask and semiconductor technology. As Senior Director Surface Technology Innovations he is today responsible for the development of advanced features and technologies for SUSS wafer and photomask processing equipment.

Dr. Peter Dress is with SUSS MicroTec Photomask Equipment (former HamaTech APE) since 1998 based in Sternenfels, Germany. During his career at SUSS MicroTec he is holding various positions in process technology and equipment development. As Director Advanced Process Development he is now responsible for the worldwide process technology development addressing photomask and wafer coat, bake, develop, wet-etch, and clean technology. He studied Physics at Duisburg University, earning a diploma in 1993 and his PhD in 1998. In parallel he studied business administration at the University Hagen finished with a Pre-diploma in 1997. While doing his PhD studies he worked as Software Engineer at NeuroTech GmbH, a company in the printing industry.

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3D TOPOGRAPHY MASK ALIGNER LITHOGRAPHY SIMULATION

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Ralph Zoberbier, SUSS MicroTec Lithography GmbH, 84748 Garching, Germany
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1. INTRODUCTION

In contrast to IC manufacturing where layers are thin and substrates are planar, MEMS, IC packaging, 3D IC, interposer and display application exhibit a strong 3D topography, typically requiring thick resists to cover the topography. Major lithography challenges of 3D topography are:

- Variation of effective distance of mask (proximity gap) and substrate surface
- Resist thickness variations
- Reflectivity and absorption variation of layer below resist
- Complex reflection and diffraction effects on tapered, shadowing on steep sidewalls

Experimental verification and optimization of design (mask layout) and exposure conditions is very time consuming and expensive as it cannot be done on planar test wafers.

Lithography simulation is an excellent technique for analyzing and optimizing complex scenarios without the need of experiments, and is a standard for high resolution IC manufacturing using projection lithography[1]. For proximity lithography GenISys introduced the LAB[2] simulation software few years ago. Recently, SUSS MicroTec and GenISys enabled "source-mask-optimization" (SMO) for mask aligner, including illumination shaping provided by the new SUSS MO Exposure Optics, and the mask layout[3, 4, 5].

However, calculating the light propagation in a 3D topography is a big challenge. Rigorous methods which have been developed for IC manufacturing fail for MEMS, packaging or display applications because the larger areas to be simulated would lead to excessive data volumes and calculation times. This paper is presenting a 3D topography simulation dedicated for proximity lithography for high-topography, thick resists and larger areas in reasonable calculation time.

2. MASK ALIGNER LITHOGRAPHY SIMULATION

2.1 PLANAR STACKS

Mask aligner lithography simulation for planar cases starts by calculating the so called "aerial image" (the intensities in air at a given distance below the mask) using a fast algorithm based on Kirchhoff scalar diffraction theory. The model takes into account a broad band light source (e.g. spectrum of mercury lamp), and the source

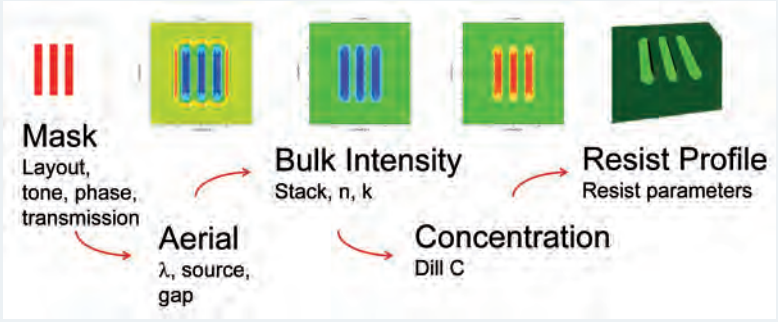

Figure 1. Essential steps in mask aligner lithography simulation; 80% of the lithographic effects are already contained in the aerial and bulk images

shape (e.g. circular with collimation angle, or an arbitrary source shape). This “aerial image” is then propagated into the resist, taking into account all back-reflections from substrate and coatings. LAB simulation software is also able to model resist “bleaching” (change of absorption coefficient during exposure). The well-established Dill Model computes photoactive-compounds concentration (PAC) from the light intensities, and the development process is modeled using empirical models such as MACK4.

2.2 3D SIMULATION PRINCIPLES

Simulation of mask aligner lithography coupled with wafer topography is a challenging task for several reasons. First, the simulation window is typically large (about laterally 100 µm x 100 µm simulation area, vertically 10 µm resist thickness and topography). Second, modeling of broad-band illumination requires repeating the simulation for all wavelengths individually. Third, several different angles of incidence must be taken into account for extended light sources. Last but not least, light propagation in a non-planar stack has to be computed. The usage of established electromagnetic modeling methods such as FDTD (Finite Difference Time Domain) or RCWA (rigorous coupled wave analysis) in case of large volumes is prohibitive because of their high computation cost and memory consumption.

To address the challenges mentioned above, we developed a fast approximate method that exhibits excellent time and memory scaling properties (Table 1). In our method, the simulation domain is divided into homogeneous convex regions. Inside each region, propagation from interface to interface is computed in a single step. Then, transmission and reflection is calculated (Figure 2). The entire procedure is repeated for each interface several times until convergence is reached.

Method	Time Scaling	Memory Scaling
RCWA	$N^6 \times Z$	N^4
FDTD	N^4	N^3
Our Method	N^3	N^2

Table 1. Comparison of different electromagnetic modeling techniques with respect to time and memory consumption. N denotes the number of unknowns along one dimension, Z is the accuracy of vertical discretization.

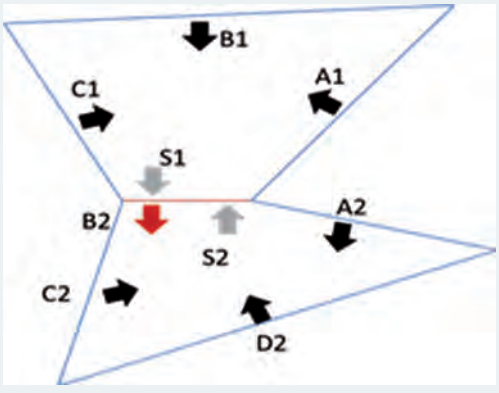

Figure 2. Iterative computation of propagation and transmission/ reflection. For a given interface (here exemplarily B2), first the fields at the neighboring interfaces are propagated to the selected interface and are summed up (S1 and S2). Then, field B2 is computed as the transmitted part of S1 + the reflected part of S2.

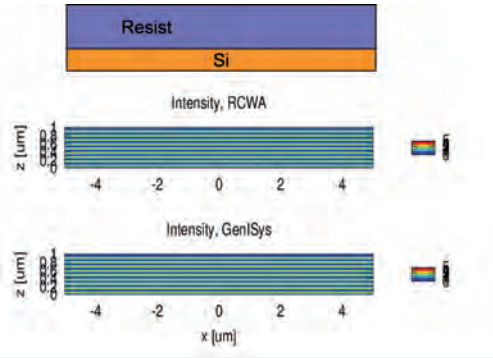

Figure 3. Comparison of TMM and 3D on a planar stack

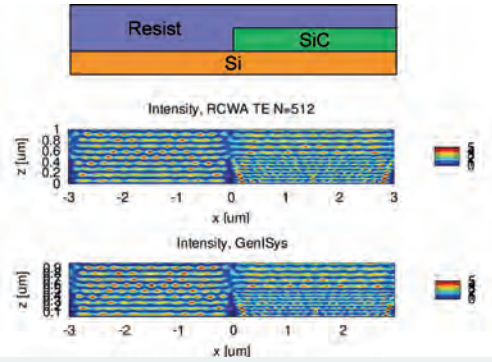

Figure 4. Comparison of RCWA reference and 3D algorithm on a vertical step

2.3 VALIDATION

The method has been validated by comparing the result of the 3D computation to well-known solutions. For planar stacks, the new method results in the same intensity distributions as the well-established TMM algorithm (Figure 2). To test topographic scenarios, the new algorithm was benchmarked on an existing RCWA implementation (Figure 3).

3. INDUSTRY EXAMPLE

The study was done on a 2 micron step in the stack. Would that lead to visible lithographic artifacts?

The method, applied to a real case scenario shows a good agreement to the visible artifacts. Fortunately, the structure turned out to be printable as is – no further optimization was required.

Figure 5. The stack exhibits several "steps", the most pronounced being a 2 micron step; the entire stack is buried under 5.5µ resist; exposure conditions are: broadband illumination, 70µ proximity gap

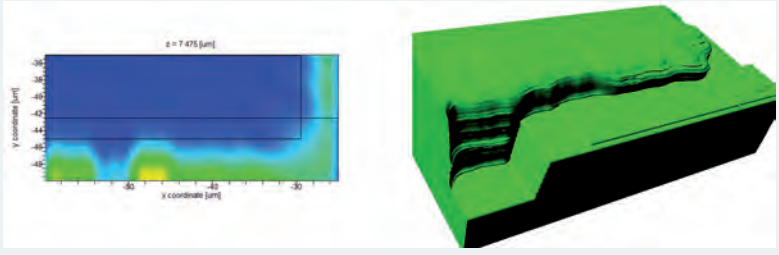

Figure 6. Simulation, XY-View at resist top (left) and resist image (right)

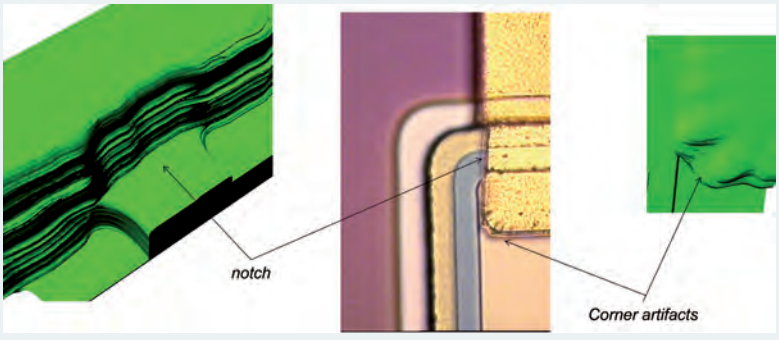

Figure 7. Comparison of resist Image to experimental result (Al layer already etched, resist is still present); the notch is clearly visible, as well as the corner artifacts at the 70µ proximity gap

4. SUMMARY

Lithography simulation enables the ability to transfer the benefits of mask aligners beyond the classical limits by resolution enhancement techniques such as layout optimization (OPC), source shaping, advanced mask technologies (grey-tone, phase shift), or combinations thereof such as source-mask-optimization. The combination with the SUSS MO Exposure Optics opens new opportunities for next generation products for 3D packaging, flat panel display and MEMS products, particularly through the integration of the 3D topography simulation that is capable of computing larger areas, thick layers, and high-topography in reasonable time using off-the-shelf PCs.

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THE AUTHORS

Ulrich Hofmann holds a physics degree (Diplom) from the Technical University in Munich and has more than 20 years experience in the semiconductor industry, working in various technical and management positions on E-beam technologies as well as optical lithography technologies. Ulrich pioneered technologies such as real-time proximity effect correction, hierarchical data processing, and ultra-high bandwidth datapath for massive parallel E-Beam direct write, and drove the development and factory integration of a next generation mask lithography tool. In 2005, he founded GenISys GmbH, a software house providing solutions for the optimization of microstructure fabrication processes for R&D, semiconductor manufacturers and equipment suppliers throughout the world.

Nezih Unal received his Diploma in Electronics Engineering at the University Wuppertal, with a focus area on semiconductor technology. He has started working on the development of Reactive Ion Etching (RIE) processes for IC manufacturing at Motorola in 1988. In 1992 he joined microParts GmbH to develop and manufacture 3D MEMS devices using X-ray lithography. Nezih joined SIGMA-C GmbH as Director of Sales in 2003, and positioned the optical lithography simulation software SOLID in the market. As Vice President Marketing & Sales at GenISys GmbH, Nezih Unal is one of the company's key figures in creating unique solutions that make a difference.

Ralph Zoberbier graduated in Precision Engineering and Microsystems Technology from the University of Applied Sciences in Nuremberg. He joined SUSS MicroTec in 2001 as R&D Project Manager and became International Product Management Aligner in 2005.
Since 2010 he leads the Aligner Product Management team as Director Product Management. With the recent acquisition of Tamarack Scientific Inc. his area of expertise was extended by complementary projection lithography and laser process technology. In 2006 Ralph gained a MBA degree in Entrepreneurship at Louisville University, Kentucky

Ton Nellissen holds a Masters degree in Chemistry from the Utrecht University, The Netherlands. In 1982 he joined Philips, where he worked on semiconductor process development, and became responsible for the development and implementation of colour filters for CCD image sensors. Other activities were in the field of semiconductor packaging where he developed special photolithographic techniques based on inclined illumination and diffractive optics to realize out of plane conductor tracks. Further he was strongly involved in the development of a mask-less imaging technique for pattern-wise UV exposure on photoresist coated substrates. Ton Nellissen is currently active as project leader and senior scientist in the field of process development for MEMS devices. He has authored several papers on micro electronics and packaging and holds also several patents in this field.

ALIGNMENT ACCURACY IN A MA/BA8 GEN3 USING SUBSTRATE CONFORMAL IMPRINT LITHOGRAPHY (SCIL)

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Substrate Conformal Imprint Lithography (SCIL) originally invented by Philips Research is an innovative nanoimprint technology. With this technology substrates up to 200 mm can be patterned with features down to a few nanometer resolution, delivering a unique uniformity of the imprint and the residual layer. The SCIL process was implemented as an option in a standard SUSS Mask Aligner in 2009 and is available on MA/BA6, MA/BA6 Gen3 and MA/BA8 Gen3 (Figure 1).

Figure 1. SUSS MA/BA8 Gen3 with SCIL toolset

Figure 2. SCIL stamp holder

The SCIL technology uses a three layer stamp for structure transfer (see Figure 3 and Figure 4). This stamp is composed of a thin glass back plate (~200 µm), a soft PDMS buffer layer (~500 µm) and a high modulus PDMS layer (100 µm) with the structures to be transferred. With this setup of the stamp absolute distortions like magnification errors but also the relative distortions due to elastic deformation during the imprint are minimized. Furthermore distortions of the structures during the imprint process are avoided by using only a small imprint pressure (20 mbar) and mainly capillary forces to pull the stamp into the resist layer.

SCIL can be of interest to many applications like LED, Lasers, Solar, Optics and MEMS. In some of them an alignment of the stamp to the

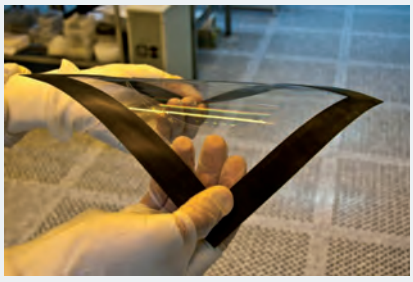

Figure 3. Flexible SCIL working stamp

substrate prior to the imprint is required. Due to the composite SCIL stamp, the overlay alignment capabilities should mainly be limited by the mechanical capabilities of the Mask Aligner.

To investigate SCIL performance on SUSS Mask Aligner platform a three months visit of Robert Fader (Fraunhofer IISB) at Philips Research / Philips Innovation Services in Eindhoven was financed by the Fraunhofer IISB. This stay was supported by Philips Research and SUSS MicroTec. Philips Research provided its facilities and Philips Innovation Services the cleanroom for the corresponding experiments. Goal of the investigations during the stay was to determine the overlay accuracy of SCIL at the SUSS Mask Aligner and to measure process induced distortions of the SCIL stamp over large distances.

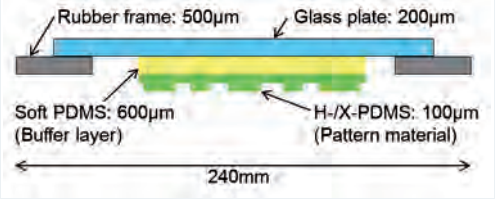

Figure 4. Schematic cross section of a SCIL stamp

For the analysis of the overlay alignment accuracy a master with common box in box fiducials (Figure 5) has been used to replicate a stamp and imprint wafers of 4" and 6" size. In a first step the alignment marks were imprinted into an epoxy resist layer on a silicon wafer and afterwards transferred into the silicon wafer by dry etching using the structured resist as

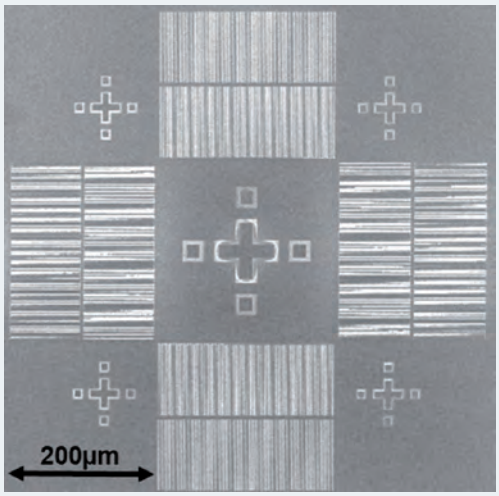

Figure 5. Box in box fiducials

etching mask. Subsequently, this wafer was again coated with the resist and a second aligned imprint was performed (Figure 6). Because the used master structure included

Figure 6. Aligned second imprint on transferred marks.

big and corresponding small box in box fiducials, the small fiducials could be aligned to the big ones using the same stamp (Figure 6). The stamp had just to be shifted. The alignment error could be determined by measurement of the relative position of the features imprinted in the second step with respect to etched marks (Figure 7).

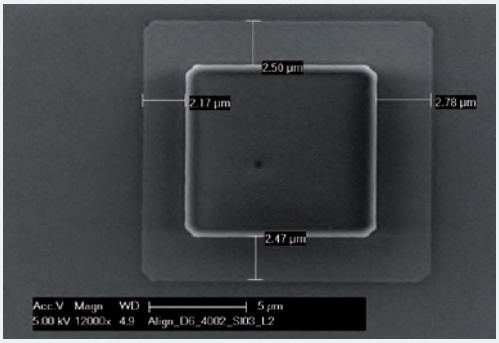

Figure 7. Relative position determination with SEM

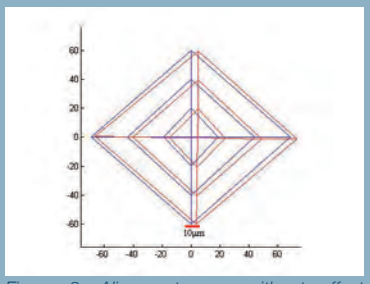

Figure 8. Alignment error without offset correction, X and Y axis show units in mm, alignment errors are magnified with a factor of 1000

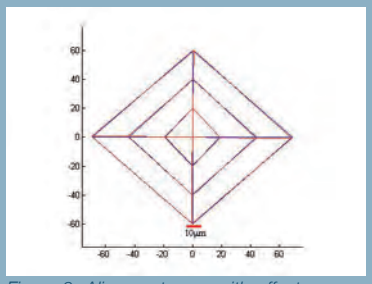

Figure 9. Alignment error with offset correction, X and Y axis show units in mm, alignment errors are magnified with a factor of 1000

The alignment in the Mask Aligner is performed with standard 10x magnification objectives. The imprinted wafers were measured in a SEM. All results showed that there is a reproducible offset mainly in imprint direction (Figure 8) which was adjusted by an offset correction in the Mask Aligner software (Figure 9). The offset is induced by the movement of the stamp from the SCIL actuator towards the resist coated substrate and, therefore, also dependent on the process gap. The results after offset correction showed that the overlay accuracy was within the specified mask aligner accuracy in all cases (<1 µm).

In order to characterize distortions of imprinted structures and deviations of specific distances (Figure 10) in the imprinted patterns compared to the original GDS-design (which was used for the master design) several imprints were performed with two different stamps. These measurements were done to investigate, if the SCIL process creates systematic distortions due to the bending of the stamp towards the substrate during the imprint process. Furthermore the measurements can be used to check reproducibility of the stamp replication process. Therefore, two separate SCIL stamps were prepared and with each stamp a number of imprints were performed. On each imprinted wafer a matrix with 15 different distances up to 40 mm has been defined (Figure 10) and these were measured in a SEM. These measurements with the two stamps were compared to each other and to the GDS pattern design, which was used to build the Si master wafer as a basis for replicating the stamps.
First the SEM stage accuracy was determined by repeatedly measuring distances on an imprinted wafer. These measurements showed that the stage accuracy was 200 nm in X-direction and 250 nm in Y-direction.

	S7		S11		S13	
	Distance in µm:	Standard deviation in µm:	Distance in µm:	Standard deviation in µm:	Distance in µm:	Standard deviation in µm:
GDS-File	27586.2	-	40000	-	31000	-
Stamp 1	27587.2	0.2	39999.4	0.4	31000.2	0.5
Stamp 2	27587.0	0.5	39999.2	0.2	31000.6	0.5

Table 1. Average results of three measured distances

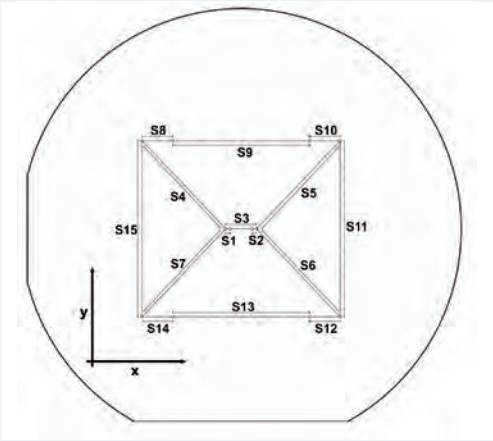

Figure 10. Measured distances on a 100mm wafer

The measured distances on the imprinted wafer for the two stamps vary in a range of a few hundred nanometers (400 nm maximal) which is within the measurement error (Table 1). This error results from the accuracy of the stage in the used SEM. The difference between the distances in the GDS file and the distances on the imprinted wafers are the same for the two stamps (Table 1). Therefore, this difference is constant for different stamps and a result of accumulated, mostly thermally induced, errors.

In summary all results of the performed experiments approved the assumption that the SCIL process itself does not induce any relevant distortion of the SCIL stamp. More than this it does not apply a misalignment that is above the standard specifications of a Mask Aligner.

THE AUTHORS

Robert Fader studied physics at the Friedrich-Alexander-University in Erlangen. After graduating in 2010, he continued doctoral research at the Fraunhofer Institute for Integrated Systems and Device Technology IISB in Erlangen in electrical engineering. Subject of his doctoral thesis is Substrate Conformal Imprint Lithography.

Ulrike Schoembs has been responsible for product management of the manual mask aligners at SUSS MicroTec since 2009. Having set off a practical career in mechanical engineering Ulrike joined SUSS MicroTec in 2003 and started off in various positions in Applications and Product Engineering. 2006 she has received an academic degree in precision and micro engineering. Since 2006 she is also holding a teaching position in microsystems engineering at the University of Applied Sciences Munich.

Marc Verschuuren started working at Philips Research in 2001 after he finished his bachelor in chemical engineering. Marc currently holds a position as senior scientist and project leader. Past work at Philips Research focused on material science in combination with electrical and optical device fabrication and characterization. Main topics include sol-gel chemistry, metal and semiconductor nano particles and surface chemistry. The common factor in this work was using soft-nanoimprint technology to pattern a variety of materials. Diverse projects within Philips research include the development of this technique, which led to the licensing of SCIL to Suss MicroTec in 2008. In 2010 he obtained his PhD on the subject of: Substrate Conformal Imprint Lithography for nanophotonics.

CMOS COMPATIBLE HERMETIC WAFER LEVEL PACKAGING FOR INERTIAL MEMS

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INTRODUCTION

Recently, there has been an increased demand for MEMS devices where the MEMS structure is integrated with CMOS circuitry at wafer level. Such devices could be fabricated in a conventional foundry using CMOS compatible materials in the manufacturing process. Currently, wafer level packaging of inertial MEMS devices either involves traditional glass frit or metal systems involving gold eutectic which is expensive and not compatible with CMOS front-end processing. The use of Al as a bonding metal is compatible with CMOS integration since Al is already used as a bond pad metal and has no contamination concerns in a standard CMOS clean room environment. Al-Ge based eutectic wafer bonding has been shown to provide a practical solution for MEMS-CMOS integration and hermetic wafer level packaging due to both Al and Ge being CMOS fab friendly, electrically conductive and orders of magnitude less permeable than glass.

This applications note describes a practical Al-Ge bonding process where Al is used as a seal ring metal on the MEMS device wafers while Ge is used as a cap wafer material. The Aluminum-Germanium system[2, 3] is a simple eutectic system with three phases (a) liquid (b) fcc (Al) solid solution and (c) diamond cubic (Ge) solid solution as shown in Figure 1. The eutectic point of this system has not been reliably reported but most published data points at a eutectic point of 420 °C ± 4 °C placing the atomic percentage of Ge at 28.4 % to 30 %.

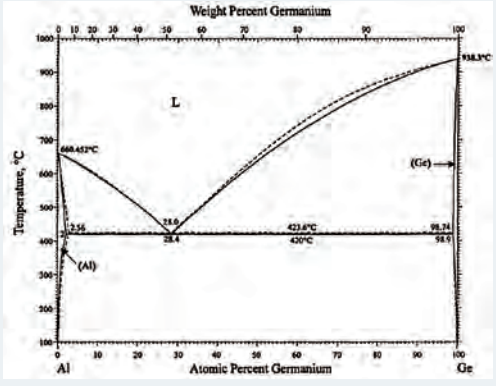

Figure 1. Phase diagram for Aluminum- Germanium system showing a simple eutectic system with three phases (a) liquid (b) fcc (Al) solid solution and (c) diamond cubic (Ge) solid solution with eutectic point of 420°C ± 4°C (J Phase Equil. 19(1), 1998)

For Al-Ge bonding, the thickness of the stack as well as the seal ring geometries should be designed while taking into account the expected atomic percentage of Ge at the interface. In addition for this process, care needs to be taken to ensure that the Al and Ge surfaces are free of native oxides and organic contamination from previous DRIE and lithography steps. One of the common methods to clean Ge deposited substrates is to dip the wafers in a dilute HF BOE solution. In addition, forming gas (3-5 % H_2) is used as an overpressure gas to avoid oxide growth inside the bonder prior to substrates coming in contact.

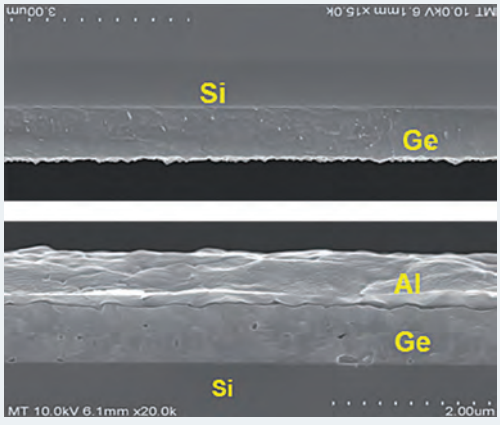

Figure 2. SEM cross-sections of pre-bonded wafers (a) Substrate 1: Si/0.1µm TEOS/0.5µm Ge (b) Substrate 2: Si/0.1µm TEOS/0.5µm Ge /1.5µm Al

PROCESS SETUP

This study used 200 mm single side

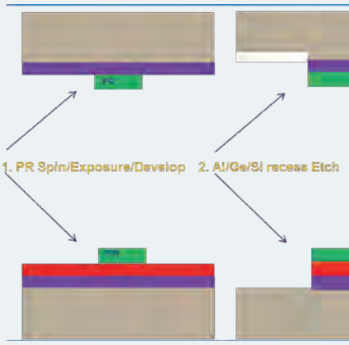

Figure 3. CB200 Process curve showing Al-Ge temperature are plotted on Left axis while cham the right axis (log scale).

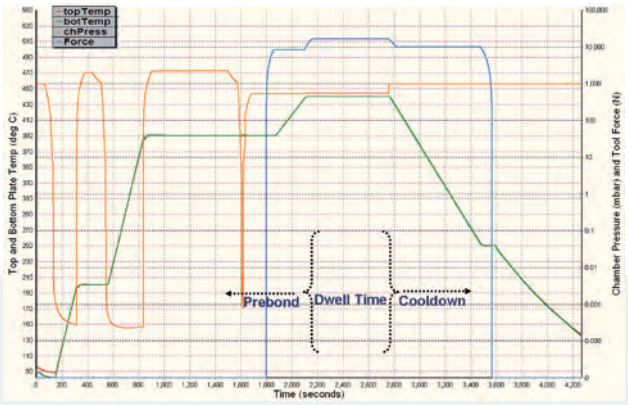

Figure 4. Bonding Process curve showing typical Al-Ge bond parameters: top and bottom chucks temperature are plotted on Left axis while chamber pressure and tool force are plotted on the right axis (log scale).

polished (100) silicon wafers for the substrate material. Figure 2 shows the SEM cross-sections of the deposited film stacks prepared for blanket AlGe bonding. As a starting point, blanket Al/Ge deposited wafers with 0.1 µm TEOS/0.5 µm Ge /1.5 µm Al were bonded to varying thickness Ge deposited on Si wafers to qualify the bond process.

Once the bond process was proven on the blanket pairs, patterned wafers were used to optimize the process and to reduce eutectic squeeze out. For aligned wafer bonding preparation, the Si cap wafer had patterned 5 - 10 kÅ Ge with varying seal ring widths while the device wafer was deposited and patterned with 10 kÅ Al plus 5 - 10 kÅ Ge on top (Figure 3). The seal ring widths varied from 10 µm to 200 µm. Both device and cap wafers had front side targets and were aligned using SUSS MicroTec BA200 bond aligner inter-substrate alignment method in which the microscopes move in between the substrates for face to face alignment.

During the alignment process, 100 µm - 200 µm thick spacers were inserted between the substrates prior to clamping to allow the flow of forming gas and consequently to pull precise vacuum between the substrates prior to bonding. Once aligned, the wafers were clamped on the bond fixture and transferred to a SUSS MicroTec CB200 wafer bonder.

bond parameters: top and bottom chucks
ber pressure and tool force are plotted on

Forming gas (95%N_2, 5%H_2) was used as the process gas while N_2 was used as the purge gas. During the bonding cycle, the bond chamber was pumped down to base vacuum at 350 °C - 390 °C, followed by introduction of forming gas in overpressure (2 bar abs). After the forming gas step, the bond chamber went through a final pump-down step. The two substrates to be bonded were separated by spacers until the final pump-down step. After the chamber reached the specified vacuum level, the spacers were removed via sequential spacer removal process and a uniform force was applied on the substrates. The temperature was then elevated to 5 - 30 °C above the AlGe eutectic point under force.

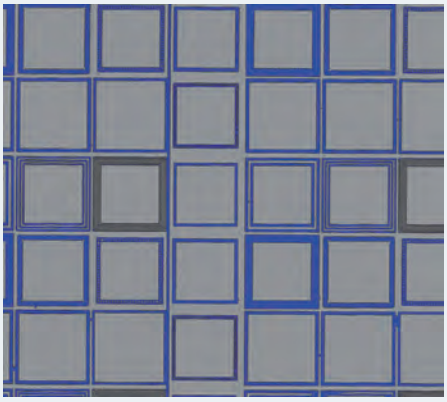

Figure 5. High-resolution SAM Image of patterned bonded Al-Ge pair section showing well-bonded seal rings. The variation in seal rings colors is due to varying seal ring widths

For these experiments, the bonding conditions were varied from 420 °C to 455 °C for the bond temperature, while the applied force and bond time varied from 15-50 KN and 2 - 30 minutes respectively. The typical bonder process profile for AlGe bonding from CB200 is shown in Figure 4. Post bond alignment was measured using an offline transmission IR (infrared) microscope. Post bonding, the bond interface was evaluated via scanning acoustic microscopy (SAM). To further investigate the bond interface, cross-sections of the samples were analyzed via Scanning Electron Microscopy

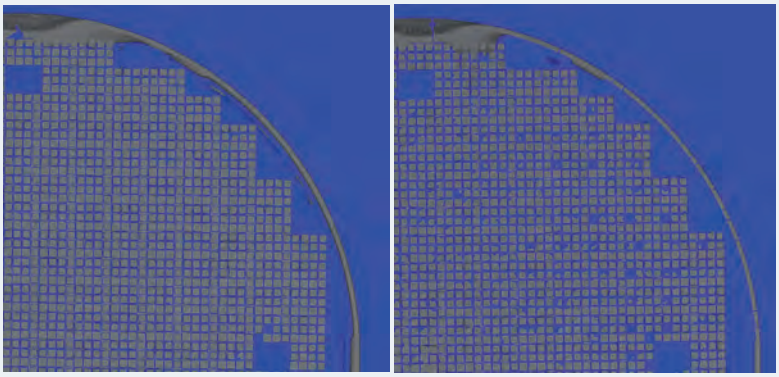

Figure 6. SAM Images of patterned bonded Al-Ge pairs showing bonded seal rings with (a) minimal eutectic squeeze- out at 440°C/ 30kN (b) excessive eutectic squeeze-out in to the cavities at 455°C/40kN

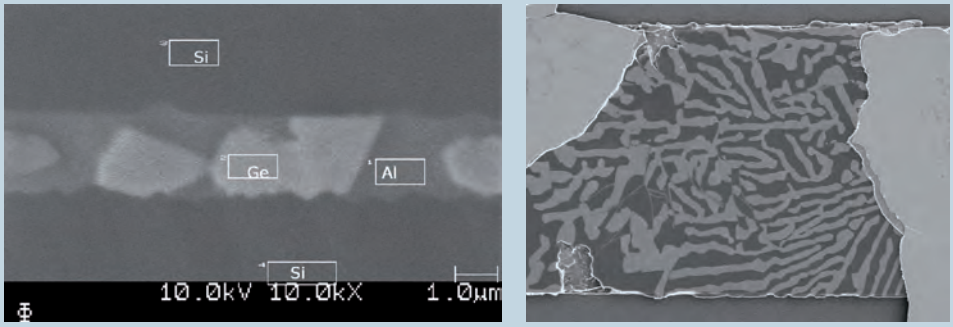

Figure 8. (a) Cross-section SEM of the bonded pair section showing void-free eutectic AlGe alloy at the bond interface (b) Plan SEM view of Al-Ge seal ring showing germanium dendrites (light) within a dark aluminum matrix

(SEM) and the presence of germanium and aluminum and their distribution was investigated via Auger Electron Spectroscopy (AES).

RESULTS & DISCUSSION

SAM & IR ANALYSIS:

Void-free bonding (SAM) for both blanket as well as patterned substrates with good post bond alignment (<3µm post bond) was observed in the temperature range 435°C - 445°C and tool force range of 20kN - 40kN. Figure 5 shows the high resolution SAM image of a section of from a patterned Al-Ge pair showing bonded seal rings with varying seal widths. Figure 6 compares the squeeze-out of the eutectic alloy from two Al-Ge runs processed at 440°C and 455°C respectively. At temperatures above 445°C, eutectic squeeze-out was observed irrespective of the tool force used owing to excessive melting while minimal squeeze-out was observed at temperatures up to 440°C. In addition, at temperature >445°C, post bond misalignment >5µm was observed which is attributed to the molten eutectic state and therefore slippage at the bond interface. Mixed bonding was observed in the 425 - 440°C range with moderate tool force (20kN - 30kN) while poor bonding was observed below 425°C irrespective to tool force up to 50kN. Figure 7 shows the transmission IR images of seal rings taken with an offline microscope and depict void free bonding and no eutectic squeeze-out with post bond alignment <3µm. X-section and plan SEM analysis of the bonded pairs shown in Figure 8 shows Ge dendrites within an Al matrix due to low solubility between Al and Ge.

Figure 7. Transmission IR images) from an offline IR microscope at 50, 100 and 200x magnification shows seal-rings from aligned and bonded AlGe substrates

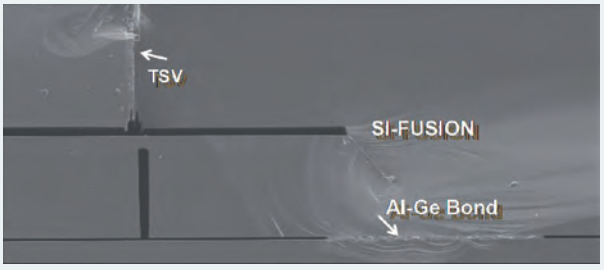

Figure 9. Cross-section SEM of triple bonded stack showing an Al-Ge bond and a Si-Si fusion bond.

CONCLUSION AND ONGOING WORK

This applications note described an optimized Al-Ge based bonding process for CMOS friendly wafer level packaging that can be easily integrated into MEMS wafer level packaging line. The integration of this process with a fusion bonding is also being actively investigated as shown in Figure 9. Ongoing process development is geared towards optimizing this process for high throughput and yield in a production environment. With optimization of pre-cleaning techniques, it is hoped that the process temperature and forces can be further reduced.

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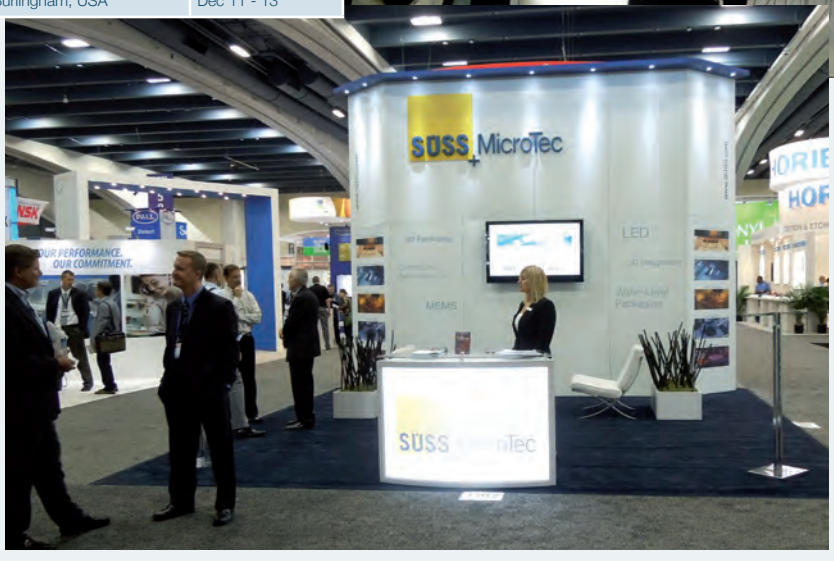

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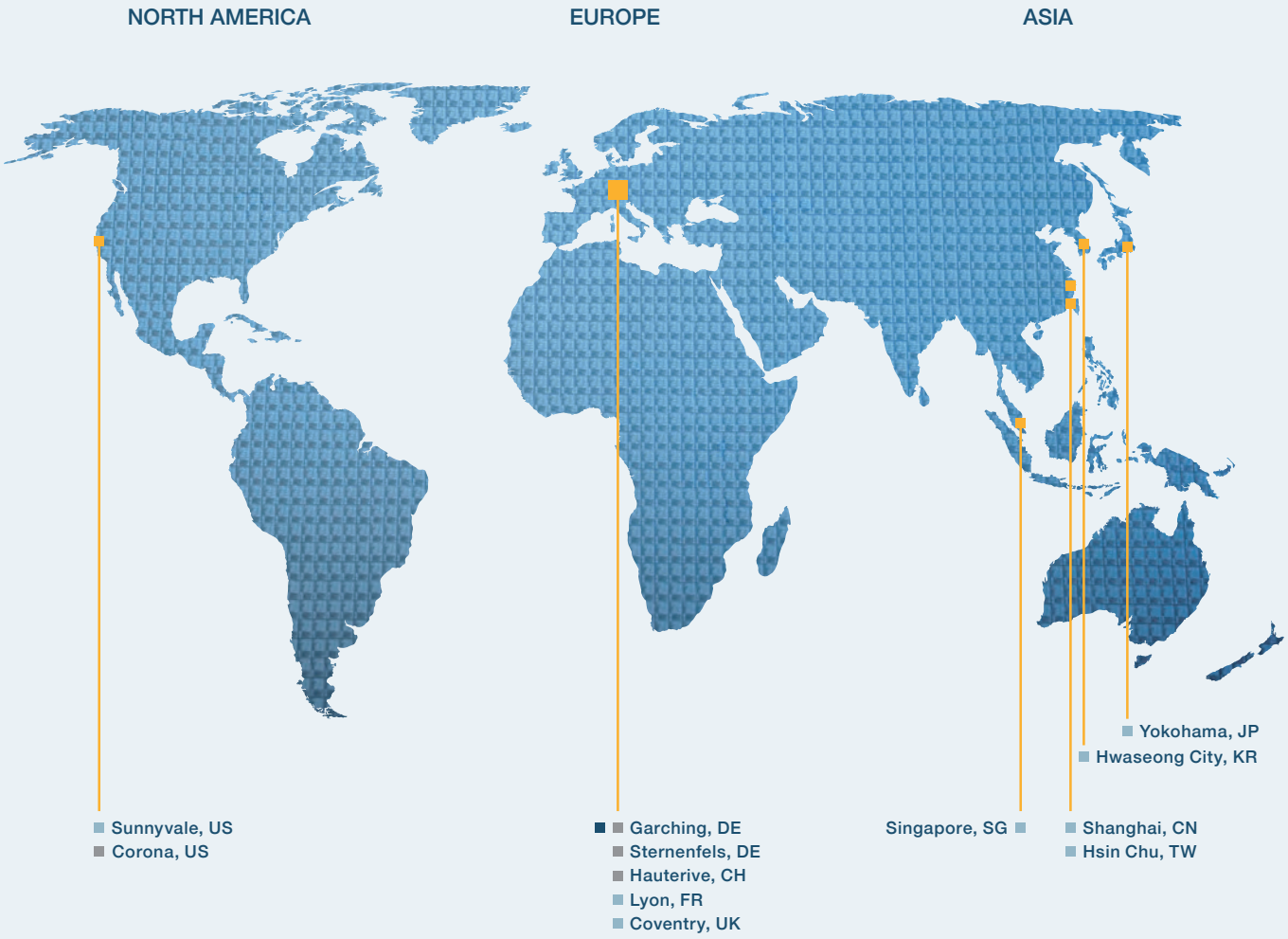

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