

300 mm Lithography and Bonding Technologies for TSV Applications in Image Sensor and Memory Products

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Abstract

Technology advances such as 3-D Integration are expanding the potential applications of products into mass markets such as consumer electronics. These new technologies are also pushing the envelope of what's currently possible for many production processes, including lithography processes and wafer bonding. There is still the need to coat, pattern and etch structures. This paper will explore some of the lithographic challenges and wafer bonding techniques as used in the 3D Packaging and will describe all the challenges and available solutions. The processing issues encountered in those techniques will be discussed with a focus on wafer bonding and lithography steps.

Introduction

The expanding consumer electronics market is clearly driving the development of today's semiconductor innovation. The push for integration, reduction in power consumption and the need for smaller form factors lead to new architectures which combine dissimilar technologies and lead to creative packaging methods, where maximum functionality is packaged into minimal space. So 3D Integration is considered the next generation packaging solution.

Today different 3D packaging approaches like SiP (System in Package), SoC (System on Chip) and SoP (System on Package) have been developed in order to answer the requirements for smaller footprint, shorter interconnects and higher performance.

SiP "System in a Package" is a functional system or subsystem with multiple wire-bonded or flip-chip dies in an IC package. Other components are placed on the motherboard, like passives, SAW/BAW filters, pre-packaged ICs, connectors and micromechanical parts. This technology enables a stacked chip package with reduced form factor.

SoC (System on Chip) integrates all the different functional blocks, like processor, embedded memory, logic core and analog in a monolithic way. These blocks are required to integrate the system design on a single semiconductor chip. SoC designs usually consume less power and have a lower cost and higher reliability than the multi-chip systems that they replace. And with fewer packages in the system, assembly costs are reduced as well.

SoP (System on Package) uses through-vias and high density wiring in order to achieve a higher miniaturization. It is an emerging microelectronics technology that places an entire system on a single chip-size package. Where "systems" used to be bulky boxes housing hundreds of components, SoP saves interconnection time and heat generation by enabling a

full system with computing, communications, and consumer functions all in a single chip [1] [2].

Through Silicon Via (TSV) has evolved as one of the key technologies for 3D integration and wafer level packaging. 3D TSV has the potential to one day replace wire bonding and thus enable further size and cost reduction and increase the performance of the device.

Today 3D TSV technology has become critical to the growth of 3D components integration, like memory stacking, or for MEMS structure packaging. The first application which is using TSV as mainstream technology is the packaging of CMOS image sensors (CIS). For CMOS image sensors, WLP is already an industrial reality. Today, already about 35% of CMOS imager sensors can be found into latest consumer cell-phones and notebook cameras are encapsulated in a WL-CSP and this number keeps growing (Fig. 1.) [3] [4].

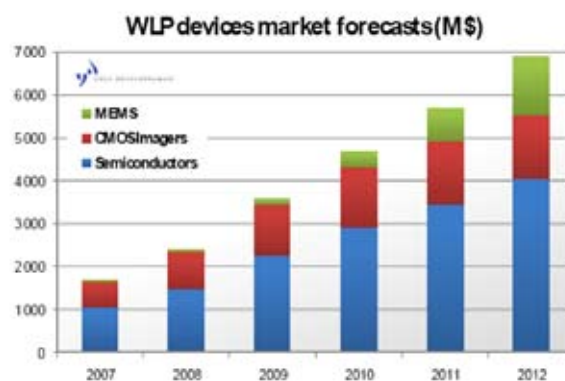


Figure 1. WLP devices market forecasts [4]

The spin-coating, photolithographic and wafer bonding processes which are necessary to create and connect these TSVs will be presented. Also the achieved results and used equipment will be described.

Process Flow

One of the typical process flows to form TSVs is shown in Figure 2. These steps are required for through silicon via wafer processing. First, the etch mask must be created. This involves coating, exposing and developing the mask. Once the mask is created, the vias can be etched and insulated. Via filling can then be completed using various materials such as copper and tungsten. The fill process is determined by the fill materials. As of today, copper is the most commonly used material for TSVs, but other materials like Tungsten (W) or Cu₃Sn alloy are used as well.

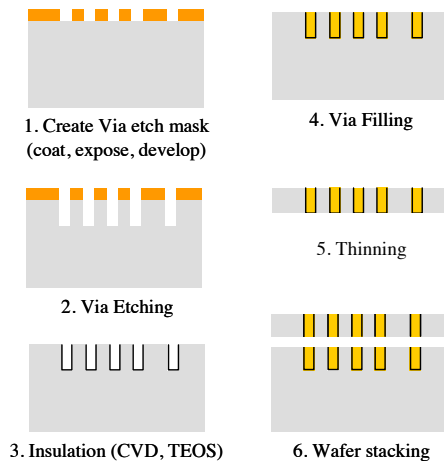


Figure 2. Typical TSV formation flow

Once the vias have been made, the wafers can be stacked using various methods of wafer bonding and micro-bumping. The steps that will be described in this paper are the formation of the etch mask and wafer stacking.

Process Details

Coating and Baking

The first steps in preparing the etch mask for vias was coating and baking of 300mm bare silicon wafers.

For this process sequence the SUSS ACS300 Gen2 coat/bake/develop cluster tool was used. This tool was equipped with the GYRSET® (closed cover coating technology) coater module for open and closed bowl coating, an aqueous type develop module as well as proximity type hot and cool plate cassettes.

Three different positive-tone photo resists were coated on 300mm wafers using a CPD pressure dispense system. First an open bowl process with no edge bead removal (EBR) was used for coating a group wafers with $0.9\mu\text{m}$ of AZ1505 (Fig. 3). Then another open bowl process was used for coating a second group of wafers with $1.4\mu\text{m}$ of AZ4110. Finally a closed cover GYRSET® process followed by an open bowl cast-off step including EBR and back side rinse (BSR) was used for coating a third group of wafers with $9.3\mu\text{m}$ of the higher viscosity AZ9260. After resist coating a 110°C proximity soft bake followed by a cooling step was carried out for all of the wafers. Different bake times were used for the different resist thicknesses.

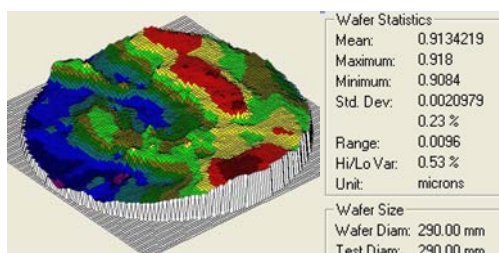


Figure 3. Coating thickness and uniformity of AZ1505

Exposure and Development

Photolithography of via openings in photo resist looks pretty straight forward. However, the various following process steps and different via sizes require specific photo resist exposure and development conditions and ask for an optimized set of parameters.

Typically via sizes down to $5\mu\text{m}$ (Fig. 4) can be easily and cost effectively achieved by 1X full field photolithography. State-of-the-art resolution limits are at about $3\mu\text{m}$ in proximity printing on 300mm substrates. However, tight CD control of via openings requires accurate gap setting, excellent light uniformity and exposure dose control. All this will affect the final exposure results and therefore need to be accurately controlled.

For the described experiment a typical via test mask having different via diameters was used. The SUSS MA300 Gen2 Mask Aligner provides an average intensity of about $90\text{mW}/\text{cm}^2$ (broadband) coupled with a light uniformity of less than 3% over the whole 300mm wafer. All wafers were exposed with an exposure gap of $20\mu\text{m}$. Figure 4 shows exposed and developed vias with a diameter of $3\mu\text{m}$ in AZ1505.

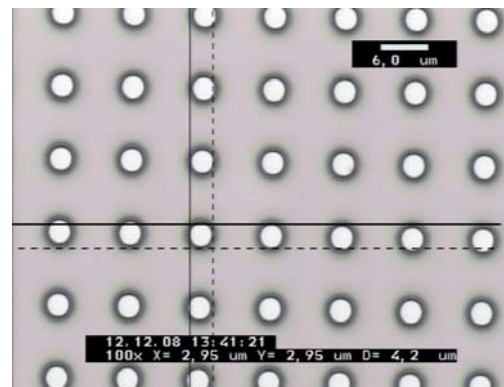


Figure 4. Exposed and developed via with a diameter of $3\mu\text{m}$ in AZ1505

The development process was again carried out on the ACS300 Gen2 using an aqueous develop module that was equipped with a binary spray dispense system. The binary spray nozzle setup and water-jacketed dispense line with temperature control to point-of-use allow for reducing process times and minimizing material consumption. Variable rate arm movement across the wafer was employed in order to optimize the uniformity of the spray process. Both, AZ4110 and AZ9260 were developed using a 1:4 dilution of AZ400K and deionized water. TMAH based AZ726MIF was used for the development of AZ1505. Figure 5 shows exposed and developed vias with various sizes.

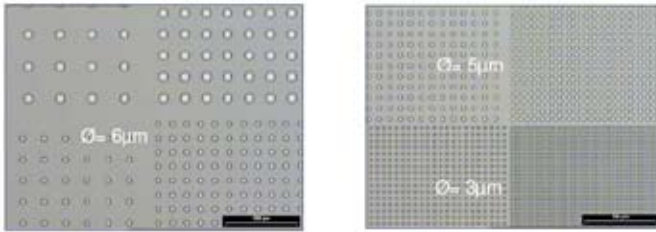


Figure 5. Exposed and developed vias with various sizes

The trend for smaller vias also requires accurate overlay of the print result. Overall alignment performance of the mask aligner as well as runout effects are the two main important factors that influence the overlay result. The SUSS MA300 Gen2 uses two novel technologies to achieve highly accurate overlay.

Alignment accuracies below $0.5\mu\text{m}$ (3σ) can be achieved on the MA300 Gen2 by adopting the DirectAlign® technology. First of all, the system accurately aligns wafer and mask in alignment gap, which is typically set to 50 - $100\mu\text{m}$. The final high accuracy alignment step is performed in exposure gap. Advanced pattern recognition software measures and controls the alignment, thus achieving sub-micron alignment accuracy.

Besides an excellent equipment performance in terms of alignment accuracy, the control of mask and wafer temperature is also crucial to achieve optimum overlay results on 300mm wafers. The MA300 Gen2 employs a temperature controlled exposure chuck to keep a constant and uniform wafer temperature and to compensate for runout effects. In a proximity printing system, mask and wafer are in close proximity to each other, assuring that the mask temperature is indirectly controlled by the chuck. Any runout, measured via pattern recognition, can be reduced by changing the temperature in the exposure chuck (Fig. 6). The ThermAlign® technology is able to reduce runout down to 0.2 to $0.3\mu\text{m}$.

During the experiment the ThermAlign® chuck was set to 22°C . The alignment was done using an automatic alignment system in direct alignment mode with SUSS proprietary alignment targets.

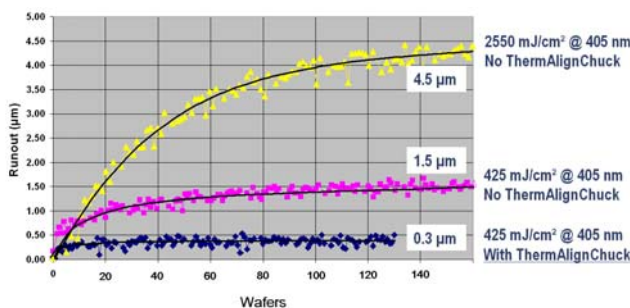


Figure 6. Runout effect between wafer and mask with and without temperature control

The achieved overlay data on 300mm wafer are shown in figure 7 and the x-y plot is shown in figure 8.

	Data left side		Data right side	
	x [μm]	y [μm]	x [μm]	y [μm]
Mean	0.02	-0.12	-0.20	0.08
Range/2	0.15	0.20	0.20	0.25
3σ	0.30	0.30	0.32	0.35
Mean+ Range/2	0.17	0.32	0.40	0.33
Overlay	0.32	0.41	0.52	0.42

Figure 7. Alignment accuracy measurement results

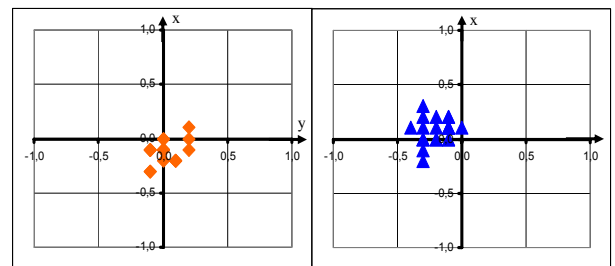


Figure 8. X-Y-plot of the measurement results

Bond Alignment

One of the most important topics in 3D Stacking is the alignment accuracy. As can be seen from the roadmap shown in fig. 9, via diameters will continue to shrink over the next couple of years.

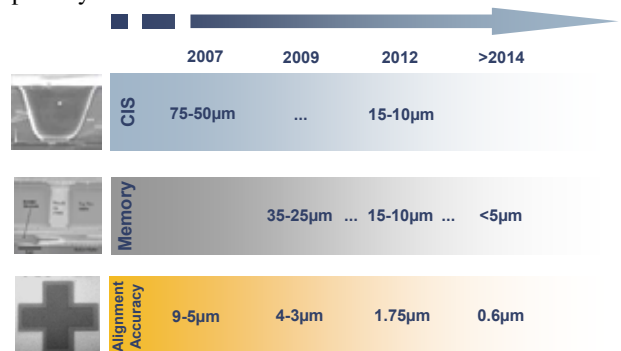


Figure 9. Post-bond Alignment Accuracy Roadmap[4]

Today via diameter in range of 25 to $75\mu\text{m}$ are used in CMOS Image Sensors devices. In memory devices typically few microns diameter is used for a TSV. For the wafer bonding technology, shrinking via diameters have a direct effect on the post bond alignment accuracy that is required. There is always a minimum overlap requirement so that metal vias have good electrical connection with minimized resistance. This minimum overlap requirement directly translates into post-bond alignment accuracy, which will be in the sub-micron range within the next couple of years.

As both of the wafers which need to be aligned for 3D stacking have metal layers IR alignment becomes impossible. Another approach is the Inter Substrate Alignment (Fig. 10).

This technique is capable of achieving the required alignment accuracies outlined in figure 9.

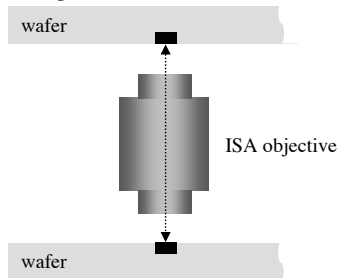


Figure 10. Inter Substrate Alignment (ISA) Principle

In this alignment technique special optics are used that are inserted between the two wafers. The ISA objectives, on left and right, image the alignment key on the upper and lower wafer simultaneously. The alignment stage moves the wafers and a pattern recognition algorithm performs the alignment according to the recipe.

After the objectives are retracted both wafers move into contact or to a predefined gap. Typically moving the wafers in the z-axis can create some misalignment. Therefore new precision optics and mechanics have been combined with global inline calibration methods to achieve sub-micron alignment accuracy in the BA300UHP (Ultra High Precision) Bond Aligner.

Bonding

Wafer bonding techniques used for 3D Stacking are mainly:

- metal to metal diffusion bonding (Cu)
- metal eutectic bonding (Cu/Sn)
- silicon fusion bonding
- adhesive bonding (BCB)

There are a lot of pros and cons for each kind of bonding process. Which one will be chosen depends on the application and its requirements. However, there is a clear trend for metal to metal diffusion bonding using copper as bond layer. The advantage of this bond process is that the electrical as well as mechanical connection is done simultaneously.

Copper-Copper Bonding

When two metals are pressed together under applied force and heat, the atoms can migrate from lattice site to lattice site bonding the interface together. Such diffusion processes require intimate contact between the surfaces since the atoms move lattice vibration. Copper or Aluminum are optimal for such diffusion processes due to their ductile properties and fast diffusion rates. Copper bonding requires temperatures in the range of 300°C up to 400°C to achieve a good hermetically seal interface. The oxidation of copper can hamper the bonding process. It can be cracked by applying a high force during the bonding or to incorporate a vapor

cleaning process to remove the surface oxidation. Using the vapor from formic acid (HC00H) in a bubbler, SUSS MicroTec has developed a point of use removal system for metal oxides. Wafers are placed in cleaning chambers and exposed to the vapor for a few minutes. The chamber is purged and by controlling the partial pressure of O₂ in the module no salts are formed that required post process rinses. The process is totally dry and the copper surface is stable for several hours. [5]

Metal Eutectic Bonding

Eutectic bonding is also of interest for 3D stacking due to the low temperatures, which are beginning at 231°C for Cu₃Sn (Fig. 11). Thus the most often requested eutectics are AuSn, AuSi, AlGe, and CuSn, as already mention. It also required the usage of inert gas to prevent oxidation.

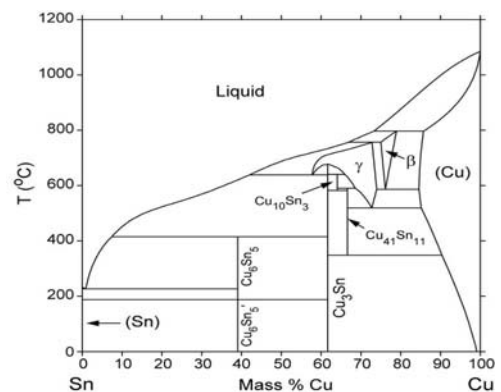


Figure 11. CuSn phase diagram

Silicon Fusion Bonding

Fusion Bonding is interesting for 3D stacking due to the very short process times and high bond strengths. Nevertheless during the fusion bonding only the mechanical contact is created. However, there are no direct electrical connections across the interface to interconnect the metal layers. Additional processing is therefore required to etch through the wafer stack and backfill vias with metals. This is done by thinning one of the substrates to several tens of micrometers and follow by a patterned etch and metal backfill in a process known as “via last” processing.

The drawback to fusion bonding is the requirements for surface flatness and roughness. Another issue is the limitation in the annealing temperature due to the used metal materials in the wafers. But using plasma treatment the annealing temperature can be reduced from ~1000° down to the required 200°C - 400°C.

Silicon fusion bonding needs the following process steps:

- plasma treatment creating a hydrophilic surface with a specific chemistry and contact angle
- DI water cleaning combined with reactivation and bonding
- temperature annealing in a standard furnace 8batch process)

Adhesive Bonding

Adhesive bonding is very often used in 3D due to the low range of process temperature and the topography tolerance. The most often used polymer for precision 3D adhesive bonding is BCB (benzocyclobutene) and is bonded from 150°C-320°C. The flow properties of BCB can be manipulated in order to provide low temperature bonding and alignment accuracies in the range of 1-2 μ m. BCB needs to be coated on one or both wafers, the use of adhesive promoter AP3000 is absolutely essential. Before bonding the BCB needs to be baked out. Figure 12 shows the BCB film structure at different baking temperatures. If the procuring is below 150°C not all solvents are removed. So the bond will almost certain result in a poor mechanical connection.

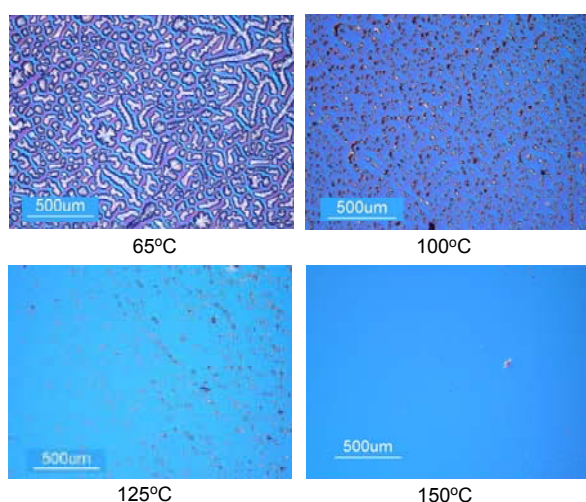


Figure 12. BCB film structure baked at 65°C, 100°C, 125°C and 150°C for 1h before bonding at 250°C

Conclusions

In this paper the lithography and bonding techniques were introduced. The coating, exposure and developing of different resists were described. Also the alignment and bonding techniques used in 3D were illustrated with their advantages and drawbacks. Some required equipment characteristics were introduced, which are beneficial especially for processes in 3D Integration. Also process results, like developed via holes in photo resists, which is necessary to create an etch mask for further processes, were shown.

Currently the only applications in 3D in production are CMOS image sensors. These products use lithography processes and metal bonding technology for CU TSVs and also the fusion and adhesive bonding techniques at wafer level. But there is a lot of development in 3D ongoing, which hopefully will make production processes also available for other applications in the near future.

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