LITHOGRAPHIC CHALLENGES AND SOLUTIONS FOR 3D INTERCONNECT

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ABSTRACT
In order to integrate higher levels of functionality within a package, designers have employed creative strategies wherein multiple chip sizes, types or even materials have been combined into a single unit. Joining heterogeneous chip types such as optical, mechanical, and switching circuits has even been pursued to fabricate highly complex packages such as image sensors, biological or chemical sensing devices.

In the effort to create this new generation of advanced devices, designers have increasingly turned to the vertical dimension to increase the density and minimize the space, weight and power consumption. Chip stacking, through-silicon vias (TSV's) and other vertical integration strategies have led to an increase in the Z dimension, which has created a new set of challenges for process engineers. Among these challenges are the needs to coat, pattern and etch structures which may have tens or even hundreds of microns in height. This paper will explore some of the lithographic challenges associated with 3D interconnection technology, where use of the vertical dimension has necessitated new methods of conformally coating high topography, new imaging techniques to align various masking levels to the underlying patterns, and new exposure techniques to accomplish high fidelity patterning over such high structures.

Keywords: lithography, photoresist, conformal coatings, 3D Integration and Packaging, exposure

INTRODUCTION
Since the dawn of the micro-electronics age in the 1950's, there has been a consistent push to house ever-greater functionality in ever-smaller confines. The trend began when scientists discovered that they could create various functional elements such as resistors, transistors, diodes, and the like, all on the same piece of semiconductor material. Thus, the integrated circuit was born, and with it, the electronics age.

This revolution has continued into the present day, enabled by such technologies as UV and DUV lithography, fine-pitch plasma etching, selective depositions of materials like tungsten, and highly uniform ion implants at medium or high current levels. As each new device generation was conceptualized, designers would shrink the required circuit geometries to pack greater electronic functionality into smaller spaces. Moore's law, calling for exponential growth of circuit functionality, stated that the number of circuit elements would double approximately every two years. [1] To keep up with this market demand and the required shrinkage of geometries, chip fabricators would require the surface of the semiconductor to be highly planar so that the new and smaller features could be printed within the depth-of-focus (DOF) of the imaging system.

But Moore's Law alone cannot maintain the necessary progress in circuit density. The market continues to ratchet up the requirements for electronic systems, driven by such consumer markets as automotive control systems, handheld electronics, imaging devices and gaming systems. To meet this demand, a new era is emerging for miniaturization, one in which the circuit is being built not only in the X and Y dimensions, but also in the Z dimension. To keep up with demands for chip performance, chip designers continue to shrink the XY dimensions of the circuit features, but are also building up functional elements in the Z direction by means of multi-level interconnects, chip stacking and even integration of heterogeneous devices. And along with increases in functionality come the increased challenges in power delivery, cooling and signal input/output. [2] The increased use of the vertical dimension is referred to as 3D Interconnect.

As the circuit is built up in the Z direction, topographical steps are being created which are well beyond the coating and printing capability of conventional lithographic techniques. While relatively planar substrates with topographies less than a few microns in height can be patterned by spin coating a photoresist material onto its surface, the topographies being utilized in 3D Interconnect may be built up to a height of tens or even several hundred microns – far beyond the capabilities of conventional spin coating and photolithographic printing. Short- or mid-term main applications which demand this integration in the 3rd dimension include CMOS image sensors, stacked memories, and true heterogeneous integration of disparate circuit elements such as CMOS switching circuits, MEMS sensors and power circuitry. The motivation for this integration includes the form factor of the device (reduced volume, weight, footprint), performance, (increased

integration density, reduced interconnect length, higher speed, lower power consumption) and the need to have varying functions within the same electronic system. [3] High topographical steps such as trenches, mesas, and the now-popular through-silicon-via (TSV) have been created to capitalize on the available Z dimension in creating greater chip complexity within a small space.

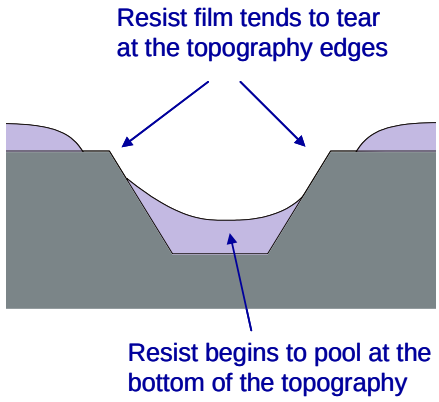


Figure 1: High topography coated by spin coating results in non-uniform resist coverage

Figure 1 depicts a generic trench structure as might be found in various process flows. But if this trench were ten's of microns in height and were to be coated by the historical method of spin coating, various physical forces of rheology would dominate the process and the photoresist coating would likely be highly non-uniform, as depicted. [4] This resultant coating is unacceptable for a lithographic patterning process, as the critical upper corners of the trench are not covered at all and would result in an "open" in the coating continuity. Perhaps just as detrimental would be the pooling of the resist in the bottom of the structure, resulting in an undesirably thick layer which would be very difficult to expose and develop. So spin coating, while maintaining its prevalence in coating low to moderate topography, simply cannot adequately coat structures with high topography as are found in 3D Interconnect. A new resist deposition method is needed whereby the resulting coating is highly conformal, following very closely the high topographical steps of the underlying substrate, such as depicted in Figure 2.

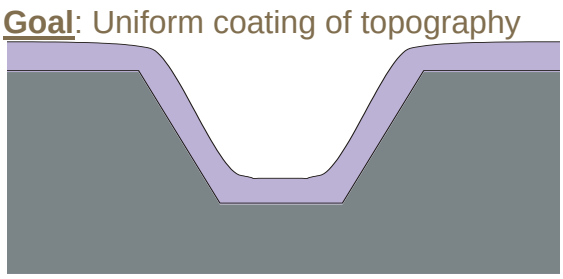


Figure 2: Ideal conformal coatings over high topography

After coating the high topographical step, the next problem would arise when trying to align the masking level to the previous structures and expose the conformal resist coating over such topography. In some circuit layouts high topography used to create a dense circuit has created a difficult scenario for alignment by obliterating the targets or placing them on varying planes of the substrate. Since all imaging systems have a practical depth of focus – the vertical dimension over which they can resolve a certain feature size – they are limited in the topographical step over which they can print the required circuit geometries. If the lithographic process is to support the increase in topography required by 3D interconnect, it must meet this three-fold challenge to coat, align and expose features over high topography.

EXPERIMENTAL

In order to conformally coat these tall structures, a new method has been proposed which does not employ conventional spin coating of the resist. Rather than allowing the resist to flow in a viscous state and to follow the forces of rheology, the fluid would have to impinge on the substrate initially in a fluid state, then "freeze" or dry very quickly so that the fluid is not allowed to flow or pool in response to gravity, centrifugal force, or the surface tension of the film.

A spray-coating technique has been proposed [5] which creates an aerosol from the diluted photoresist, mixes it with a carrier gas, then delivers the aerosol to the stationary substrate by means of a nozzle mounted onto an XY shuttle system. Since the thinned photoresist arrives on the heated and stationary wafer, it is allowed to flow for only a short period of time before the film dries and becomes a solid surface.

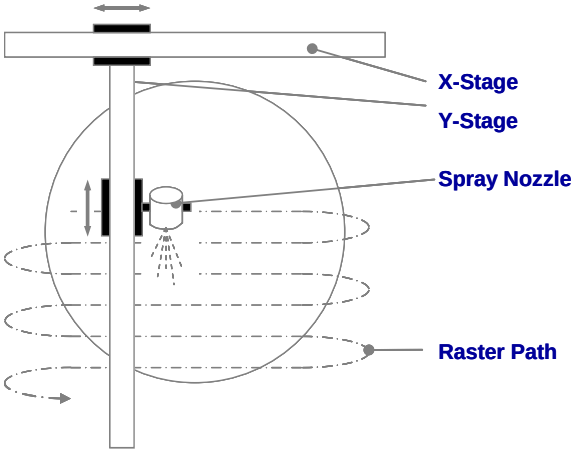


Figure 3: Layout of Spray Coat Apparatus

The apparatus is depicted in Figure 3 and employs a binary nozzle for creating the resist aerosol, an XY stage, and a heated chuck to hold the wafer. The binary nozzle is mounted to an arm a certain distance above the substrate, and is supplied with a flow of photoresist and nitrogen pressure. As small, controlled volumes of photoresist are delivered to the nozzle, the nitrogen is mixed with the resist to create a stream of very small droplets. Many different materials have been successfully spray coated, and materials are typically diluted

with their native solvents down to a viscosity of only a few centipoise.

The binary nozzle is mounted to an arm on an XY translation stage. This stage transports the binary nozzle at a programmed slew rate to all portions of the wafer. This slew rate and the stepping pitch have been determined by properties of the material and the substrate topography. Figure 4 shows the resulting photoresist deposition pattern on the substrate after one pass and after multiple passes. By selecting appropriate resist flow rates, N2 dispense pressure and chuck temperature, the resist droplets impinge onto the wafer surface and dry very quickly, allowing the resist to flow only a desired amount or not at all.

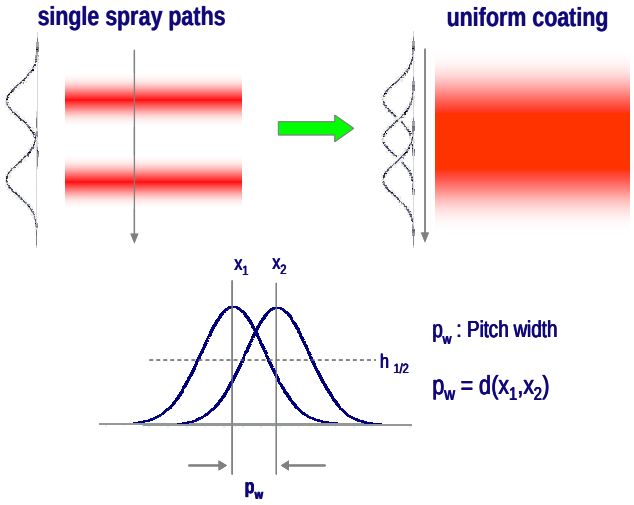
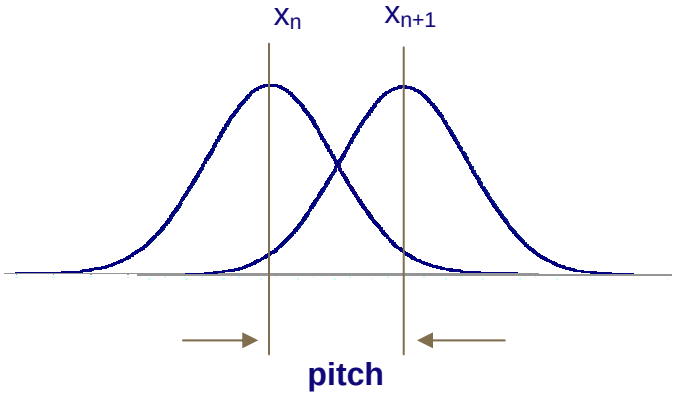


Figure 4: Coating Pattern after Multiple Passes with Spray Coat Apparatus

To achieve a uniform, conformal layer of material on the topography, the spray head is directed across the entire substrate with multiple passes of arbitrary substrate rotation. The desired coating thickness is determined by follow-on process requirements such as etching, deposition or stripping; the spray coat process is repeated until the desired coating results have been achieved. Figure 5 depicts the modeled results of such a sequential spray-rotate-spray process, indicating that more uniform results are obtainable with a stationary wafer and an XY raster of the resist nozzle than with a rotating wafer and sweeping the resist nozzle. Empirical results confirmed the model over a large variety of topography shapes and sizes.



Spray Profile:

$$p_n(x) = a_0 * e^{-\frac{b0}{(x+n*pitch)^2}}$$

Thickness on

$$\sum_n p_n(x)$$

!

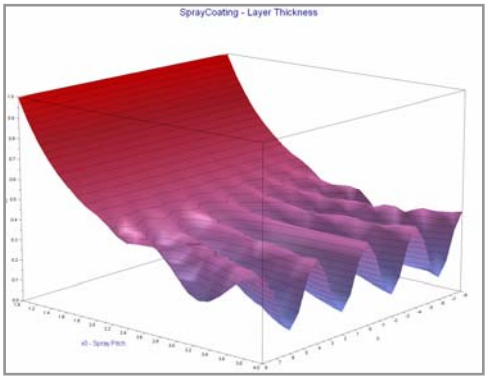


Figure 5: Modeling of sequential coatings on a stationary wafer

After the substrate has been conformally coated, the next step in the lithography process is to align the present mask level to the previous layer's, then expose the photoresist to create a pattern. The same topographical steps which were a challenge to the coating process may mean that the previous layer's fiducial patterns may lie on a much different image plane, and they may even be obscured by deposited layers or damaged by intermediate processing steps.

Figures 6 and 7 show a number of alignment fiducials typical of what a process engineer might employ, including box-in-box, cross-in-cross and other such structures. But due to the deposited layers or other optical or mechanical effects, the size, shape, contrast or even the tone of the targets' images can change from wafer to wafer or within the wafer.

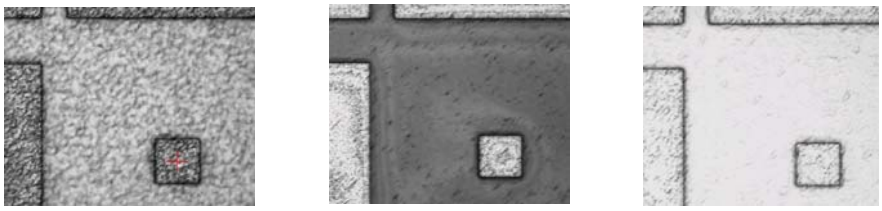


Figure 6: Contrast and tone changes within the wafer or lot.

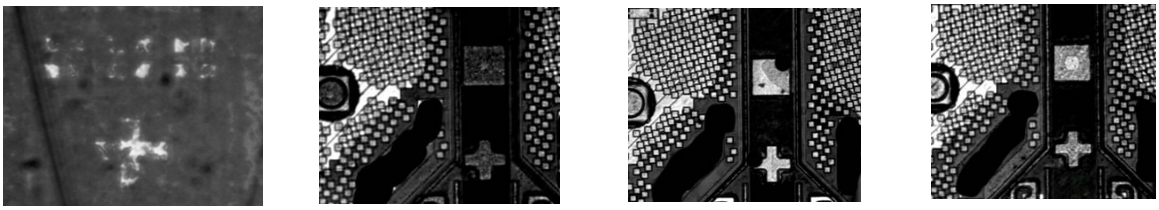


Figure 7: Examples of damaged or obliterated targets

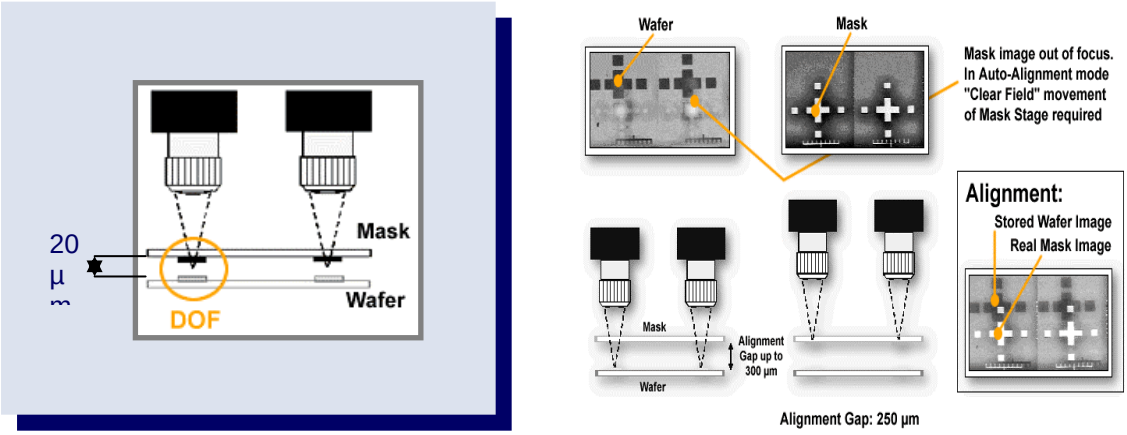


Figure 8: An image capture system to align fiducial targets despite limited depth-of-focus of the alignment optics

Leading-edge alignment software, supplied by the Cognex PATMAX© system, coupled with stable, high-resolution alignment optics, are able to consistently align these difficult targets in a production environment. Even alignment targets which may lie hundreds of microns away from the top surface of the substrate are able to be successfully aligned with an image capture system.

To address the issue of limited depth-of-focus of the alignment system, an apparatus has been employed to repeatably set the height of the imaging objective at selectable positions. A precision focusing rack minimizes the alignment error which could be introduced by this method. By means of specialized hardware and software, the alignment system captures, stores and displays the image from one focal plane (e.g. mask) while displaying the live image from another focal plane (e.g. wafer). As shown in Figure 8, the operator or automated alignment system can clearly and accurately determine and correct any alignment error between the two target positions before the exposure takes place.

A specific alignment challenge in the 3D application space is created by certain process flows which call for patterning the reverse side of the substrate. In this case, the circuit patterns on the front side of the wafer have been completed, and the process calls for additional circuit elements – backside vias, discrete components such as inductors and capacitors – to be created on the backside. Typically, the substrate is temporarily mounted to a carrier using an adhesive with the patterned side down. Next, the substrate is thinned by backgrinding and polishing techniques, then the backside lithography can take place. A mounted and thinned wafer is depicted in Figure 9.

Figure 9: Wafer mounted on supporting carrier, ready for backside lithography

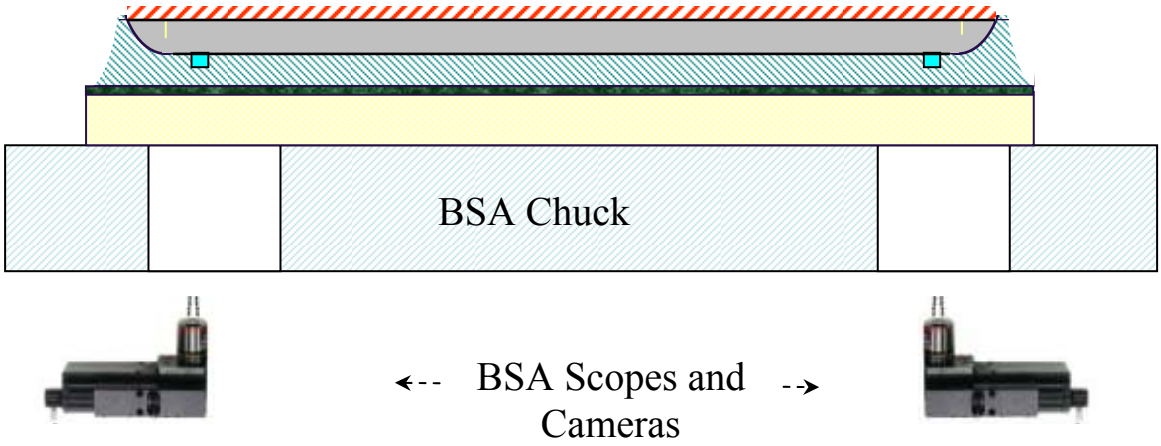


Figure 10: Backside Alignment (BSA) method to align to targets

To align to the patterned side of the substrate, the alignment system must be able to image this side of the wafer, even though it is now face down on the alignment chuck as shown in Figure 10. Utilizing a backside alignment system analogous to the image capture system to that described above and shown in Figure 8, the photomask images can be captured and stored before the wafer is loaded into the tool, then the real-time image of the bottom-side wafer targets can be easily aligned to the stored image of the mask.

Alignment for 3D applications is further complicated by the fact that some lithographic levels may even need to be aligned to a layer which has either been covered by an opaque mounting glue, or has been obliterated by deposited films such as subsequent circuit layers or opaque films. To align in this case, the tool has been outfitted with infrared alignment hardware as depicted schematically in Figure 11 so that even buried circuitry is visible to the alignment system.

The final portion of the lithography process is to expose the conformal resist with the appropriate UV light. Again the issue of high topography places special burdens on the exposure tool due to many factors such as the depth-of-focus of the exposure optics, plus the transparency of the photoresist if printing through thick films. While most exposure systems are designed with high effective numerical aperture to maximize the printing resolution, this design would yield very limited depth of focus. For 3D interconnect applications, a special optical system, dubbed LGO for Large Gap Optics, has been employed which maximizes the usable depth of focus for the moderate geometries typically encountered in this application. Diffraction patterns from a conventional imaging system and an optimized large gap printing system are shown in Figure 12.

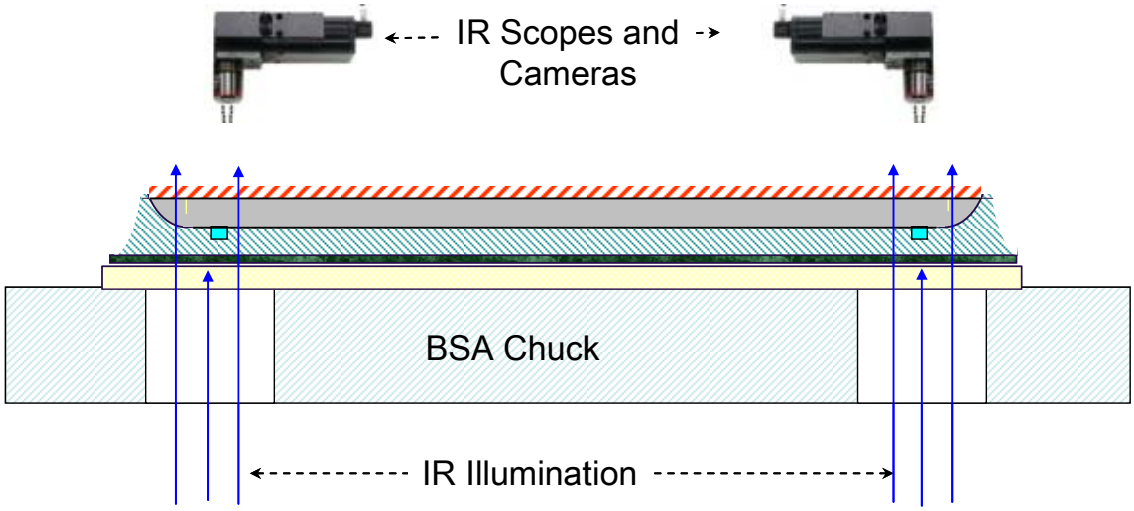


Figure 11: Infrared viewing apparatus to align to buried or obliterated targets

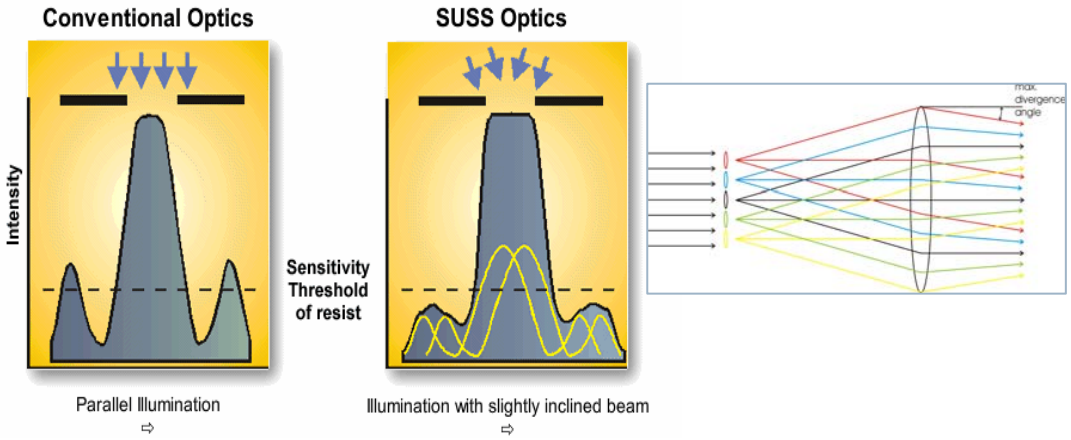


Figure 12: Collimation angle in printing optics has been tweaked to create Large Gap Optics (LGO), optimized for printing features at larger exposures gaps

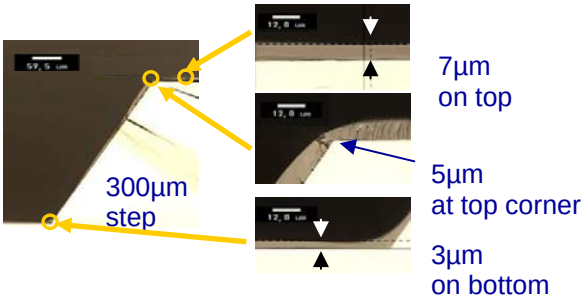


Figure 13: Modified BCB4024 conformally coated onto a v-groove

RESULTS AND DISCUSSION

Structures encountered in 3D interconnect schemes often involve high topography such as trenches, mesas, columns and via holes. Though these structures have been used in previous circuit generations, the dimensions and sheer number of these geometries within 3D interconnect is unprecedented. Figure 13 shows a trench structure which has been conformally coated with the spray coat apparatus described above.

The degree of confomality of the Dow Chemical BCB4024 material is notable not only because of the uniformity on this high topography, but also because of the planarizing nature of this material in normal use. Structures of even sharper feature angle and greater aspect ratio are also successfully coated with a commercially available photoresist from AZ Electronic Materials, shown in Figures 14 and 15.

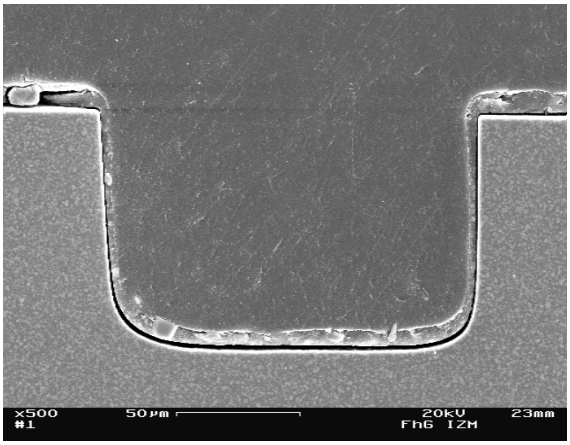


Figure 14: Trench of 90degree sidewall coated with spray apparatus and AZ4999 resist.

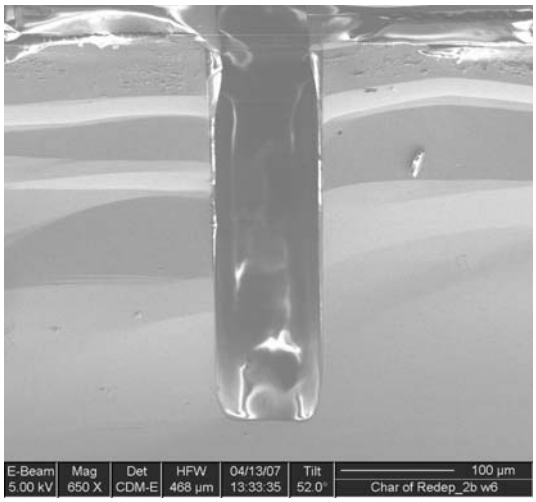


Figure 15: Deep trench with 6:1 aspect ratio coated with spray apparatus and AZ4999 resist. Image courtesy of Seagate Research, Inc.

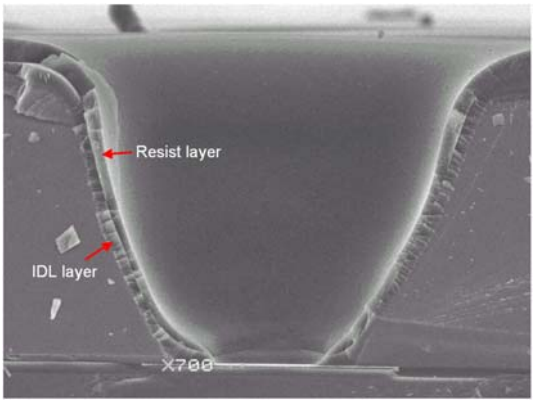
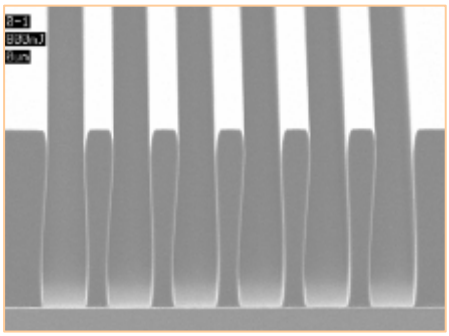


Figure 16: Good step coverage of spray-coated dielectric on a sloped via. Image courtesy of Schott Advanced Packaging

A CMOS image sensor was fabricated using the spray coat setup; images of the tapered vias coated with a conformal dielectric layer and a conformal imaging resist are shown in Figure 16.



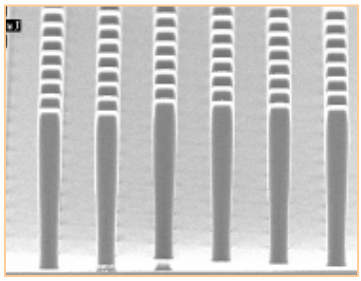


Figure 17: AZ EXP125NXT-10A resist exposures, 60µm thickness, exposed on SUSS MA200 aligner. Nominal measurement for the lines, spaces and columns is 10µ. Images courtesy of AZ Electronic Materials.

Analysis of the spray-coated vias indicated that the process was well under control and delivered very uniform conformal thicknesses of dielectric and resist layers, meeting the process specs for the production scenario. [6] This process uniformity contributed to an electrical probe yield between 92% and 96% for the tested lots, verifying

that the dielectric and photoresist deposition processes yielded excellent electrical results. Process modeling shown in Figure 5 as well as measured results on real wafers agreed that uniform conformal coatings could be produced only if the wafer were stationary, not rotating, during the spray coat process.

A variety of structured customer wafers and test wafers were conformally coated with photoresist using the spray apparatus described above, then exposed with the LGO optics for maximum depth of focus in the exposed image. These structures, including dense lines/spaces, contact holes, sloped trenches, and completely vertical structures, were selected because they are representative of the high aspect ratio features commonly encountered in many process schemes in the 3D interconnect and related market spaces. Some of the tested images are shown in Figure 17.

The very clean, near-90 degree photoresist profiles were realized due to the optical properties of the resist as well as the exposure optics of the exposure tool. Even with thick photoresist and high aspect-ratio exposures, the feature was very clearly defined and was without a "foot" (undeveloped or under-developed residue where the resist meets the substrate), as shown in Figure 18.

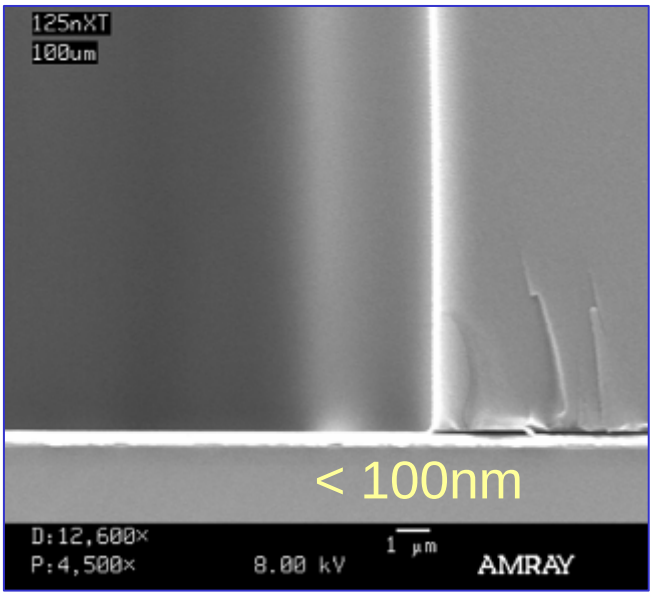


Figure 18: AZ EXP125NXT-10A, 70µm thickness. No foot was present at bottom of image when exposed on SUSS MA200 aligner tool. Image courtesy of AZ Electronic Materials.

Not only must features be resolved in thick photoresists with high aspect ratio, but also features which traverse great topographical steps or even lie at the bottom of deep features. To qualify these aspects of the coat and expose process, trenches of 200µ depth were conformally coated with commercially-available AZ4999, then exposed with the LGO exposure optics described above. The results show a very uniform coating of resist on all areas of the trench, plus very consistent linewidth measurements even as the exposed line travels up and down the trench, as depicted in Figure 19. An even greater lithographic challenge is to resolve small features at the bottom of cylindrical structures such as contact holes or TSV's. Figure 20 indicates successful resolution of 10µ features at the bottom of 80µ deep vias. For this type of structure, overlay of 0.5µ at 3σ was achieved, as shown in Figure 21.

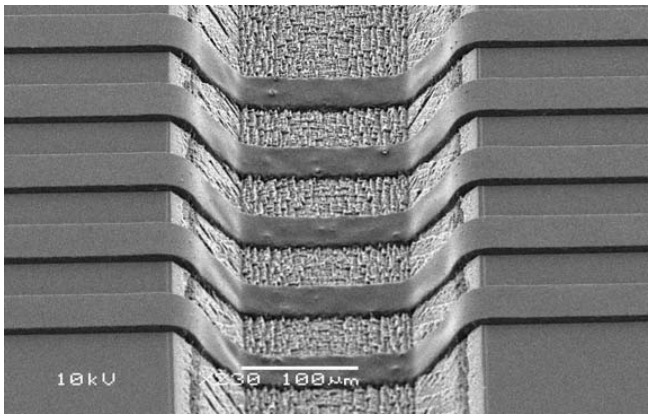


Figure 19: 10um of AZ4999 resist conformally coated onto 200um deep trench, then exposed with LGO optics. Note that linewidth of exposed structure is very uniform even over high topography.

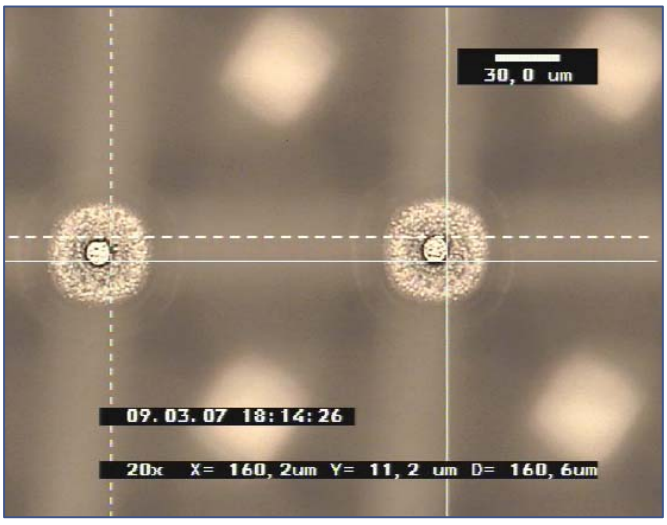


Figure 20: 10µ features successfully resolved at the bottom of 80µ deep vias. The structures were conformally coated, exposed and developed with the spray coating and exposure apparatus described herein.

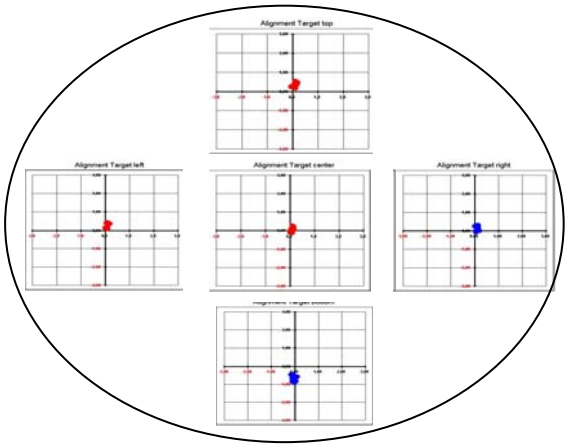


Figure 21: Scatter Plot of Alignment Results; 0.5μ at 3σ were achieved

CONCLUSIONS AND RECOMMENDATIONS

To continue to increase value to the customer, designers and technologists are turning to the vertical dimension of the substrate to maximize performance while minimizing chip size and power consumption. This technique of 3D interconnect leads to larger topographical steps on the substrate which are beyond the printing capabilities of conventional lithographic systems for coating and exposing such high steps. New methods have been proposed to meet this challenge which include spray coating of the photoresist layer, advanced imaging techniques to view and align the alignment fiducials, and printing optics with greater depth of focus. Apparatuses for these techniques have been proposed and applied to typical structures encountered within the field of lithography over high topography, with the results showing the effectiveness of these new methods for this 3D technology.

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