LED Production on the SUSS MA100e Gen2 Mask Aligner

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Light emitting diodes (LEDs) are increasingly used in many lighting products covering not only the visible spectrum but also ultraviolet and infrared applications. To replace conventional light bulbs the costs for the production of LEDs must be low. Historically, the semiconductor industry has relied on increasing the diameter of silicon wafers in order to push productivity and lower cost. LEDs, however, are made from compound semiconductors rather than from silicon. And while red LEDs can already be manufactured on 150mm GaAs wafers other compound semiconductor substrates for technical reasons are still limited to a wafer diameter of 2, 3 or 4 inches. Therefore, the demand for increased productivity and lower cost needs to be met by dedicated equipment that combines highest throughput with the ability to meet the particular technological requirements and cost constraints of the LED industry.

These requirements can be met by the new MA100e Gen2 Mask Aligner from SUSS MicroTec. On the basis of the well established SUSS MA150e, the MA100e Gen2 was optimized for small wafer sizes up to 4 inch and is equipped with a special high throughput upgrade, including a new pre-aligner, especially designed for transparent wafers.
With the high throughput upgrade on the MA100e Gen2, up to 145 wafers (215 wph first mask mode) per hour can be exposed in auto alignment mode.

For LEDs in the short wavelength range (green, blue, ultraviolet) the commonly used materials are group III – nitrides. As GaN substrates are still very expensive, the GaN layers are grown on less expensive sapphire wafers. In contrast to conventional silicon IC technology sapphire substrates as well as the functional layers of the LED are transparent to visible light. Even electrical contact layers such as indium tin oxide (ITO) are transparent. Thus the contrast of micro structures (e.g. alignment keys) on the patterned wafer is typically very poor and therefore challenging for the alignment system. In order to increase the efficiency of LEDs the wafer is often textured (roughened) before depositing the functional layers adding another challenge to the pattern recognition system. The surface roughness causes light scattering and diffuses the image of the alignment target (see Figure 1).

The alignment microscope and camera system of the MA100e Gen2 in combination with its advanced alignment software, however, can cope with this

Figure 1:
Microscope image of an alignment target on a GaN-Wafer. The contrast between the target cross and the background is very poor.

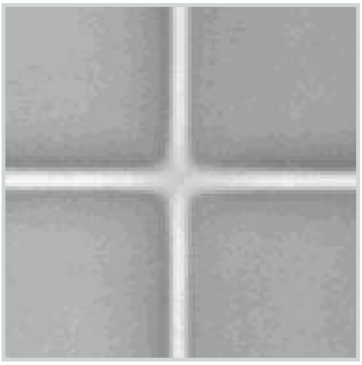

Figure 2:
Image of the alignment target on the screen of the MA100e Gen2. The contrast is good enough for training and auto alignment.

challenge. Figure 2 shows the image of the alignment target when using the SUSS MA100e Gen2. Obviously, it offers much better contrast than the image obtained from a standard optical microscope. Generally, pattern recognition and alignment is no problem with the MA100e and targets are found even if the surface background changes on each wafer. For these challenging targets, however, careful target training is essential.

Due to the crystal lattice differences of sapphire and GaN, these wafers often tend to exhibit a dome-like warpage caused by strain. With the special warped-wafer-handling system of the MA100e Gen2, such wafers can be handled efficiently and reliably.

Resolution requirements are still fairly relaxed compared to standard IC technology. Lift-off processes are common because the quantum efficiency of LEDs is sensitive to the condition of the wafer surface. However, new types of photoresists such as the DNR-L300 series from Dongjin Semichem Inc. (South Korea) are increasingly used. The DNR-L300 is a negative acting chemically amplified resist. The advantages of this material are that it is developed in common aqueous base developers and is easy to strip/lift-off with organic solvents. As a chemically amplified resist it delivers straight sidewalls even when exposed in larger proximity gaps.

In the following example the DNR-L300 resist was coated on 2-inch sapphire wafers using the manual SUSS Delta80 Coater. The mean layer thickness was 2.95 µm ± 1.16% (1s). The MA100e was equipped with UV400 High Resolution Optics and a 1000W mercury lamp. The achieved resolution of lines and spaces depends slightly on the wafer surface and the evenness of the top epitaxial layer (Table 1). The surface of a deposited GaN layer is not as even as that of a silicon or GaAs wafer (see Figure 3).

The exposure optics of many low-cost aligner feature only a resolution limit of about 5 µm with this resist. The MA100e Gen2, therefore, features superior exposure results than competing equipment and can cope with all lithography challenges given by the LED manufacturing process.

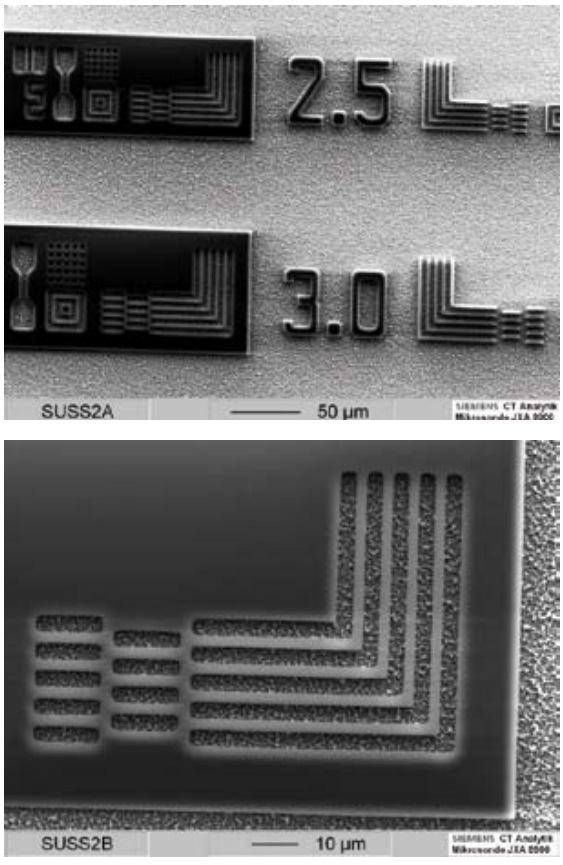

Figure 3:
Electron microscope images of 2.5µm and 3µm lines and spaces in a 3µm thick layer of Donjin DNR-L300 D1 negaive tone resist.

Contact mode	Lines and spaces resolution
Proximity 20 µm	≤ 3.5 µm
Soft contact	≤ 3.0 µm
Hard contact	≤ 2.5 µm
Vacuum contact	≤ 2.0 µm

Table 1: Resolution of MA100e Gen2 in 3µm thick negative tone DNR-L300 resist. The given resolution refers to the resolution limit on the most challenging surface.