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Abstract

This paper introduces the new MA8 Gen3 Aligner generation designed specifically for the development of 3D and MEMS packaging technologies. Photolithography on the wafer backside, wafer bonding and replication of microstructures are specific 3D / MEMS processes. They have in common that all of them require precision alignment and often will have to run on ultra-thin wafers. The MA8 Gen3 allows to run all the processes above on a unified equipment platform and therefore offers the ideal equipment solution for 3D and MEMS technologies.

A second focus of this paper is at the applicability of electrostatic carriers as a thin wafer handling solution for the processes mentioned above. Electrostatic carriers are a straight forward and cost effective handling solution. They are not based on temporary adhesive wafer bonding and therefore do not require expensive adhesives or other consumables.

The electrostatic carriers and the multi-functional Aligner platform combined result in a very cost effective manufacturing solution for 3D and MEMS packaging. The advantages of this solution will be discussed in more detail for the wafer-level manufacturing and assembly of camera modules and for Plasma Dicing.

Key Words: Mask Aligner, Replication, UV Bonding, Image Sensors, Plasma Dicing, Thin Wafer Handling

Introduction

3D and MEMS packaging involve process steps that are not common to semiconductor manufacturing. Among these processes are photolithography on the wafer backside, wafer bonding and replication of microstructures. These processes have in common that they require precision alignment with a trend for the alignment accuracy towards the sub-micron range. As an additional challenge, these processes will have to run on ultra-thin wafers.

Presently, much of the research and development of 3D packages and ultra-thin wafer handling is geared towards a low cost and reliable manufacturing process for Through-Silicon-Vias (TSVs). There are, however, many more design features of 3D packages or MEMS devices that require innovative equipment solutions. Interestingly, wafer-level camera modules that are currently under development for use in next-generation mobile phones are early adopters of many of these new process techniques.

The wafer-level camera currently drives many equipment innovations that will become key for cost effective 3D and MEMS packaging later on. The reason why the wafer-level camera is a forerunner is that manufacturers don't have to solve the thin-wafer-handling problem: CMOS image sensor wafers are permanently bonded to glass wafers prior to back-grinding. These glass wafers act as mechanical support for the thinned CMOS wafers. Since the glass wafer becomes an integral part of the camera module the thin wafer does not have to be de-bonded, an important detail that significantly simplifies the manufacturing process.

Within the manufacturing process of wafer-level cameras one can identify two complementary technologies. One is the wafer-level packaging of image sensors [1] and the other is the wafer-level manufacturing of camera objectives [2]. Both the sensor device and the objective are then assembled on wafer level by a wafer bonding process. The wafer-level packaging of image sensors was pioneered by Shellcase/Tessera (Israel/USA) while

the wafer-level manufacturing of micro objectives was pioneered by companies like Heptagon (Finland/Switzerland).

A Multi-functional Aligner Platform

As these technologies are under development for several years now, existing equipment platforms have been modified to address resulting new process requirements: For example, the manufacturing process of wafer-level camera modules includes several processes that require precision alignment:

- Through-Silicon-Vias
- Backside RDL (redistribution layer)
- Plasma dicing
- Wafer-level imprinting (micro lenses)
- Wafer-level bonding (lens stacks)

Unfortunately, compromises have often to be made when modifying existing equipment platforms leading to less-than-ideal solutions. Therefore, SUSS MicroTec has decided to completely redesign their manual Aligner product family in order to develop an equipment platform that integrates all innovations of recent years in a well thought-out tool design. The result is the MA8 Gen3, the third generation of our MA8 product line (Figure 1). The MA8 Gen3 manual Aligner supports Photolithography, UV replication, UV bonding, standard bond alignment and Nano-Imprint-Lithography processes. It has been designed to offer improved alignment capabilities in terms of accuracy, flexibility and user friendliness. In particular, many new features of the MA8 Gen3 lead to improved process control which in return makes this tool generation more suitable for production environments. In fact: Beyond its use in R&D environments the MA8 has always been utilized in specialized production environments. In particular, this is the case whenever non-standard semiconductor materials are used that cannot be handled easily by conventional automated equipment. As long as production volumes are not very high manual equipment can be more cost effective than using modified automated machines. The wafer-level camera is an example where manual equipment is very common because of the strong wafer warpage after wafer thinning. In consequence, the MA8 Gen3 has developed into a next-generation Aligner platform for many new research and production areas.

Wafer-Level Camera Modules

In the following the flexibility of the new MA8 Gen3 will be discussed with the example of manufacturing wafer-level cameras. Usually, the purpose of TSV technologies is to realize high-density vertical interconnects between vertically stacked dice. TSVs are typically etched prior to wafer thinning starting from the front side of the wafer. On the other hand, with the image sensors discussed in this paper the TSV is part of the package design. Therefore, TSVs are etched after wafer thinning starting from the wafer backside. Consequently, the etch mask has to be patterned on the backside of the wafer. This requires an accurate alignment of the etch mask (photoresist) to the contact pads on the opposite side of the wafer. Backside lithography is possible by using Mask Aligners with Bottomside Alignment (BSA) systems. BSA systems have been available on Mask Aligners for many years and are commonly used in MEMS. They are, however, largely unknown in the Advanced Packaging industry.

Figure 1: The MA8 Gen3 supports photo-lithography, UV bonding, UV replication bond alignment and NIL

Next to the photolithography function Mask Aligners are perfectly suited for replicating microstructures into UV curable polymers. This technique has been developed some years ago as part of the European Dondodem Project for replicating optical elements such as diffractive gratings, deflection mirrors or micro lenses [3]. In case of camera modules imprinting is used for replicating the lenses of the camera's objective. The process is shown in Figure 2. A UV transparent PDMS stamp is loaded onto a stamp holder. Next, a UV curable polymer with suitable properties (e.g. optical transmission, refractive index, thermal stability to survive a reflow process) is dispensed onto a glass wafer. Then wafer and stamp are brought into contact at a force strong enough to replicate the patterns of the PDMS stamp into the polymer. UV exposure cures / hardens the polymer and finally stamp and wafer can be separated again. The similarity to contact photolithography is obvious. The PDMS stamp corresponds to a photo mask while the UV curable polymer corresponds to the photo resist. In fact, this replication process can be done on a modified Mask Aligner with an increased contact force and a modified levelling of

stamp and wafer. In case lenses have to be imprinted onto both sides of the wafer aligned imprinting is necessary. In order to guarantee a good optical imaging quality of the resulting lenses an excellent post replication alignment accuracy is a must. Because of the mechanical forces acting during the imprinting step shear forces that would deteriorate the alignment accuracy have to be minimized. This can be done by an accurate levelling of stamp and wafer in addition to a mechanically robust design of the alignment system. The alignment and levelling system of the MA8 Gen3 has been significantly improved compared to the previous tool generation in order to allow highly reliable imprinting processes.

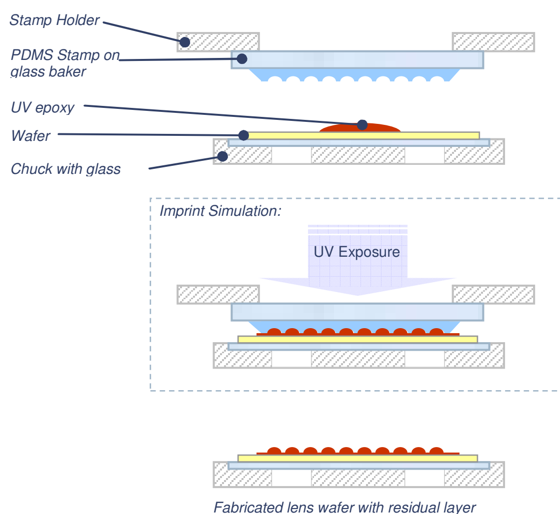

Figure 2: Micro lenses can be manufactured on wafer-level by imprinting a UV curable polymer. Hundreds of micro lenses can be replicated in only one process step.

Camera objectives usually are composed of a set of lenses. Assembling single lenses into a lens stack (objective) is time consuming and expensive especially if lenses become very small. With the lenses manufactured on wafer-level, however, it is straight forward to apply a wafer bonding process in order to assemble the lens stacks on wafer-level as well. Like in the previous example the alignment and contact printing function of Mask Aligners offer easy means to use this equipment for wafer bonding. In MEMS technology wafer alignment and wafer bonding are usually not implemented in an "in-situ" equipment setup. Instead, dedicated tools - the bond aligner and the wafer bonder - are used. The reason is that many bond processes are difficult to combine with delicate alignment mechanics especially when vacuum or high temperature processes are needed.
While with many MEMS devices the wafer bond has to seal a vacuum cavity the stacking of micro-lens wafers has no such requirement. Therefore, adhesive bonding is a good option. Moreover, lens wafers are transparent which allows to cure the adhesive by UV rather than curing the material at elevated temperatures. These two facts allow for a very simple and cost effective in-situ bonding process on a mask aligner type of equipment. The principle setup is shown in Figure 3. The Mask Aligner requires a modified mask holder that can hold the top lens wafer. Wafer alignment, wafer contact and UV exposure are the same operations as with standard contact printing. The main difference is in the wafer handling sequence as the wafer pair has to be removed from the machine after bonding. In a photolithography process the mask typically remains in the tool for subsequent exposures. Obviously, post bond alignment accuracy is critical for the overall optical performance of the objective. At the same time the accurate control of the distance of individual lenses in a lens stack is important. Therefore, the dispense volume and dispense pattern of the adhesive has to be controlled in such a way that an even and void free spreading of the material is achieved on the wafer. Finally, the Aligner has to ensure an excellent levelling of both wafers to avoid generating a wedge in the adhesive layer. And of course, the mechanical setup has to be robust enough to avoid shear movements which would deteriorate the post bond alignment accuracy.

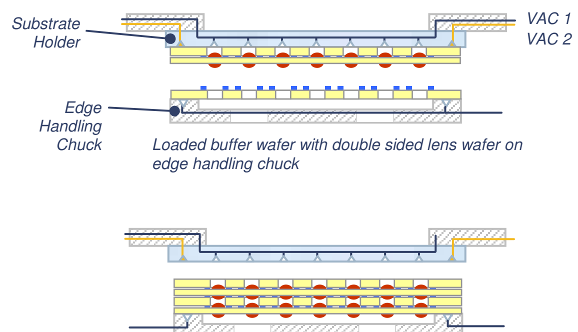

Figure 3: In-situ UV bonding on the MA8 Gen3 is very cost effective way to assemble complex micro objective at wafer-level.

The MA8 Gen3 is currently under evaluation by several manufacturers of wafer-level-cameras. At this point of time it appears that it will become a standard in this particular industry. As stated above the wafer-level camera can be considered cutting edge for other 3D packaging innovations except for the thin wafer handling issue. The question is whether replication technology and UV bonding can be instrumental to realize design features of other future 3D packages. It appears desirable as all these processes support wafer level packaging / assembly and in consequence a highly parallel and cost effective manufacturing.

Thin Wafer Handling

As stated above many 3D packaging processes will require a solution for thin wafer handling. The processes discussed before will only be applicable to 3D packaging if they can be realized on very thin wafers with the possibility to de-bond the thin wafer from its supporting carrier. At this point of time it appears to be an industry consensus that very thin wafers will require such a supporting carrier. Several concepts exist, most of them based on temporary adhesive wafer bonding. Material suppliers that offer specialized adhesives include:

- Brewer Science [4]
- 3M [5]
- Thin Materials [6]

A key issue with all these temporary wafer bonding processes is how to separate the thin wafer at the end of the process chain without damaging the wafer. This problem does not come by surprise because on the one hand the adhesive has to ensure a mechanically, chemically and thermally strong adhesion during wafer processing but on the other hand has to allow for an easy separation at the end of the process flow. These somewhat contradicting requirements make it difficult to find a reliable and cost effective manufacturing process.

A very different approach is based on electrostatic carriers [7][8]. This technology has been pioneered by the Fraunhofer IZM and is currently commercialized by companies such as ProTec Carrier Systems. Electrostatic carriers hold the wafer by an electrostatic field generated by the carrier. Electrostatic forces are strong enough to hold the wafer over a long period of time and during standard semiconductor processes. Since no organic chemicals are involved electrostatic carriers can stand up to very high process temperatures (> 400°C). And since electrostatic carriers are typically manufactured from standard Silicon wafers using standard Silicon processes they can be considered compatible with semiconductor technology.

For SUSS MicroTec the reason for looking into electrostatic carrier technology was driven by a joint project with Panasonic Factory Solutions. As part of this project Panasonic and Suss develop a Plasma Dicing process involving photo lithography and plasma etching. Plasma Dicing allows extremely accurate and narrow dicing street and avoids edge chipping. As shown in Figure 4 the Plasma Dicing process requires a photo resist etch mask on the flip side of the thin wafer. It is a key characteristic of Panasonic's process that the plasma etching is starting from the wafer backside. Therefore, metal test structures in the dicing streets don't have to be plasma etched. In order to be compatible with standard back-end processes the back-grinding tape will remain on the wafer during the entire process. While the tape is stable enough to survive the photolithography process including resist bake the biggest challenge is in the plasma etching process as care has be taken that no gas is trapped in the tape/wafer interface that may burst during a high vacuum process. At the same time the thermal coupling of the thin wafer has to be good enough to avoid excessive heating of the wafer during etching. To have solved these issues is part of Panasonic's proprietary technology.

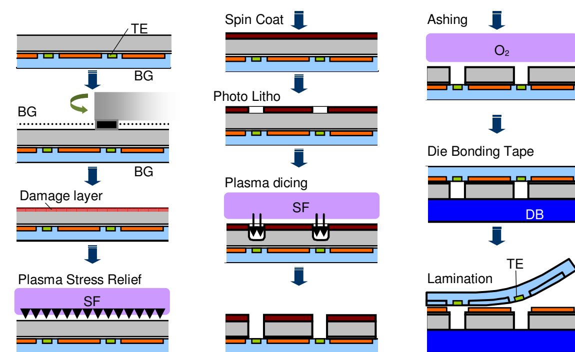

Figure 4: Plasma Dicing process flow (Panasonic)

While the tape lends some stability to the thin wafer it is still not rigid enough to be processed by standard lithography equipment. Therefore, we were looking into a carrier technology for the lithography process. If any of the temporary bonding techniques based on adhesives gains an industry wide acceptance such a solution might be very suitable for Plasma Dicing. However, at this point of time these technologies are not readily available. Therefore, we decided to evaluate the Transfer Electrostatic Carrier (T-ESC) technology.

There are uni-polar and bi-polar carrier designs. Figure 5 shows the principle design of a bi-polar carrier. A bi-polar carrier has two electrically isolated electrode structures on top. A voltage is applied between both electrodes and the carrier is charged similar to a capacitor. Charging the carrier generates an electrostatic field which has – due to the design of the carrier - the capability to attract a wafer located on top of the carrier. If sufficiently charged this attracting force is strong enough to hold the wafer during semiconductor processes. The de-bonding / de-chucking process is straight forward. It simply includes a de-charging of the carrier which eliminates the force pulling wafer and carrier together. The design of a uni-polar carrier is even more simple: The uni-polar carrier has only one electrode and the wafer acts as the second electrode. A voltage is applied between carrier and wafer and both are attracted by an electrostatic force similar to the electrodes of a capacitor.

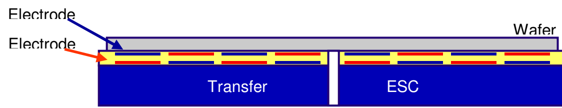

Figure 5: Principle design of a bi-polar Electrostatic Carrier

The T-ESC technology evaluated in this paper has been provided by ProTec Carrier Systems GmbH. A first run with standard High-Temperature-Carriers did not deliver good results during the photolithography processes. Problems occurred during any process involving wet chemicals of low viscosity. In case of photolithography such chemicals are used for resist developing and resist stripping. In both cases the wet chemical (solvent) is pulled efficiently between the carrier / wafer interface because of capillary forces. The effect could not even be prevented when spinning the wafer at high speed during the process. Figure 6 shows such a T-ESC carrier after de-chucking the wafer: Residues of the developer media are clearly visible at the edge of the carrier but easily can cover the entire carrier surface as well (and in consequence the backside of the thinned wafer). These residues typically will cause strong forces between carrier and wafer which makes the separation of carrier and wafer difficult.

Figure 6: Standard T-ESC carriers should not be used in the lithography process because wet chemicals (e.g. developer) are pulled between carrier and wafer.

Therefore, in a joint project, ProTec and SUSS have developed a specialized carrier design for use in a photolithography process. In order to reduce the capillary forces between wafer and carrier a step was cut into the edge of the carrier and order locally increase the gap between wafer and carrier at the wafer edge. By this means the capillary forces are significantly reduced. If the carrier/wafer is rotated at an elevated speed during the process the centrifugal force acting on the liquid in addition to the reduced capillary forces keep the interface between wafer and carrier clean. This proved essential for an easy separation of the thin wafer from the carrier.

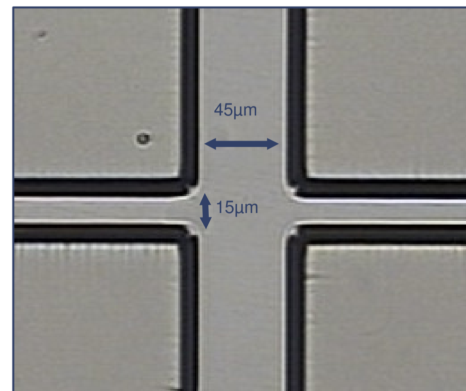

Figure 7: Resist etch mask consisting of a 15µm thick AZ 9260 resist with 15µm and 45µm wide dicing street patterns.

The T-ESC carrier technology was then applied to the Plasma Dicing process. 100µm thin wafers mounted on back-grinding tape where chucked on the modified electrostatic "Litho"-carriers. Then the photolithography process was done on standard automated processing equipment (SUSS ACS200 Coat/Develop Cluster, SUSS MA200Compact Mask Aligner). The boundary condition of having to spin the wafer at high speed during develop requires the modification of the develop recipe and may potentially lead to increased consumption of developer. However, the process ran without problems and carrier and wafer could be separated after the process without any damages. In case of Plasma Dicing the resist is stripped in the plasma chamber by plasma ashing and therefore no wet chemical process is needed. Figure 7 shows the resulting resist edge mask. A 15µm thick AZ 9260 resist film was used in order to provide sufficient resist thickness to withstand the etching process. 15µm and 45µm wide dicing streets, respectively, have been exposed into the resist film demonstrating how narrow dicing street can be when applying Plasma dicing.

Conclusions

In this paper we have introduced a new Mask Aligner platform that supports a number of wafer-level processes than can be instrumental for 3D packaging. In conjunction with the utilization of Transfer-Electrostatic-Carrier technology this equipment solution has the potential to offer very cost effective means for realizing even very advanced 3D package designs. No matter how complex future packaging technologies may become, cost will always be a significant factor defining the commercial success. The MA8 Gen3 and T-ESC technology will make a good match.

Acknowledgements

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