ABSTRACT

Eutectic metal bonding of wafers is used in advanced MEMS packaging and 3D integration technologies. A unique feature of eutectic metals is the melting of the solder like alloys that facilitate surface planarization and provide a tolerance to surface topography and particles. Often it is assumed that the alignment in eutectic metal bonding is compromised from the liquid phase transition and precision alignment is not possible. This is not true in advanced wafer level bonding using 2-3um thick metal layers. Precision control of bonding force and temperature prevent the aberrant viscous flow of the metal and prevent wafer slippage.

Key words: Eutectic bonding, wafer bonding, MEMS packaging, Au-Sn, Au-Si, Cu-Sn.

PRECISION WAFER TO WAFER PACKAGING USING EUTECTIC METAL BONDING

Shari Farrens, Ph.D., Chief Scientist, and Co-Author
Sumant Sood, Sr Application Engineer, SUSS MicroTec

INTRODUCTION

Hermetic packaging of sensors has historically been achieved with glass frit and anodic bonding techniques. However, these techniques are presently limiting scaling of devices and are not appropriate for integration plans for CMOS compatible MEMS.

The widespread use of glass frit bonding can be attributed to its tolerance to particles and surface topography, hermetic quality of the seals, and inexpensive processing costs. In comparison, eutectic alloys provide better hermeticity levels, are equally tolerate to roughness and particles and enable device scaling and integration.

EUTECTIC REACTIONS

A eutectic reaction is a triple point in a binary phase diagram in which the liquid metal solidifies into a solid alloy without going through a two phase, solid + liquid equilibrium region. Because the solidification is immediately realized the atomic rearrangements necessary to establish the equilibrium distribution of phases in the alloy is not fully achieved. The morphology of the grains within the eutectic solid are very small and best described as “feather-like”. This fine grained interdigitated structure is extremely rigid and strong. The fine grain size limits interdiffusion and corrosion.

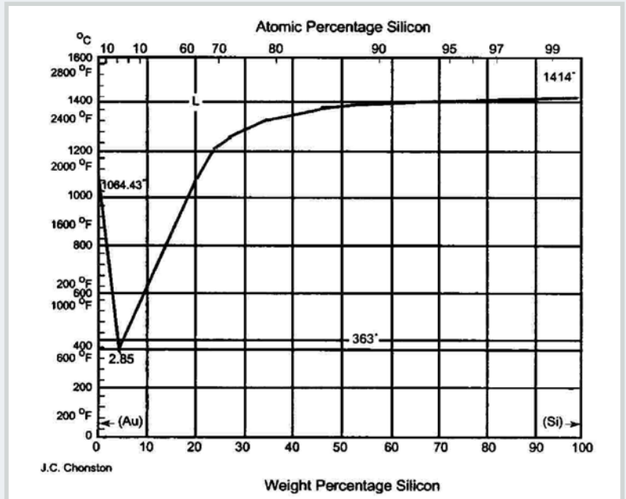

Figure 1:
Au-Si Binary Phase Diagram

Figure 1 is the phase diagram for Au-Si. This phase diagram is a classic eutectic example in which the pure fcc Au phase is denoted as α and the pure silicon diamond cubic phase is β. The diagram shows that there is very little miscibility in either Au or Si and alloys of Au and Si will consist of a two phase mixture of α and β. When an alloy of 2.85wt Si is heated the solid will immediately turn to liquid above 363C avoiding both the α+liquid and β+liquid two phase regions.

Table 1:
Eutectic Alloys used in MEMS Packaging

Alloy	Eutectic Temperature	Eutectic Composition
Al-Ge	419 C	49/51 wt%
Au-Ge	361 C	28/72 wt%
Au-In	156 C	1/99 wt%
Au-Si	363 C	97/3 wt%
Au-Sn	280 C	20/80 wt%
Cu-Sn	231 C	1/99 wt%

MATERIALS SYSTEMS

There are several alloys choices based on Cu or Au eutectic metallurgies. Table 1 shows the commonly used alloys along with the eutectic compositions and the eutectic temperature. All of these alloys have been used in MEMS packaging, or optical MEMS.

The Al-Ge system is also applicable to ternary eutectic reactions between Al and SiGe layers because Al forms a binary eutectic reaction with both Si and Ge. This system is particularly CMOS friendly.

DEPOSITION TECHNIQUES

There are two fundamental methods for creating a eutectic seal. The first method involves deposition of pure materials which then are diffused together until the eutectic composition is reached. Then the eutectic alloy can be melted and reflowed to achieve the seal. By contrast the binary alloy can be deposited as a single layer already at the composition necessary to achieve a eutectic reaction.

Eutectic alloys can be plated, sputtered or evaporated onto the substrates. There are several sources for alloy sputter targets that are ideally suited to thin layer deposition and many of the alloys can be electroplated at eutectic compositions. Because the quality of the electrical connections, as well as the reaction kinetics, are adversely affected by impurities the deposition should be done as clean as possible. Incorporation of oxygen and other gases in the thin films during deposition can lower the diffusion rates dramatically as will impurities from the electroplating bath.

It is necessary to use adhesion layers when using metal seal technologies. The semiconductor surfaces or glass surfaces should be properly cleaned to remove any previous photoresist layers or other materials remaining from earlier etching or patterning steps. Standard substrate cleaning methods before metal deposition include standard RCA1 and RCA2 or Piranha (sulfuric acid, water and hydrogen peroxide). To remove organics or to clean metal surfaces dry plasma treatments have been effective.

Typical adhesion layers include TiW, TiN, W, Cr, Ni and vary with the substrate used. The adhesion layer is very important to ensure that the strength of the interface is not limited by thin film delamination.

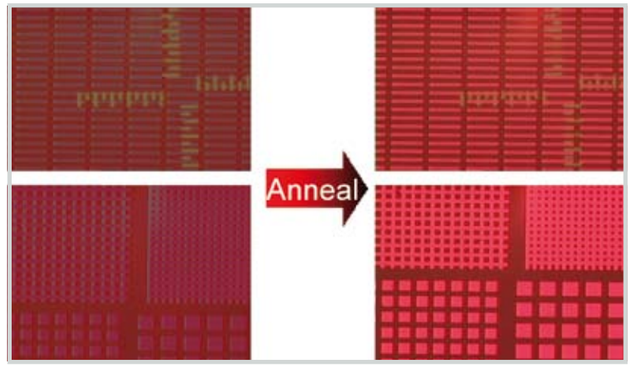

Figure 2:
Formic acid vapor cleaned Cu surface before and after heating to 400C.

SURFACE PREPARATION

The diffusion of metals as well as the solidification of eutectic phases is inhibited by contamination and oxide layers. In most fabrication facilities the timing of the device wafer and cap wafer process are such that one or the other set of substrates may be queued up for bonding before the other. This delay time between deposition of metal layers and actual bonding can lead to surface oxidation. To achieve high yields and reproducible lots, point of use surface preparation is advised to make sure that metal layers are clean just prior to bonding.

Based on experience in die-to-die and C4NP advanced bumping tools it has been established that formic acid vapor cleaning is very effective for most eutectic alloys, low temperature solders, and aluminum as well as copper in the removal of surface oxides. [2,3]

Vapor phase cleaning can be accomplished in batch processing or as a one wafer at a time, point of use, cleaning. In both cases the wafer(s) are placed in a closed chamber or cleaning station.

The formic acid vapors are introduced and the surfaces oxides are removed. The wafers are then rinsed in DI water and spun dry in the cleaning station. In automated bond cluster tools such as the SUSS MicroTec ABC200 this is done with one or two wafers simultaneously for increased throughput. The formic acid treatment passivates the surface of the metals and prevents reoxidation during the rinse, dry and alignment process that follows.

Figure 2 shows a copper surface that was cleaned with the formic acid vapor, rinsed with DI megasonic water and spun dry. Then the wafer was heated to 400C to see if reoxidation would occur. It does not and this method is used for Cu-Cu bonding in 3D integration technology.

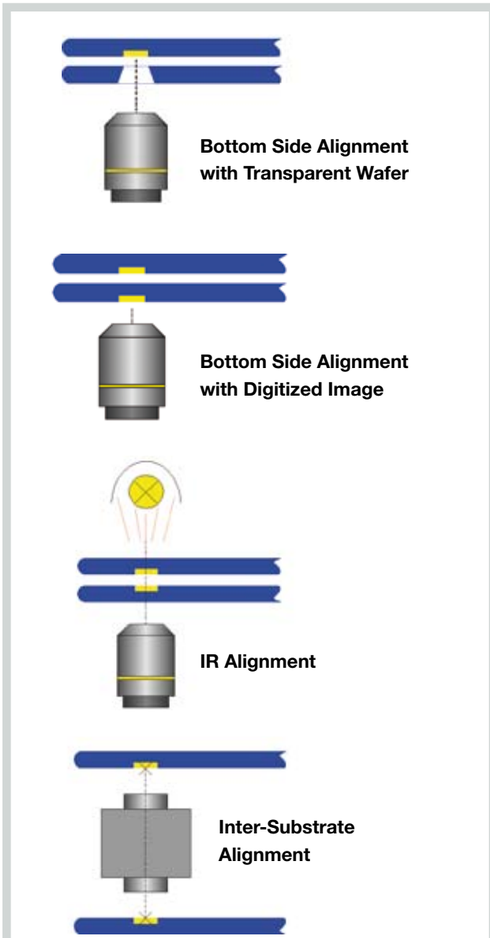

Figure 3:
Position of optics for wafer to wafer bond alignment.

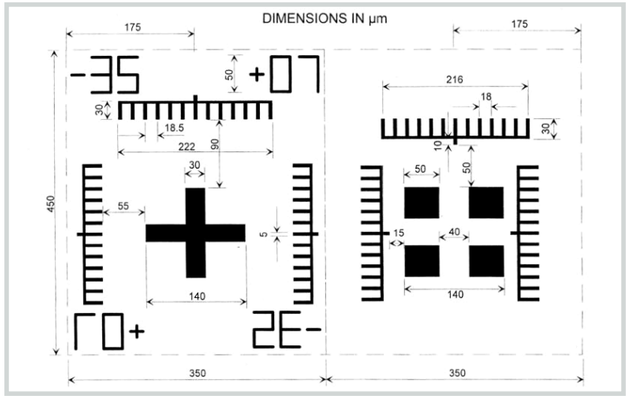

Figure 4:
Male and female alignment keys with graduate xand y- axis scales.

ALIGNMENT TECHNIQUES

Alignment techniques are separated in to methods which align to live target images and those that use stored image alignment. During live image alignment the image of both the device and the cap wafer alignment keys are viewed simultaneously. This has the advantage that throughout the alignment process any shifts that might occur because of vibration, clamping or other mechanical motions can be observed and corrected. With stored images once the position of the initial fiducial is found and captured (digitally stored to memory) the wafer is clamped into position and presumed to be stationary during all remaining teps. However, this can not be verified since the target image is no longer in the field of view.

The options for alignment techniques include BSA (backside alignment) with transparent substrates, BSA with opaque substrates, IR (infrared) alignment, and ISA (intersubstrate) alignment. Figure 3 is a schematic of the objective and substrate locations for each technique. The BAS w/ transparent substrates and the IR method align to live images. ISA also aligns to a live image however, after bonding the microscopes can not access the interface again and are not useful for post bond analysis. The BSA method can be used to verify the post bond alignment accuracy because it is possible to "look through" the transparent substrate at any time during the align and bond process. This is also true for the IR method whenever the metal layers do not obscure the field of view of the target and the wafers have a resistivity greater than 0.01 Ohm-cm (for silicon).

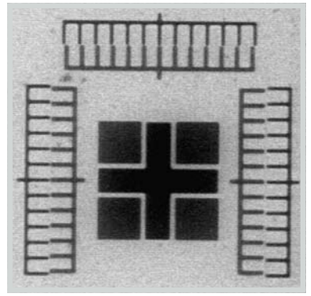

Figure 5:
Post bond IR image of male and female alignment keys in bonded silicon wafers.

Total Steps (14)	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Top Temp (°C)	40.0	40.0	40.0	40.0	40.0	40.0	220	220	300	300	90.0	40.0	40.0	40.0
Bottom Temp (°C)	40.0	40.0	40.0	40.0	40.0	40.0	220	220	300	300	90.0	40.0	40.0	40.0
Chamber Press (mBar)	1000	1.00E-3	1500	1500	1500	1500	1500	1500	1500	1500	1500	1500	1000	1000
Tool Press (mBar)	0	0	0	0	0	0	0	0	5000	5000	5000	5000	0	0
Voltage (V)	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Log Data (Seconds)	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Wait								03:00 DWELL		10:00 DWELL				
AlarmTime	00:30	00:30	00:30	00:30	00:30	00:30	01:00	00:30	00:30	00:30	03:00	03:30	01:30	01:30
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Figure 6:
Recipe for Au-Sn eutectic bonding.

ALIGNMENT TARGETS

Alignment targets play an important role in achieving good quality bond alignment. In addition some target designs also facilitate process control and monitoring, For example, the alignment key shown in figure 4 contains both a standard cross and box style alignment key as well as graduated scales along the x- and y-axes. During process development the scales can be used to accurately determine systematic shifts and rotation that may occur during the alignment or bonding steps. Note that the graduated scales are used for analysis and not used for alignment. The standard male and female keys are used by the operator or the image recognition system for overlay alignment.

Figure 5 shows an image of one of the keys after bonding. In this example the x-axis is perfectly aligned and the center of the graduated scales is aligned. On the y-axis verniers the pattern is shifted slightly upwards and the first hash mark is aligned. If this were a 0.5 µm vernier then the measurement would imply that at most the misalignment in this example is +/-0 µm in x and +0.5 µm in y. Verniers can be scaled to give 0.1, 0.2 or 0.5µm resolution depending upon the desired precision needed.

BONDING TECHNIQUES AND KNOW-HOW

Bonding of eutectic alloys requires good control over the temperature and pressure profiles in the bonder. This is directly related to the melting of the alloy. The viscosity of the alloy is related to the temperature. As the melt becomes hotter the molten metal is more fluid. With increased fluidity come the propensity of the wafers to slide relative to one another and loose alignment accuracy.

Another reason that temperature control is essential involves ensuring that all the locations on the wafer are melted. Many MEMS structures are fragile and care must be taken that when the applied force is used the interface is soft and fluid. If any areas contain solid metal this will not be flattened by the applied force and the stress may damage underlying or surrounding structures.

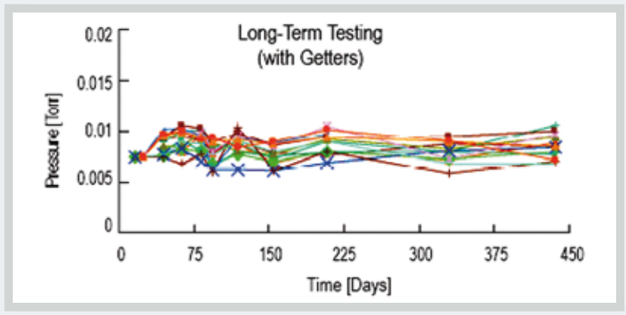


Figure 7:
Hermeticity results from 14 Au-Si eutectic sealed devices from reference 5 and 6.

Equally important is the uniformity of the applied force and the parallelism of the bond chucks to the surface of the wafers. If the force is not applied directly perpendicular to the interface the molten alloy will squeeze into unwanted areas and distortion of the bond lines will result. In extreme cases the molten alloy can be extruded in to the cavity or die structure and prevent device functionality.

In many applications the parts that are being bonded have cavities. To ensure that the cavities are filled with the proper atmosphere, separation flags or spacers are used to maintain a gap between upper and lower substrates. Spacers are thin shims of metal that are placed between the wafers at three locations.

The spacers range from 50-100 µm in thickness and only penetrate the outer most 2-3mm of the wafer perimeters. The spacers allow gases to be purged to and from the cavities throughout the interface via the vacuum pump system in the bonder. Once the proper atmosphere is established within the cavities, the spacers must be removed prior to bringing the wafers in contact for final annealing. Removal of spacers has been identified as a source of mechanical motion that can lead to shifting of the substrates.

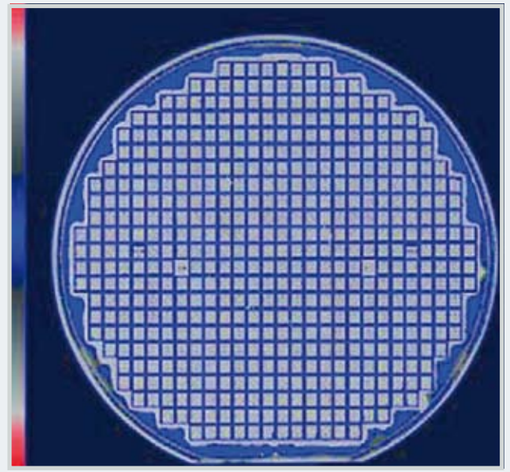
Early generation bonders used an all at once removal methodology to retract the spacers. This was accomplished by using a center pin to come down from the upper pressure plate and press the wafers together in the center. This fixed the position of wafers together in the center only. Then the clamps were lifted and the flags pulled out one at a time from the wafer edge. Later generation equipment enabled the flags to be pulled one at a time, however a fundamental problem still existed; if the wafer stack is pinned only in the center it is still free to rotate about the z-axis.

In addition many times the center pin causes harm to delicate dice in the center of the wafer. The solution is new control software that allows for only one clamp to be lifted leaving the other two clamps available to confine the wafers in two locations along the edge of the wafer stack. After the first clamp is lifted the spacer is removed and the clamp is put back down on the stack. Then the next clamp location is released still leaving two locations pinned in position. This improved flag retraction method has been shown to reduce shifting by seven times.[4] This method, called sequential clamp removal is only possible when there are at least three clamp mechanisms on the bond fixture.

The bond recipe itself will resemble the example shown in figure 6. There may be some pump and purge cycles in the initial stages of the recipe to exchange the atmosphere inside the bond chamber with one that is typically inert or reducing. Forming gas, hydrogen mixed with either nitrogen, argon or helium has been shown to dramatically improve yield by suppressing oxidation and metal film contamination. The atmosphere also aids in heat transfer and is preferred to vacuum annealing unless the device requires vacuum sealing.

The temperature as well as the force should be ramped in a controlled fashion. Force is used to establish physical contract between the surfaces. By gradually applying the force the metal will flow between the wafers and remain confined to the pattern seal ring area.

The reaction time is generally short for eutectic bonds when the reaction is driven from melting an alloy layer. When the diffusion reaction is used the recipe may be lengthened by several minutes. Once the material is in the liquid state only a few minutes are required to equilibrate the composition and reflow the interface. Cooling can be done as rapidly as stress conditions in the device or sample will allow.



APPLICATIONS AND RESULTS

Eutectic bonds are used for a variety of inertia devices such as accelerometers, gyroscopes, and applications such as RF switches and resonators. A recent publication presented a lengthy study of Au-Si eutectic bonded pressure sensors.[5,6] It is rare to find published hermeticity data and these tests used encapsulated pirani gauges within the device to monitor the leak rates of the seals over more than one year. The study included several eutectic alloys and data in Figure 7 is for a diffused Au-Si eutectic bond showing excellent results.

Several examples of successfully bonded wafers are shown in figure 8-11. Figure 8 shows an example of a Au-Si eutectic bond on 6" MEMS wafers. This particular example was driven from a diffusion reaction and Sonoscan acoustic imaging found no voids within the seal ring area. The blue in this figure indicates a void free bond line.

Figure 8:
Sonoscan image of 6" wafers bonded using Au-Si diffusion based Eutectic bonds.

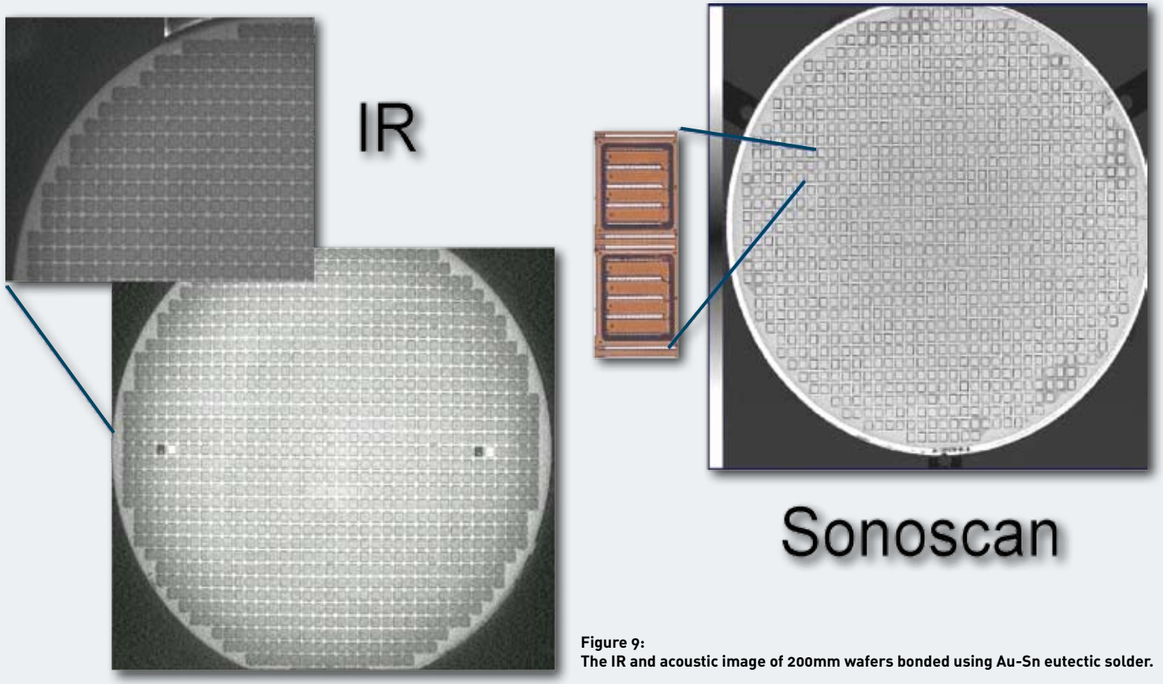


Figure 9:
The IR and acoustic image of 200mm wafers bonded using Au-Sn eutectic solder.

Another feature to point out is that the edge of the wafer is sealed. This is very important if acoustic imaging is used for void detection because when the edges of the wafer are not sealed, capillary action will draw fluid into the areas between the die and complicated post bond process flows.

Gold tin eutectics have been the most requested alloy system in the demo facilities of Suss MicroTec. Shown in figure 9 is an example of the IR and Sonoscan acoustic image of the bonded 200mm wafers. The dice were uniformly bonded at all locations within the wafer.

The gold tin system has also been used on ceramic packages as shown in Figure 11. Due to the surface waviness of the ceramic substrate the conformal nature of a eutectic sealing technology was a desired benefit of this bond method.

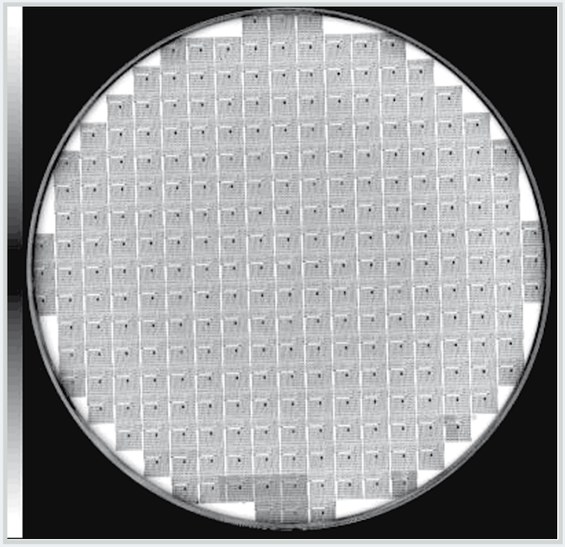


Figure 10:
Au to SiGe eutectic bond on 200mm silicon wafer. Acoustic image shows no voids or unbonded areas.

The last example is a Au to SiGe eutectic bond. Whenever a eutectic forms between two binary phases it will be possible to form a ternary eutectic phase as well if the remaining binary system also has complete solubility or exhibits a eutectic reaction. In the case of Au a simple eutectic exists between Au-Si at 363C and 2.65wt% Si and between Au-Ge at 419C and 28 at%Ge. Meanwhile, Si and Ge are completely miscible. In figure 11 we show a 200mm wafer bonded by eutectic alloy formation between Au and a SiGe alloy layer on silicon substrates. This process was completed at 420C.

Because eutectic alloys melt and are therefore, self planarizing there is no need to CMP (chemical mechanical polishing) the metal layers. The wetting behavior of the alloy to its adhesion layer will assist with confinement of the molten flow as long as the force is applied gradually. This eliminates one of the costly processes normally associated with metal bonds.

CONCLUSIONS

Eutectic alloy bonding is widely used in advanced packaging and MEMS device fabrication for hermetic seals. The processing temperatures of the various alloy choices are below 400C (except the Au-Ge system) and the selfplanarization of the molten metal make this type of bond a very surface topography tolerant method. Alignment methods can include IR, intersubstrate alignment, or backside alignment. The accuracy of the aligned features depends on the choice of alignment method, quality of the targets and thickness of the alloy layer. However, for metal layers 1µm thick or less alignment accuracies of ~2 µm can be expected.

It is expected that eutectic alloys will gradually replace some of the glass frit sealing technologies in applications that require device scaling to smaller packages and for integrated devices. The methods and materials systems described here should give some insight into what the possibilities can include.

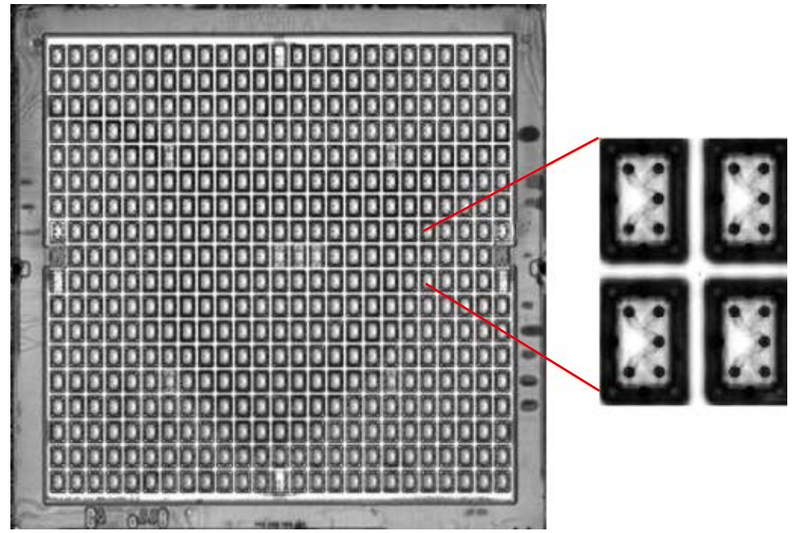


Figure 11:
Ceramic packaging using Au-Sn eutectic bonds

DR. SHARI FARRENS
is the inventor of plasma activated substrate bonding and holds several patents for this enabling technology. Dr. Farrens has authored and co-authored over 100 publications on SOI, wafer bonding and nano-technology. With over 15 years of hands-on, worldwide experience in academia and industry she is considered an expert on MEMS and wafer to wafer bonding technologies.

SUMANT SOOD
is the Senior Applications Engineer for Wafer Bonders at SUSS Microtec Inc.. His recent experience includes development of plasma enhanced wafer bonding processes for SOI and strained silicon on Insulator (sSOI) applications. Sumant has authored and co-authored more than 15 papers in wafer bonding, SOI, strained silicon and related areas. He received his B.Tech in Electrical Engineering from Punjab Technical University, India and MS in Microelectronics from University of Central Florida.

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