METAL BASED WAFER LEVEL PACKAGING

Shari Farrens, Ph.D.
SUSS MicroTec
Waterbury Center, VT, USA
sfarrens@suss.com

ABSTRACT
Metal based wafer bonding for WLP has several advantages including enhanced hermeticity and it facilitates vertical integration. These advantages allow for reduction in die size and cost savings with improved device performance. Until recently, first level packaging for MEMS was done using glass frit or anodic bond process. The glass based bonding methods are used in over 80% of volume MEMS production for high volume products such as pressure sensors, accelerometers and gyroscopes. All of these products as well as RF resonators require vacuum packaging. The physical properties of glass and frit sealing materials translate into seal geometries that are in the range of 100's of microns.

Using advanced bonding and bond alignment equipment, in combination with metal bonding methods significant improvements in COO and device performance can be realized.

INTRODUCTION
The permeability rate of a material is a rate at which gas atoms diffuse through a material. Permeation rates can be compared for materials of equal thickness and under standardized atmospheres. Figure 1 shows this type of analysis for a generalized category of sealing materials; polymers, glass, and metals. By definition materials with less than 1 day of sealing capacity (1e-14 gm/cm-s-Torr) are considered Non-Hermetic as indicated by the red line.[1] If a comparison is made between the glass seal and a metal seal both 10µm thick the lifetime of the seal is a few years versus a century or more. The metal seals used for MEMS packaging have seal geometries of 1-2µm and could conceivably be reduced to less than 1µm if mechanical integrity (strength) could be ensured.

The combination of improved hermeticity and smaller seal rings enables significant die size reduction. With reduced die size the number of die per wafer increases as does the yield, all contributing to cost reductions. Table 1 compares the area savings when the sealing geometry is reduced. The table assumes a constant dicing street size of 75 microns. Using this type of analysis, a 9mm^2 die that was formerly sealed by a glass-based technology, can be replaced with a 2-3um wide metal seal and several hundred more die can be placed on the same sized wafer.

The two types of metal seals available for wafer level bonding are diffusion based methods and eutectic methods. Both of these fabrication methods have numerous benefits and can be successful replacements for tradition packaging techniques.

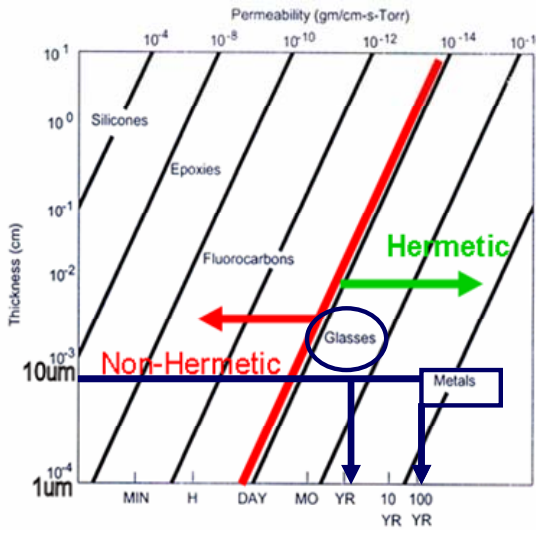

Figure 1. The Permeability of materials as a function of the thickness of the material. Highlighted arrows compare metal and glass lifetimes.

Table 1. Comparison of effective die size and number of additional die added when seal geometry area is reduced.

Die Size (mm x mm)	3	5	7	10
Effective Die Area w/ 50 um Seals	10.1	26.8	51.5	103.5
Effective Die Area w/ 25 um Seals	9.8	26.3	50.8	102.5
Effective Die Area w/ 10 um Seals	9.6	26.0	50.3	101.9

Max Added Die/wfr (100um > 50um)	187	44	17	6
Max Added Die/wfr (50um > 25um)	101	23	9	3
Max Added Die/wfr (25um > 10um)	63	14	5	2

DIFFUSION BONDING
Diffusion bonding when two metals are pressed together under applied force and heat which enables atoms to migrate from lattice site to lattice site "stitching" the interface together. Diffusion processes require intimate contact between the surfaces since the atoms move by lattice vibration. Generally speaking softer metals such as copper

or aluminum are excellent choices for diffusion bonding due to their ductile properties and rapid diffusion rates. Gold is another excellent candidate and can be used at lower temperatures than the other options.

Diffusion rates vary dramatically depending upon the reaction path. Surface diffusion is diffusion along the terraces of a surface. Since there are no atomically flat surfaces on MEMS wafers the atoms will move from surface site to surface site to reduce the terracing and free energy. This is the most rapid diffusion process since the atomic motion occurs relatively unimpeded.

Grain boundary diffusion is next most rapid reaction pathway. Since most deposited layers are polycrystalline there are numerous boundaries between the grains in which 1:1 atomic lattice matching is incomplete. This leave empty space in which the atoms can migrate freely.

Diffusion through the bulk of the crystal is the slowest of the three mechanisms. Exchange of atoms or vacancies within the lattice enables the mixing to occur. The onset of bulk diffusion is typically ⅓ to ½ of the melting point of the material and increases exponentially with temperature in a Arrhenius relation.[2] However, oxidation and impurities in the metal films also play a significant role in diffusion reactions and generally reduce the diffusion rates significantly. Thus manufacturing techniques need to include clean deposition practices and bonding using surface oxide removal and re-oxidation prevention are recommended.

Table 2 give the recommended processing ranges for the three leading metal diffusion bonding techniques. Aluminum bonding is generally not pure aluminum but rather the metallization alloy used in the fab which includes up to 4% Cu or other binary additions. Both aluminum and copper bonding require temperatures above 400C to achieve a good hermetically seal interface. Aluminum also requires a large applied force which is apparently needed to crack the surface oxide which spontaneously forms on any aluminum surface. The surface oxide of aluminum is not soluble in the matrix (<2e-8 wt%) and tracer studies have proven that aluminum does not penetrate the oxide.[3,4] Rather, oxygen from the surface diffuses through the Al_2O_3 layer to provide the source of addition oxidation until the surface is fully passivated. However, the surface oxide can be cracked and bonding can be completed by using a high applied force.

Gold diffusion is the lowest temperature process of the three and is successfully managed at temperatures as low as 380°C. Unlike copper and aluminum gold does not readily form an oxide and under normal processing conditions it is not necessary to use surface cleaning prior to bonding.

Table 2. Typical processing parameters for metal diffusion bonding.

Metal	Temperature	Applied Force Range†	Time	Atmo-sphere
Al	400-450°C	>70KN	20-45 min	Vac or H_2/N_2
Au	350-450°C	>40KN	20-45 min	Vac or H_2/N_2
Cu	380-450°C	>30KN	20-60 min	Vac or H_2/N_2

†Applied force depends on wafer diameter and pattern density. Table values are representative of 200mm wafers.

Copper on the other hand, readily forms a surface oxide. The oxide can be successfully removed and the surface passivated by the use of formic acid vapor cleaning. Vapor cleaning with formic acid is used in 3D vertical integration to ensure high conductivity of interconnects.[5] The vapor cleaning is demonstrated in figure 2. A patterned copper wafer was exposed to elevated temperatures with and with out the formic acid cleaning. The cleaned wafers were able to withstand post cleaning exposures to high temperature in the bonder and subsequently showed improved electrical performance.

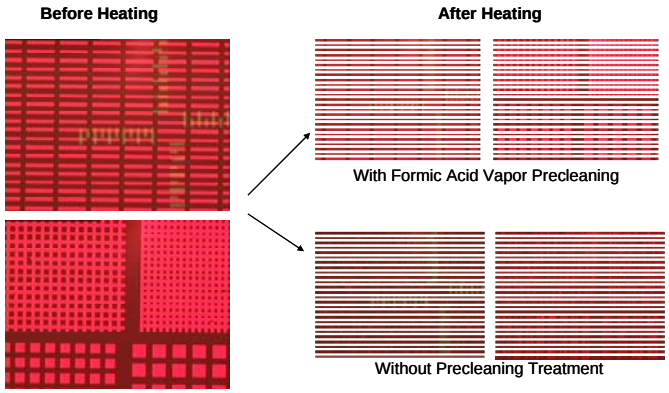

Figure 2. Images on the right are the wafer as-received. The wafer was then heated in a bonding chamber to 450°C for 30 minutes. Right upper images were cleaned with formic acid cleaning prior to heating and the right lower wafer was not cleaned.

EUTECTIC BONDING

The other major category of metal based bonding used in MEMS packaging is the eutectic bond. A eutectic alloy is sometimes called a "solder" however, this is not necessary the correct metallurgical term. A eutectic alloy is a two component alloy that undergoes a direct solid to liquid phase temperature at a specific composition and temperature.

Table 3. Eutectic alloy commonly used in MEMS wafer level packaging.

Eutectic Alloy	Eutectic Composition	Eutectic Temp.
Al-Ge	49/51 wt%	419ºC
Au-Ge	28/72 wt%	361ºC
Au-In	0.6/99.4 wt%	156ºC
Au-Si	97.1/2.9 wt%	363ºC
Au-Sn	80/20 wt%	280ºC
Cu-Sn	5/95 wt%	231ºC

The composition and temperature define the reaction and are unique to only a few materials systems. Table 3 shows the alloys most often used for wafer level bonding. The choices are alloys of gold, aluminum or copper since these materials are already used in semiconductor fabrication labs and in most cases have established processing and deposition methods. The most common choice is the gold-tin system with interest in other alloys fairly evenly distributed.

Choosing the correct eutectic alloy for an application is most often determined by the processing temperature and compatibility of the materials with the existing manufacturing flow. In addition to alloy selection it is equally important to determine the method of eutectic alloy formation.

Eutectic alloys have several advantages over the diffusion processes which include lower processing temperatures and reflow. The reflow process enables the interface to self-planarize and minimize the effects of surface topography or less than ideal CMP (chemical mechanical polishing) steps. However the reflow must be controlled through proper thermal and force application in the bonder.

Figure 3 is the Al-Ge phase diagram.[6] This is a simple eutectic phase diagram with no intermetallic phase formation. The aluminum has a melting point of 660°C and germanium melts at 938°C. The eutectic reaction is at 51.6 wt% Ge and has a solid to liquid transition (eutectic point) at 420°C. In most eutectic bonding applications the rule of thumb is to remain at 7-15°C above the eutectic temperature. Going to higher temperatures will increase the fluidity of the alloy and can lead to excess flow into unwanted regions in the die. However, if the temperature is not uniform the viscosity of the melt will vary. Some areas on the wafer may be solid and others liquid and the wafers will crack under the applied force as bending moments develop in regions with varying compliance.

The next decision that must be made for a eutectic bond is whether or not the bond will be done by melting the alloy or by a combination of diffusing pure materials together in the solid state to reach the eutectic composition and then melting the alloy. In case the alloy, for example 51.6 wt%

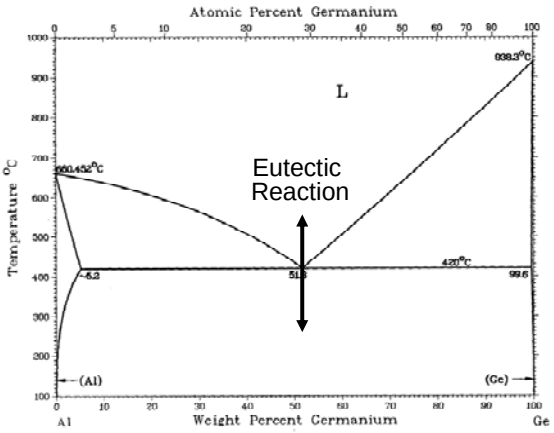

Figure 3. Aluminum – germanium phase diagram showing simple eutectic reaction at 56.1wt% Ge and at 420°C.

Ge, can be deposited as an alloy layer on both sides of the interface then the wafers are simply aligned, brought into a contact and pressed together. After contact is established the wafers are heated to the eutectic temperature, melted and re-solidified. Alloys can be deposited by sputtering of alloy targets or electroplated in some but not necessarily all cases. The advantage of the direct melting of alloy layers is speed because the diffusion step can be avoided.

Alternatively the aluminum can be deposited on one wafer and the germanium on the other substrate. Then the wafers are pressed together and heated (below 420°C) until the interface mixes. Note that limited solid solubility means that the diffusion is only a few percent and grain boundary reactions will play a major role in the success or failure of the bonds when completed with this strategy. After mixing the material the wafers are reflowed and cooled.

After eutectic bonds are cooled there is a possibility that microvoids form in the eutectic microstructure. These voids may be due to the Kirkendall effect which occurs when one element diffuses more quickly than the other and the lattice sites left behind are empty.[7] Or rather then are filled with vacancies. If a substantial vacancy concentration exists then the vacancies can cluster and lead to microvoiding. In most cases this can be overcome by adjusting the cooling rates and the amount of hyper eutectic heating.

ALIGNMENT

Alignment accuracy is affected by the quality of the alignment keys, the method of imaging used during wafer to wafer alignment and the thermal response of the wafers during heating and bonding. There are three primary alignment methods used for metal bonding. These are BSA (backside alignment), ISA (inter-substrate face-to-face alignment), and IR (infrared) alignment. In general metal bonding provides a huge benefit over other types of bonds whenever the fiducials can be defined with the metal layers. The sharp contrast between the metal and semiconducting layers provides excellent human or automated image resolution.

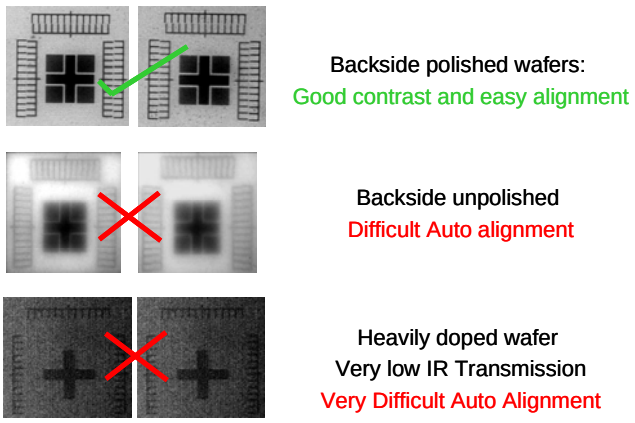

Figure 4. Image degradation from sample effects.

Backside polished wafers are recommended for BSA alignment and usually required for IR alignment. IR alignment has the additional advantage that for samples that are IR transparent (resistivity levels >0.01 Ohm-cm) and have a low density of metal surrounding the alignment keys the IR imaging method can be used for post bond overlay accuracy assessment and inline metrology during full automated production.[8] Figure 4 shows the degradation that occurs in IR imaging when the wafers are too highly doped or do not have a polished backside on at least one of the wafers.

Alignment key recommendations exist for all the types of imaging conditions. In addition it is very useful to consider the use of verniers in the alignment key as a method of quantifying lot to lot variations. Figure 5 shows an alignment key with graduated lines used to assess the post bond alignment shifts. Fast, calibrated assessments of final overlay accuracy allow for rapid feedback and process development improvements.

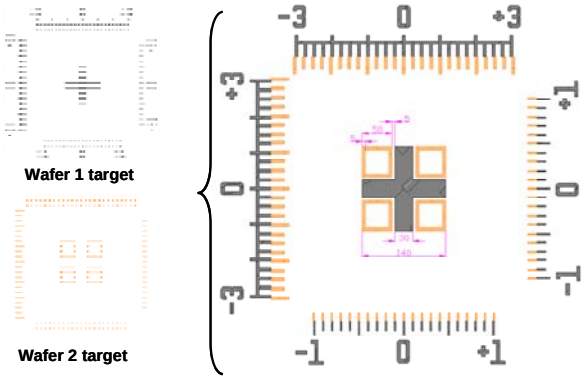

Figure 5. Suggested male and female targets for IR or ISA alignment. Note dual scale verniers provide either 0.25µm or 0.1µm resolution.

One of the key benefits of post bond alignment checks are that the alignment can be checked for each wafer pair. Thus when production tools are running unattended the cluster tool can make use of the rapid speed of the alignment module relative to the rate at which the bonder can complete a full metal bond thermal treatment with atmospheric controls. The master recipe or path is defined such that when the bonds are completed in the bond module the wafers can return to the aligner and a post overlay image is taken. If the accuracy is within the tolerances set by the recipe then the bond chamber is loaded with the next aligned pair. If the accuracy is not within specification the operator is notified to remedy the situation. The frequency of the checks can be selected to match the product necessities.

Both metal diffusion and metal eutectic bonds are capable of achieving <5µm post bond alignment accuracy. The metal diffusion bonds are affected by thermal expansion difference between top and bottom wafers if the upper and lower heat sources are not consistent with one another. In eutectic bonding the major contributor to post bond alignment accuracy is the shifting that may occur if the applied force or other mechanical systems in the bonder do not prevent the two wafers from sliding on the liquid interface. Currently metal diffusion bonding with Cu has be proven as a 1-2µm process with ability to achieve <1µm alignment accuracy in well defined 3D integration applications. MEMS bonding with eutectic bonds are usually a 2-3µm process.

EQUIPMENT

The sensitivity of the metal bonds to uniform temperature and force applications has led to improvements in wafer level bonding equipment. Improvements in materials and design have led to bonders such as the SUSS MicroTec CB8 (or CB200 and CB300 in 200mm and 300mm cluster tools) and have led to temperature uniformity levels with <1% difference within wafer or between upper and lower heaters. The force uniformity in advanced bonders is now 5% and results from the fact that in these bonders the upper and lower pressure plates establish parallelism by a WEC (wedge error compensation) operation before bonding begins. During the WEC operation the lower bond head assembly is floated on a bed on N2 air and allowed to rotate on a spherical bearing. This eliminates any non-parallelism between upper and lower plates and ensures the applied force is perpendicular to the bond interface at all locations.

A study was performed in which a glass wafer and a silicon wafer were bonded using eutectic alloy balls.[9] The balls were placed between the two substrates and put into the bonder. Several parameters were explored including the effect of overheating and non-planar force application.

When the temperature is too high above the eutectic the alloys has a very low viscosity and flows readily with even the lightest application of force. This can lead to the formation of bubbles at the interface and areas with

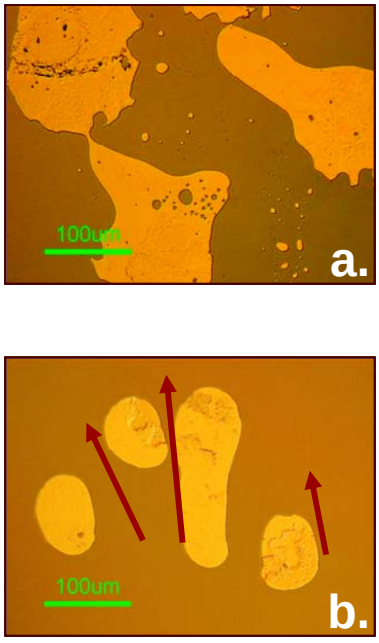

Figure 6. a) Bubbles formed in the eutectic alloy due to overheating; **b)** smearing of the eutectic alloy in the direction of non-parallel force application.

unwanted metal. Figure 6a is an optical micrograph looking through the upper glass substrate. The unconfined flow is clearly visible and there are numerous bubbles. In figure 6b the flow direction is very obvious and this is a tip off that the bond heads were not parallel to one another as the contact was made.

RESULTS

Gold to gold bonding is the lower temperature diffusion bonding method of the three options discussed above. Table 4 is the post bond alignment accuracy of several wafers aligned with face-to-face ISA alignment on the SUSS MicroTec BA200+ aligner. The wafers were subsequently bonded on the SUSS MicroTec CB8 shown in figure 7, and measured independently on a free standing IR microscope. The average overlay accuracy of all wafers measured in three locations each, was +0.89 µm in x and -1.03µm in y overlay accuracy.

Table 4. Au to Au alignment accuracy, post bond.

	Alginment Shift X-axis and Y-axis in Three Locations							
	X1	Y1	X2	Y2	X3	Y3	X misalign (µm)	Y misalign (µm)
	-0.03	0.02	-0.08	0.07	-0.10	0.10	1.25	-1.85
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.80	-0.90
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.50	-1.75
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.95	-1.05
	-0.03	0.02	-0.08	0.07	-0.10	0.10	1.70	-2.15
	-0.03	0.02	-0.08	0.07	-0.10	0.10	1.85	-2.40
	-0.03	0.03	-0.08	0.08	-0.10	0.10	1.60	2.25
	-0.02	0.03	-0.07	0.07	-0.10	0.10	-1.20	0.30
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.55	-1.75
Average	**-0.03**	**0.02**	**-0.08**	**0.07**	**-0.10**	**0.10**	**0.89**	**-1.03**

Table 5. Cu to Cu diffusion bonding, post bond alignment results.

Sample #	POST BOND ALIGNMENT DATA				
	LX	LY	RX	RY	ACC POST
1.0	-3.0	0.0	-1.5	0.0	**2.3**
2.0	-0.5	-2.0	0.0	2.0	**2.0**
3.0	-3.5	-0.5	1.5	0.0	**1.1**
4.0	0.0	0.5	0.0	0.5	**0.5**
5.0	-1.0	-1.0	-0.5	-1.0	**1.3**
6.0	-0.5	0.0	0.0	0.0	**0.3**
7.0	0.0	-2.0	-0.5	0.0	**2.0**
8.0	-0.5	-2.0	-0.5	2.0	**2.1**
9.0	0.0	0.0	-0.5	-2.0	**2.0**
10.0	0.0	-1.5	-0.5	0.0	**1.5**
Max	**0.0**	**0.5**	**1.5**	**2.0**	**2.3**
Min	**-3.5**	**-2.0**	**-1.5**	**-2.0**	**0.3**
Avg	**-0.9**	**-0.9**	**-0.3**	**0.2**	**1.5**
StDev	**1.3**	**1.0**	**0.8**	**1.2**	**0.7**

A similar analysis was done with a copper to copper bond on 200mm wafers. These wafers did not have backside polished surfaces and the IR alignment was compromised as a result. In addition the additional temperature, approximately 100°C would have increased the radial expansion of the wafer by over 50µm and would have exacerbated any upper and lower heater deviation. Nevertheless the data in table 5 shows that the post bond alignment accuracy for copper wafers bonded at 450°C was an average of 1.5µm microns well within needed requirements and specifications.

Figure 7. SUSS MicroTec CB8 wafer bonding with WEC (wedge error compensation) to ensure parallelism between pressure plates for all bonds.

Figure 8 shows an example of 150mm successful aluminum diffusion bonding. These wafers were also bonded in the SUSS MicroTec CB8 chamber using 80KN of force at ~400°C. Both the blanket layers of aluminum as well as the patterned device wafer structures were successfully bonded in a void free fashion.

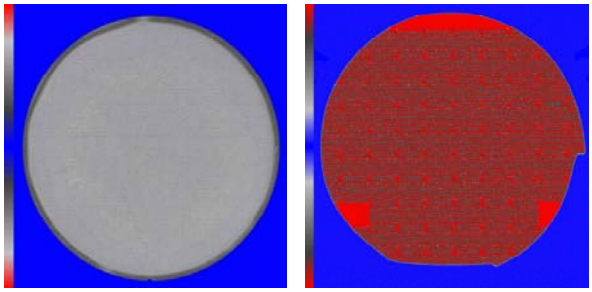

Figure 8. Left is a blanket layer of aluminum on a 200mm wafer successfully bonding with Al diffusion techniques. On the right is a 150mm device wafer also bonded with aligned Al to Al diffusion methods.

The eutectic bonds are used in a variety of applications. The lower temperature processes make these bonds appealing to optical markets such as LED's. The LED device is grown by epitaxial methods on lattice matched substrates such as InP, GaAs or Sapphire. The growth substrates are generally removed to access the backside of the device and improve output efficiency and brightness. Bonding is used to attach the LED structure to a lower cost substrate such as silicon and the growth substrate is removed by mechanical methods (grind an etch) or by laser lift off.[10] In all these process flows the thermal mismatch between the growth substrate and the silicon is extremely severe. This stress often cracks the epitaxial layers and ruins the device.

Figure 9 shows the results obtained using a AuSn eutectic alloy to bond silicon to sapphire at 290°C for 20 minutes. The bonds are void free and the wafers did not crack. The ability to reduce the processing temperatures minimized the time needed to heat and cool the bonder and the sample. The decreased sensitivity to thermal gradients (less CTE mismatch) also enabled faster cooling rates and improves the throughput and COO for this metallurgical choice.

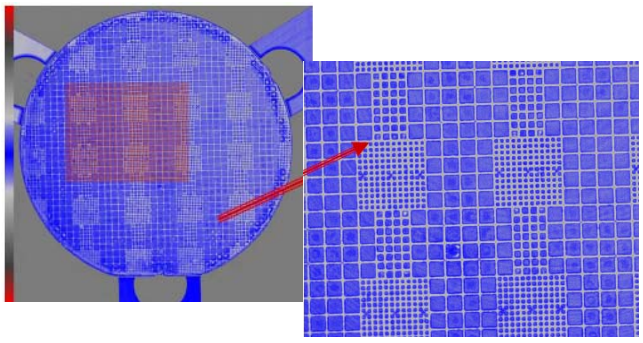

Figure 9. Au-Sn eutectic bond between silicon and sapphire. Gray areas are the seal rings in this Sonoscan acoustic image.

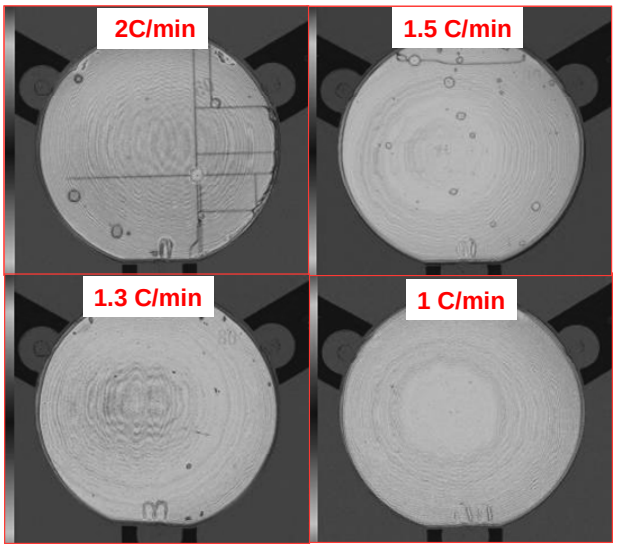

Figure 10. Gold diffusion bonding of Si to GaAs at 300°C for 1 hour. Cooling rate must be extremely slow to prevent the subsurface cracking shown in these acoustic images of the bulk GaAs substrate.[11,12]

This is in direct contrast to the results shown in figure 10 for a gold diffusion bond at 380C in which the cool down rates must be extremely slow in order to control the additional stress from the temperature difference between the two metallurgies and expansion differences between the substrate materials. In figure 10 one can truly see the difference that temperature and heating rate plays in thermal expansion induced stress. The CTE (coefficient of thermal expansion) for Si is 3.2 ppm compared to 5.32 ppm for GaAs and 8.4 ppm for sapphire. Thus the benefit of the lower temperature process for the AuSn eutectic compared to the Au-Au diffusion process allows the Si to sapphire to be successfully bonded even with the extreme (3.2 vs. 8.4ppm) CTE mismatch.

CONCLUSIONS

Several technologies based on metal bonding methods are available as replacements for glass frit or anodic bonding techniques. The metal bonds are categorized according to the type of metallurgical reactions that are used. These are the diffusion based processes and the eutectic reactions. The former does not involve reflow and generally requires a higher processing temperature and potentially longer cycle times. The eutectic process enables reflow similar to the glass frit processes and is more forgiving to surface roughness. The choice of eutectic alloys is large and processing temperatures range from slightly above 150°C to over 400°C. Thus it is possible to find a metallurgy that is compatible with materials requirements as well as post bond processing needs like solder packaging.

The key motivation for device manufacturers to transition to metal based wafer level bonding is the increased hermeticity which improves device functionality but more importantly enables the continued scaling of the device to smaller sizes.

In addition to device scaling the geometry of the sealing rings surrounding the device can be diminished further increasing the number of die per wafer. In closing it is worth noting that while the market growth of products such as accelerometers, gyros and RF MEMS is growing at more than 25% per year through 2011, the ASP (average selling price) is expected to drop by 8-13%.[13] Thus the analysis in table 1 is very poignant This table compared, through simple analysis, the number of additional die that can be placed on a wafer by switching from a large seal area typical of glass frit to a smaller metal seal. For example a 3mm x 3mm die size switching from a 100µm seal to a 10µm seal enables an additional 363 more die. This does not include any assumptions of die scaling or increases in yield which most companies are beginning to report.

Metal bonding is a valuable asset to MEMS wafer level packing. The economic and technological advantages are clear and these methods will continue to increase in use as market become more consumer oriented and integration with other components increases

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