Metal Based Wafer Bonding Techniques for Wafer Level Packaging

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Scope of the Practice

This BKP (Best Known Practice) describes the necessary conditions required to successfully utilize metal based wafer bonding techniques, including diffusion and eutectic bonding, for wafer level packaging.

Problem Statement and Goals of the Best Practice

Wafer level bonding utilizing metal based technologies are coming to the forefront of manufacturing methods in numerous 3D integration schemes and advanced MEMS processing. Copper to copper bonding of TSVs (through silicon vias) is used for 3D IC stacking of individual layers as well as in 3D packaging operations. A primary differentiator is the via size and therefore the placement accuracy needed to obtain production yields. Meanwhile gold and aluminum diffusion bonding and numerous eutectic alloys are replacing traditional MEMS glass based bonding methods and allow for higher degrees of hermeticity. The increased hermeticity enables device scaling and vertical packaging options that dramatically reduce production costs. This document describes the necessary conditions for these metal based bonding processes.

General Description of Approach/Strategy

Types of Metal Bonds:

There are two broad categories of wafer level bonds using metals. Diffusion bonds using copper to copper are very popular for 3D integration using TSV fabrication scenarios. In MEMS device packaging, gold and aluminum diffusion bonding methods are more common. The second category of metal bonding technologies includes a variety of metal alloying methods called eutectics. The eutectic is a specific alloy composition that changes directly from solid to liquid at a unique triple point in the phase diagram. The transition to a liquid phase provides a viscous interface that can self-planarize over surface topography and particles.

In many applications the metal bonds provide several advantages over other bonding methods. These include provisions for electrical interconnects, higher levels of hermeticity, and device scaling.

Alignment Strategies and Methods:

Alignment accuracy is affected by the quality of the alignment keys, the method of imaging used during wafer to wafer alignment and the thermal response of the wafers during heating and bonding. Alignment with metal bonding technologies is facilitated by the high levels of contrast that can be achieved with both optical and IR (infrared) imaging of metal fiducials on the semiconducting substrate materials. There are four fundamental types of alignment

used in wafer bonding. They are TSA, (top side alignment), BSA (bottom side alignment), IR (infrared alignment), and ISA (intersubstrate alignment or face-to-face). The positioning of the wafers with respect to the objectives is shown in Figure 1.

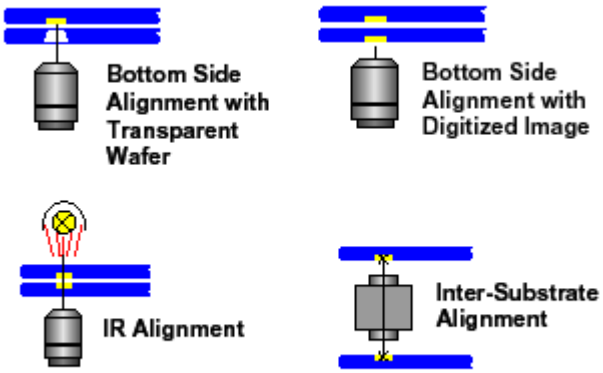

Figure 1. Four basic alignment methods used in wafer level bonding.

The BSA alignment methods have matured over several decades and are used extensively with anodic and glass frit bonding techniques. BSA alignment works equally well with all types of metal bonding assuming that one of the wafers includes backside targets that are clearly imaged on the polished or unpolished surface. Increased levels of overlay accuracy often benefit from more precise IR and ISA techniques. The IR or the ISA alignment methods both use alignment marks at the bond interface and therefore eliminate differences in focal plane depth and front to backside registration.

The advantage of IR imaging lies in the ability to observe both sets of alignment marks simultaneously and in principle maintain image information via live acquisition during the process of bringing the wafers into contact. Figure 2 shows the basic IR imaging concept. Limits to the IR method include double side polishing requirements on at least one of the wafers, limited dopant range, and metal free windows surrounding the fiducial locations. The backside polishing requirement is because light scattering from the backside roughness on standard wafers reduces the brightness and image quality of the alignment key at the camera.

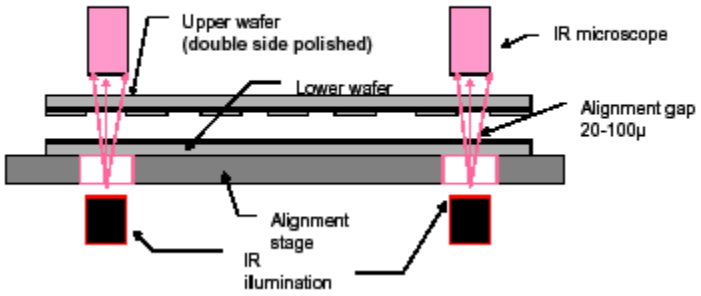

Figure 2. Schematic illustration of IR (Infrared alignment) process with bottom-side illumination.

IR absorption also limits the light reaching the imaging system. For silicon substrates, the substrate resistivity must be >0.01 Ohm-cm unless the wafers are sufficiently thin to ensure sufficient brightness. Naturally the area around the alignment keys must be metal free since the metal layers are 100% absorbing.

For samples in which the substrates are not transparent to IR radiation or backside polishing is not an option, face-to-face alignment is needed. Figure 3 shows an example in which the front side marks on both wafers are aligned using ISA mode by inserting a thin camera between the substrates and imaging the alignment keys. Once aligned, the camera is retracted and the wafers are contacted. This technique is popular with compound semiconductor substrates that are opaque to IR radiation, power devices built on highly doped substrates, or device wafers with extensive layers of metal that occlude IR transmission. Most 3D applications use intersubstrate alignment because metal layer obstruction is extensive in substrates with several thousands to millions of copper vias and multiple metal interconnect layers.

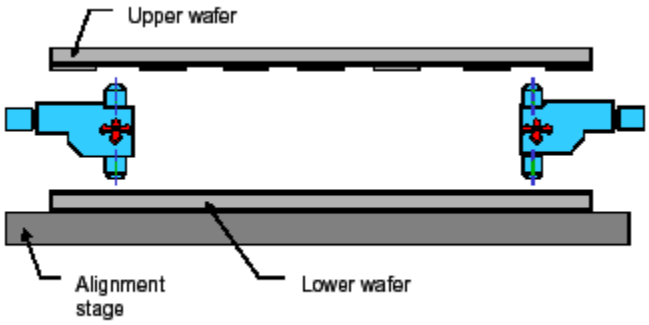

Figure 3. Schematic illustration of the ISA (inter-substrate alignment) configuration. ISA Alignment utilizes dual imaging objectives on both the left and right alignment optics.

The selection of the alignment keys is equally important and recommendations exist for each of the types of bonds and alignment methods discussed here. These are further subdivided depending upon if a human will be doing the alignment on manual systems or if an automated system is used with pattern recognition. Please refer to reference 1 for additional details.

Alignment Requirements:

Overlay/alignment accuracy is determined by several requirements. Most specifications arise from architectural design rules that will determine how accurately the upper wafers must align to the circuits or components on the lower wafer. Next are the requirements for dequate sealing and electrical connections. For a sealing ring surrounding the device it is often required that the width of the sealing ring align to within 80% of the opposing feature. This means only 20% of the width may misalign on either side. Thus, for a 100 micron wide sealing ring the offset on each side could be as much as 10 microns and the device and hermeticity needs would be satisfied.

Equipment:

The sensitivity of the metal bonds to uniform temperature and force has led to improvements in wafer level bonding equipment. Improvements in materials and design for bonders such as the SUSS MicroTec CB8 (or CB200 and CB300 in 200mm and 300mm cluster tools) and have led to temperature uniformity levels with <1% difference within wafer or between upper and lower heaters. The force uniformity in advanced bonders is now 5% and results from the fact that in these bonders the upper and lower pressure plates establish parallelism by a WEC (wedge error compensation) operation before bonding

Detailed Steps/Activities for Practice Implementation

Diffusion Bonding:

Diffusion bonding is when two metals are pressed together under applied force and heat causing atoms to migrate from lattice site to lattice site “stitching” the interface together. Diffusion processes require intimate contact between the surfaces since the atomic motion is driven by lattice vibration. Copper, gold, and aluminum are the most commonly used metals in 3D integration and MEMS packaging.

Table 1 compares the recommended processing ranges for the three leading metal diffusion bonding techniques. Aluminum bonding is generally not pure aluminum but rather the metallization alloys used in the fab which includes up to 4% Cu or other binary additions. Both

aluminum and copper bonding require temperatures above 400C to achieve a good hermetically sealed interface. Aluminum also requires a large applied force which is apparently needed to crack the surface oxide which spontaneously forms on any aluminum surface. The surface oxide of aluminum is not soluble in the matrix (<2e-8 wt%) and tracer studies have proven that aluminum does not penetrate the oxide.[2-3]

Gold diffusion is the lowest temperature process of the three metal diffusion choices and is successfully managed at temperatures as low as 300°C. Unlike copper and aluminum, gold does not readily form an oxide and under normal processing conditions it is not necessary to use surface cleaning prior to bonding. It is recommended that all metal bonds use either a vacuum bonding atmosphere or forming gas (H_2/N_2 for example) environment during the thermal cycles.

Metal	Temperature	Applied Force Range†	Time	Atmo-sphere
Al	400-450°C	>70KN	20-45 min	Vac or H_2/N_2
Au	300-450°C	>40KN	20-45 min	Vac or H_2/N_2
Cu	380-450°C	>30KN	20-60 min	Vac or H_2/N_2

Table 1. Typical processing parameters for metal diffusion bonding.

† Applied force depends on wafer diameter and pattern density. Table values are representative of 200mm blanket layer wafers.

Copper on the other hand, readily forms a surface oxide. The oxide can be successfully removed and the surface passivated by the use of formic acid vapor cleaning. Vapor cleaning with formic acid is used in 3D vertical integration to ensure high conductivity of interconnects.[4]

Eutectic Bonding:

The other major category of metal based bonding used in wafer level packaging is the eutectic bond. A eutectic alloy is sometimes called a “solder” however, this is not precisely the correct metallurgical term. A eutectic alloy is a two component alloy that undergoes a direct solid to liquid phase transition at a specific composition and temperature.

The composition and temperature define the reaction and this type of phase change is unique to only a few materials systems. ***Table 2*** shows the eutectic alloys most often used for wafer level bonding. The choices are alloys of gold, aluminum, or copper since these materials are already used in semiconductor fabrication labs and in most cases have established processing and

deposition methods. The most common choice is the gold/tin system with interest in other alloys fairly evenly distributed.

Eutectic Alloy	Eutectic Composition	Eutectic Temp.
Al-Ge	49/51 wt%	419°C
Au-Ge	28/72 wt%	361°C
Au-In	0.6/99.4 wt%	156°C
Au-Si	97.1/2.9 wt%	363°C
Au-Sn	80/20 wt%	280°C
Cu-Sn	5/95 wt%	231°C

Table 2. Eutectic alloys commonly used in Wafer level packaging.(WLP)

Choosing the correct eutectic alloy for an application is most often determined by the processing temperature and compatibility of the materials with the existing manufacturing flow. In addition to alloy selection, it is equally important to determine the method of eutectic alloy formation.

The eutectic bond can be achieved by melting the alloy or by a combination of diffusing pure materials together in the solid state to reach the eutectic composition and then melting the alloy.

When the alloy can be deposited as a compound layer on both sides of the interface, the wafers are simply aligned, brought into contact and pressed together. After contact is established the wafers are heated slightly above the eutectic temperature, melted, and re-solidified. Alloys can be deposited by sputtering of alloy targets and sometimes by dual component electroplating. The advantage of the direct melting of alloy layers is speed because the diffusion step can be avoided.

Alternatively, the pure materials that constitute the alloy can be deposited separately on each substrate. Then the wafers are pressed together and heated below the eutectic temperature until the interface mixes to form a solid solution layer via diffusion. Note that limited solid solubility means that the diffusion is typically only a few percent and grain boundary reactions will play a major role in the success or failure of the bonds when completed with this strategy. After mixing the material, the wafers are heated above the eutectic melting temperature under reduced force, reflowed, and cooled.

Results:

The three leading wafer level bonding techniques used in 3D integration are the fusion bond, copper to copper diffusion bonding and to a lesser extent the BCB bond. The fusion bond affords the highest potential for submicron alignment because the initial bonds are performed at room temperature in an aligner and tend to experience less thermal induced shifts when annealed in batch to create the permanent bonds. Table 3 shows an example of a fusion bond using IR alignment techniques that achieve deep submicron alignment accuracy.

Wafer #	Alignment in µm	Wafer #	Alignment in µm
1	0.1701	13	0.0484
2	0.0736	14	0.1008
3	0.1648	15	0.1326
4	0.0967	16	0.1898
5	0.1586	17	0.0793
6	0.0353	18	0.1195
7	0.1139	19	0.1088
8	0.0730	20	0.0725
9	0.0941	21	0.1280
10	0.0899	22	0.0951
11	0.1264	23	0.1258
12	0.0649	24	0.1165
Average	0.1088	Max	0.4385
St Dev	0.0428	Min	0.0190

Table 3. IR aligned fusion bond overlay accuracy.

Metal diffusion processes can make it more difficult to control thermal expansion differences between upper and lower wafers. Using precision alignment, quality fixtures, and state of the art bonding equipment, excellent alignment results can be obtained for 3D devices utilizing Cu-Cu TSV technology and also for Au-Au bonding of hermetically sealed MEMS devices. ***Tables 4 and 5*** show recent results of both types of metal diffusion bonds.

	Alignment Shift X-axis and Y-axis in Three Locations							
	X1	Y1	X2	Y2	X3	Y3	X misalign (µm)	Y misalign (µm)
	-0.03	0.02	-0.08	0.07	-0.10	0.10	1.25	-1.85
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.80	-0.90
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.50	-1.75
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.95	-1.05
	-0.03	0.02	-0.08	0.07	-0.10	0.10	1.70	-2.15
	-0.03	0.02	-0.08	0.07	-0.10	0.10	1.85	-2.40
	-0.03	0.03	-0.08	0.08	-0.10	0.10	1.60	2.25
	-0.02	0.03	-0.07	0.07	-0.10	0.10	-1.20	0.30
	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.55	-1.75
Average	-0.03	0.02	-0.08	0.07	-0.10	0.10	0.89	-1.03

Table 4 Post bond alignment accuracy. Average alignment shift ~1µm.

Sample #	POST BOND ALIGNMENT DATA				
	LX	LY	RX	RY	ACC POST
1.0	-3.0	0.0	-1.5	0.0	2.3
2.0	-0.5	-2.0	0.0	2.0	2.0
3.0	-3.5	-0.5	1.5	0.0	1.1
4.0	0.0	0.5	0.0	0.5	0.5
5.0	-1.0	-1.0	-0.5	-1.0	1.3
6.0	-0.5	0.0	0.0	0.0	0.3
7.0	0.0	-2.0	-0.5	0.0	2.0
8.0	-0.5	-2.0	-0.5	2.0	2.1
9.0	0.0	0.0	-0.5	-2.0	2.0
10.0	0.0	-1.5	-0.5	0.0	1.5
Max	0.0	0.5	1.5	2.0	2.3
Min	-3.5	-2.0	-1.5	-2.0	0.3
Avg	-0.9	-0.9	-0.3	0.2	1.5
StDev	1.3	1.0	0.8	1.2	0.7

Table 5. Copper to copper 200mm post bond alignment results using ISA alignment methods.

The newest technique to emerge from R&D to manufacturing are the aluminum based bonding methods for hermetic packaging. Shown in Figure 4 are examples of a 150mm MEMS wafer bonded with the aluminum diffusion process. Also shown is a 200mm wafer bonded with a blanket layer of aluminum resulting in a void free interface. Both bonds were done on the SUSS MicroTec CB8 advanced bonder.

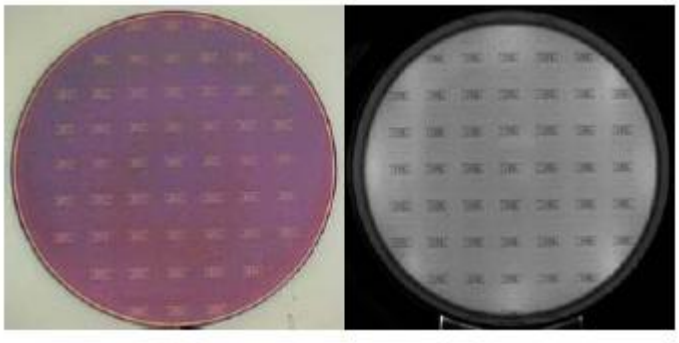

Figure 4. Optical image (left) and IR image of BCB bonded image sensor wafer. No voids visible.

Conclusion and Recommendations

Wafer level bonding has a long history in the production MEMS devices such as accelerometers, pressure sensors, and gyroscopes. As these products have matured, their scaled down cousins are entering consumer markets for gaming and mobile communications. Wafer level bonding with metal based technologies is meeting the demands of these products while presenting attractive cost models.

The utilization of metal bonds to realize vertically integrated devices and facilitate wafer level packaging with smaller form factors appears to be coming to market in 2009. Image sensors and stacked memory will test the manufacturability of these methods in production in the coming years. Successful implementation will drive further advancements in CPU and logic integration as well as heterogeneous integration. New state of the art alignment and bonding production equipment will be key to the success of these evolutionary advances in semiconductor processing.

Additional process are already evolving which combine techniques of advanced CMP (chemical, mechanical polishing) and bonding to realize Cu/Oxide, Cu/BCB and other hybridized bonding techniques. Like the microprocessor roadmaps, wafer bonding roadmaps continually seek to increase throughput and alignment accuracy while reducing production costs. This requires optimization of equipment, process flows, and materials science.

References and Supporting Documentation

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