Wafer Level Packaging:
Balancing Device Requirements and Materials Properties

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Abstract

Wafer level packaging for MEMS devices in the front end has a field proven history that now allows for these techniques to facilitate back end packaging and device integration. The most common methods for MEMS assembly include anodic and glass frit bonding which comprise more than 70-80% of all volume manufacturing processing today. However, metal based bonding schemes such as metal eutectics and metal diffusion seals provide increased hermeticity levels and facilitate inter-wafer and intra-device electrical connections. Adhesive bonds using a variety of materials types has been a long standing method for die to package assembly and over the past several years these techniques have been merged with metal techniques to enable wafer level 3D packaging.

At the same time that decisions are made regarding the choice of bonding methods it is necessary to consider the upstream and downstream processing. Integral to the success of the total packaging flow is balancing the thermal expansion issues of the various layers and substrates to minimize wafer bow and device stress. Understanding alignment requirements, hermeticity, and environmental requirements of the device must be met with the appropriate bond process flow.

Key words: wafer bonding, WLP, eutectic bonding, diffusion bonding, polymer bonding

Introduction

The first step in wafer bonding is wafer to wafer alignment. This is done using a bond aligner equipped with optics that uses visible or infrared illumination to image fiducials on each wafer. The type of bond, as well as the substrate and device materials, determines which alignment technique is best suited for the application.

Following the alignment step the wafers will be bonded in a thermal compression bonder. This chamber is able to control the ambient atmosphere, apply force and heat as necessary and for some bonding techniques it will also apply an electric field across the wafers.

Additional processing chambers are available for specialized bonding methods such as fusion bonding with plasma activation. Cleaning modules can also be quite helpful for surface preparation.

The decision tree starts with the device requirements evaluation which usually has to relate to cost and performance needs.

Performance Needs -Hermeticity

In all MEMS packaging operations there is an expectation of product lifetime and this is directly related to functionality of the device. MEMS device all have moving mechanical components and, at the very least, limited circuitry. These functions require specific environments and protection from corrosion, water vapor, and oxidation.

The permeability rate of a material is the rate at which gas atoms diffuse through a material. Permeation rates can be compared for materials of equal thickness and under standardized atmospheres. Figure 1 shows this type of analysis for a generalized category of sealing materials; polymers, glass, and metals. [1] By definition materials with less than 1 day of sealing capacity (10^{-14} gm/cm-s-Torr) are considered non-hermetic as indicated by the red line.

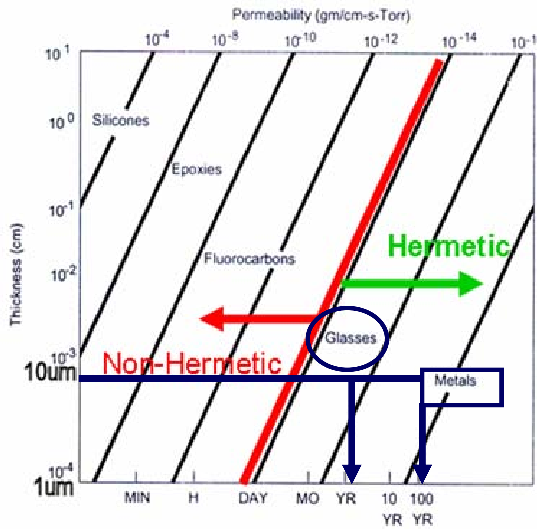

Figure 1. The Permeability of materials as a function of the thickness of the material. Highlighted arrows compare metal and glass lifetimes.

If a comparison is made between the glass seal and a metal seal both 10µm thick, the lifetime of the seal is a few years versus a century or more. The metal seals used for MEMS packaging have seal geometries of 1-2µm and could conceivably be reduced to less than 1µm if mechanical integrity (strength) could be ensured. Thus both glass and metal materials can create a hermetically sealed device but the geometries required will be different and this can dramatically affect the cost of the device.

Although considered “non-hermetic” the epoxy seals are adequate to keep out moisture (water molecules) but not single gas atoms regardless of the thickness of the seal ring. However, if the adhesive seal is over coated with metal, then the interface remains hermetic due to the permeability of the outermost layer.[2] This cost effect method uses an inexpensive polymer seal and then an unpatterned overcoat for hermetic sealing. Alternatively the metal overcoat may be patterned to facilitate connections to the metal redistribution layer.

Performance Needs -Thermal Expansion

Wafer bow is the curvature of the wafer and affects precision lithography steps and, in severe cases, leads to dislocation formation or fracture of the films and substrates. Upstream processes such as thermal oxidation, metal deposition and via filling all contribute to wafer bow. The primary cause of wafer curvature is the thermal expansion mismatch between materials deposited on the wafer. Table 1 gives all the parameters necessary to calculate simple wafer bowing.

The bonding method will determine a processing temperature necessary to complete the interfacial reaction. Thus, if a specific method is absolutely necessary then the only options that exist are to attempt to control the cooling rates or to start with one of the substrates thinner than the other and attempt to reduce the interfacial stress and resulting wafer bow.

Table 1. Materials Properties of Common MEMS Substrates and Thin Films

Material	Tm (melt)	Density	CTE	E (Young's)	ν Poissons Ratio
units	C	g/cm3	1.00E-06	Gpa	none
Si	1414.0	2.33	2.5(RT)-3.8(300C)	1.30	0.28
Ge	938.3	5.32	5.7-6.7	1.03	0.26
GaAs	1510.0	5.32	5.4-5.7	0.86	0.31
GaP	1750.0	4.13	5.3	1.03	0.31
GaN	1500.0	6.15	5.59	181.00	0.352
InP	1330.0	4.79	4.6	0.61	0.36
Sapphire	2040.0	3.98	8.4	344.73	0.29
Quartz		2.20	0.6	72.39	0.17
Pyrex-7740		2.20	3.3	63.00	0.2
Pyrex-7070		2.13	3.2	51.00	0.22
Borofloat 33		2.20	3.3	630.00	
Corning 7056		2.29	5.5	640.00	0.21
Cu	1084.9	8.93	16.8-18.9	0.12	0.36
Au	1064.4	19.28	14.2		0.44
Al	660.5	2.70	23.2-28.3	0.07	0.33
In	156.6	7.29	35.0		
Sn	232.0	7.29	25.0		

Figure 2 shows the theoretic values of wafer bow for fusion bonded GaAs to Si as a function of bonding temperature. The thickness of the GaAs substrate is varied and Si substrate thickness is fixed at 525µm. The model used here assumes the starting substrates are flat and ignores contributions from other device layers, structures and ramp rates. As shown, the lower the bonding temperature the lower the resulting bow. Thus it is an advantage to choose bonding methods which minimize the bond. When this is not possible some improvements can be made by altering the substrate thickness but this has not proven economical or viable in production.

Performance Needs - Alignment

Overlay/alignment accuracy is determined by several requirements. The most specifications arise from architectural design rules that will determine how accurately the upper wafers must align to the circuits or components on the lower wafer. Next are the requirements for adequate sealing and electrical connections. For a sealing ring surrounding the device it is required that the width of

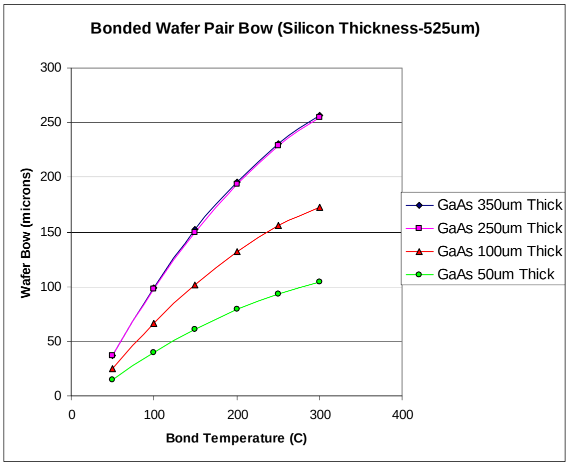

Figure 2. Wafer pair bow for a GaAs – Si bonded pair as a function of bonding temperature for several GaAs substrate thicknesses.

the sealing ring align to within 80% of the opposing feature. This means 20% of the width may misalign on either side. For a 100µm wide sealing ring the offset on each side could be at much as 10µm and the device and hermeticity needs would be satisfied.

The same type of analysis applies currently to through silicon via alignment for device stacking. Figure 3 shows the typical via size for CIS (CMOS image sensors) and memory device. These are currently the only devices being wafer level packaged using TSVs. As shown the requirements of alignment accuracy presently range for 5-9µm.

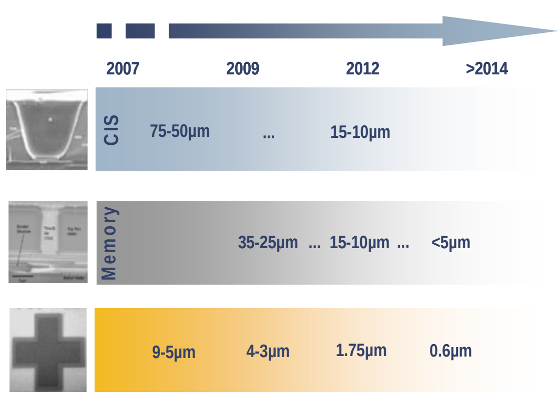

Figure 3. The CIS (CMOS Image Sensor) and Memory through silicon via (TSV) size roadmap from 2007 through 2014. The required alignment accuracy is on the last line.

Alignment Strategies

Alignment strategies build on the fundamentals from mask alignment lithography systems. Therefore it is well known that the quality of the alignment marks, separation distance (proximity versus contact), and mechanical positioning systems all contribute to final alignment accuracy. In order to discuss the various combinations it is first important to review the various alignment strategies.

There are four fundamental types of alignment used in wafer bonding. They are TSA, (top side alignment), BSA (bottom side alignment) IR (infrared alignment) and ISA (intersubstrate alignment or face-to-face). The positioning of the wafers with respect to the objectives are shown in figure 4.

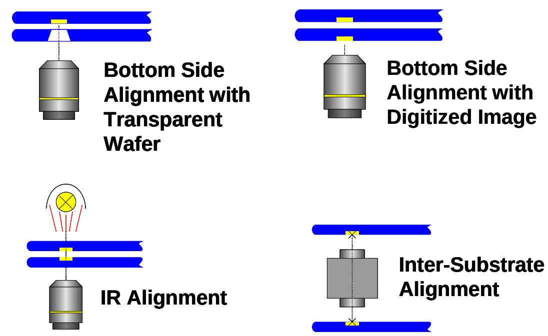

Figure 4. Four basic alignment methods used in wafer level bonding.

The BSA alignment methods have been around for several decades now and are used extensively with anodic and glass frit bonding techniques. Newer more advanced bonding requirements often require the IR or the ISA alignment methods and will be discussed in detail.

IR Alignment

The advantage of IR imaging lies in the ability to observe both sets of alignment marks simultaneously and in principle maintain image information on a live acquisition basis during the process of bringing the wafers into contact.

For a normal IR light source the band gap of the semiconductor must be ≥1 eV and the intensity (brightness) will decrease exponentially with the thickness of the substrate as a function of the

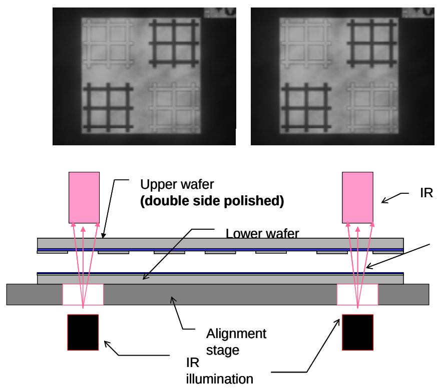

Figure 5. Schematic illustration of IR (Infrared alignment) process. Also show are the submicron IR alignment marks designed for automated alignment software.

absorption coefficient in the material. If the photon energy of the light in electron volts is greater than the semiconductor band gap, there will be strong or total adsorption. For silicon substrates the substrate resistivity must be >0.01 Ohm-cm unless the wafers are sufficiently thin to prevent absorption of the light.

Figure 5 shows the basic IR imaging concept and also demonstrates that the requirement for dual side polishing only applies to one wafer. This is because the scattering from the backside roughness on standard wafers is only problematic on the wafer that lies between the bond interface and the imaging camera. The source side scattering generates minimal image distortion.

For samples in which the substrates are not transparent to IR radiation or backside processing is not an option face-to-face alignment is needed. Figure 6 shows an example in which the front side marks are aligned using ISA mode in which a thin camera is inserted between the substrates and simultaneous imaging of the alignment marks is possible. Once aligned, the camera is retracted and the wafers are contacted. This technique is popular with compound semiconductor alignment, power devices built on highly doped substrates or wafers with extensive blanket layers of metal. Many 3D applications also use intersubstrate alignment because metal layers and device structure make the IR method very difficult unless open areas are reserved around the alignment keys.

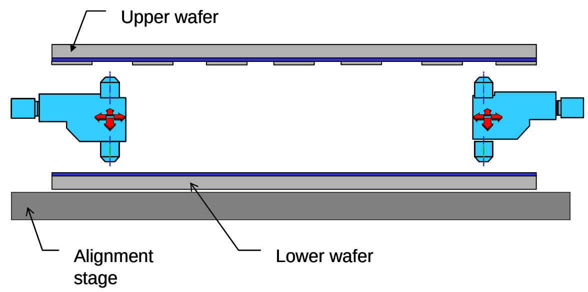

Figure 6. Schematic illustration of the basic steps involved in ISA (inter-substrate alignment) process. ISA Alignment utilizes dual imaging objectives on both the left and right alignment optics.

The selection of the alignment keys is equally important and recommendations exist for each of the types of bonds and the alignments. These are further subdivided depending upon if a human will be doing the alignment on manual systems or if an automated system is used with pattern recognition. Please refer to reference 3 for further details.

Bonding Strategies

There are six basic bonding techniques to choose from. These include: anodic, metal diffusion, metal eutectic, glass frit, polymers and fusion (silicon direct) bonding. Table 2 compares and contrasts the important difference of each technique.

Anodic Bonds

Anodic bonding is an electric field assisted diffusion process. In this process flow a cap wafer, usually a thermally matched glass is aligned with the silicon based MEMS wafer. A negative voltage is applied to the glass side of the stack and the positive voltage is applied to the backside of the silicon. During heating the mobile ions in the glass (generally Na^{+}) are drawn away from the interface to the backside of the glass against the anode. Simultaneously the silicon ions are pushed toward the glass interface and fill in the vacancies left behind. This reforms the glass/silicon interface and creates the bond usually a silicate reaction via ionic bond formation.

TABLE 2. Bond Methods Comparison

Example Materials	Temp. (C)	Applied Force(N)	Voltage (V)	Surface Roughness	Bond Vac. (Torr)	Hermetic	Alignment	Application	Comments	Cautions
Anodic Bonding										
Corning 7740,7070, etc	180-500	500N	200-1000	<20 nm	$>=10^{-6}$	Y	>2µm	MEMS Hermetic Seals, Gyros, accelerometers, pressure sensors	Requires Glass to Si all other combinations are experimental	Not compatible with CMOS or FEOL due to ion contamination
Soda Lime 0080	180-500	500N	200-1000	<20 nm	$>=10^{-6}$	Y	>2µm			
Aliminosilicate 1720	180-500	500N	200-1000	<20 nm	$>=10^{-6}$	Y	>2µm			
Sputtered Glasses	180-500	500N	200-1000	<20 nm	$>=10^{-6}$	Y	>2µm			
Lead Free Glass from Schott, Corning and Asahi	>400C	500N	200-1000	<20 nm	$>=10^{-6}$	Y	>2µm			
Silicon Fusion, Silicon Direct, Thermal Fusion or SOI Bonding										
Si, SiO_2, Nitrides.LTO, TEOS etc	<=1100*	NA**	NA	<1nm	$>=10^{-6}$	Y	≥0.5µm	Advanced substrates (SOI, GeOI, sSOI, SOS), optical materials	Requires extremely smooth and flat wafers with zero particles.	Very low yields on most MEMS products. Some success on 3D IC applications.
GaAs, InP,GaP	<400*	NA**	NA	<1nm	$>=10^{-6}$	Y	≥0.5µm			
Sapphire,Quartz,Glass	<400*	NA**	NA	<1nm	$>=10^{-6}$	Y	≥0.5µm			
Thermal Compression Bonding										
Glass Frits										
Ferro 11-036	400-500	2-5KN	NA	<1um	10	Y	>5µm	MEMS Hermetic Seals, Gyros, accelerometers, pressure sensors	Requires large seal rings but very forgiving for surface shape and particles	Not compatible with CMOS or FEOL due to ion contamination
Lead Free Glass Frit	>500	2-10KN	NA	<1um	10	Y				
Eutectics										
Au-Si (T_e=363, 81.4% Au)	363	1-10 kN	NA	<0.1um	Reducing	Y	>2µm	MEMS Hermetic Seals and Packaging, RF resonators & switches, accelerometers some optical devices	Can be driven by alloy melting or diffusion/melt process. Must discuss the depositon of the material. Force ramp is required to get high yields. Suss exclusive feature.	Because the materials melt, severely bowed wafers not compatible with this process. Works with all substrate types.
Au-Sn (T_e=280, 20% Au)	280	1-10 kN	NA	<0.1um	Reducing	Y	>2µm			
Au-Ge (T_e=361, 88%Au)	361	1-10 kN	NA	<0.1um	Reducing	Y	>2µm			
Au-In (T_e=156,1%Au)		1-10 kN	NA	<0.1um	Reducing	Y	>2µm			
Al-Ge (T_e=419, 49%Al)		1-10 kN	NA	<0.1um	Reducing	Y	>2µm			
Cu-Sn (T_e=231, 1%Cu)		1-10 kN	NA	<0.1um	Reducing	Y	>2µm			
Metal Diffusion										
Au-Au	300-400	5-40 kN	NA	<4nm	Reducing	Y	≥0.5µm	Advanced hermetic sealing. 3D integrated devices	Temperature drives the misalignment. For critical alignment you need advanced platforms not standard offerings.	Requires good quality films. Usually needs CMP. Works for all substrates.
Cu-Cu	380-450	5-40 kN	NA	<4nm	Reducing	Y	≥0.5µm			
Al-Al	375-425	>40KN	NA	<4nm	Reducing	Y	≥0.5µm			
Polymers*										
BCB, WL5300, HD3003	<300	1-5 kN	NA	<1um	Atm or Vac	N	≥0.5µm	3D, CMOS IS, MOEMS	Works with any substrate material	Not hermetic to vacuum
SU8, AZ400 (UV resists)	<200	1-5 kN	NA	<1um	Atm or Vac	N	>5µm	Mostly thick resist applications. BioMEMS etc.	Several SU8 formulations can be chosen to fit the applications. Any substrate works.	Not hermetic to vacuum
PMMA,PLG (LIGA resists)	<200	1-5 kN	NA	<1um	Atm or Vac	N	≥0.5µm	Microfluidics, MEMS	Not so common as other polymer bonds.	Not hermetic to vacuum

* Usually done in Batch processing after pre-bond

**Not usually needed but can be used.

***Precision alignment requires thin layers, typical alignment applications will be >2µm

Typical processing parameters range from 200-500°C with ~1KN of force applied for approximately 7-10 minutes. Note, the applied force is used to press out bow/warp and create intimate contact between the surfaces to ensure good electrical conduction across the wafer stack. The atmosphere inside the cavities can be control by the adjustment of the processing chamber and ranges from very low vacuum levels to overpressures up to 3bar.

Due to the contamination associated with the sodium and other mobile ions there are limitation to using anodic bonding when integrating MEMS and CMOS. Anodic bonding is not compatible with CMOS fabrication and front end processes.

Metal Diffusion Bonding

The three most common diffusion bonds are gold to gold, aluminum to aluminum and copper to copper bonds. Permanent bonding with metal diffusion bonds has benefited greatly from the CMOS industry. For copper, the development and infrastructure for copper damascene processing is extensive as is the deposition methods and infrastructure for aluminum deposition.

Atomic motion (diffusion) proceeds from one crystal lattice location to another and can not “leap” free space. Hence, high applied forces in the bonder can be used to press out bow and warp and plastically deform (to some degree) the surface asperities in the metal films. However, fundamentally the CMP processing must create flat films with a microroughness on the order of ~5nm RMS in order to achieve void free diffusion bonds.

The metal surfaces must be free from oxidation and contamination. Metal self-diffusion rates can drop several orders of magnitude if the surface is oxidized. The removal of the oxide layer is achieved by various oxide etch chemistries. Dry methods such as acid vapor treatments are advantageous because the wafers do not have to be immersed in fluids and etching of underlying passivation or adhesion layers can be minimized or excluded. One chemistry that has worked well is the formic acid vapor cleaning.[3,6]

Metal films for diffusion bonding can be deposited by several methods. Evaporation and sputtering methods produce high quality films with limited impurities. However the deposition rates are slow and these methods are generally used when a micron or submicron layer thickness is needed. For thicker films, electroplating is used and care should be taken to control both the roughness of the films and the purity of the layer.

Glass Frit Bonding

When MEMS devices headed into production glass frit was an alternative bonding method to anodic bonding which provided for a more forgiving interface with expectations of good hermeticity levels. Small glass particles are suspended in a paste matrix. The frit can be applied by screen printing techniques and glazed onto the cap wafer. Since the paste is applied in a softened state particles are encapsulated during application and solidified into the seal ring during the glazing operation. Most of the volatiles of the paste are removed during the glazing operation and the pattern that remains is solid. During bonding the frit is sandwiched between the cap wafer and the device wafer and heated above its softening point. As the force is applied to the wafer stack in the bonder the paste reflows and creates a conformal seal around the active devices. The frit hardens and contracts upon cooling.

Critics of glass frit will point out that the seal geometries are necessarily large due to the hermetic properties of glass. The alignment is sometimes compromised by shifting of the upper wafer with respect to the lower substrate as the force is applied to the viscous interface. The technique is capable of ~5µm alignment accuracy if modern equipment and best known practices are followed. The true advantage of the glass frit technique is the self-planarization of the interface and lack of sensitivity to particles and surface topography.

Unfortunately the permeability of glass seals precludes the scaling of glass frit to smaller device geometries. In addition the cleanliness of the frit itself is not compatible with CMOS fabrication and limits integration possibilities in new devices. A good alternative to glass frit processes when hermeticity is required are the eutectic metal bonds.

Eutectic Metal Bonding

Eutectic metals are alloys that transition directly from the solid to the liquid state without dissociating into a two phase (liquid + solid) equilibrium. Eutectic alloys can be deposited via electroplating an alloy, via alloy sputter targets or with dual source evaporation. The eutectic alloy can also be formed by diffusion reactions of pure materials followed by melting of the eutectic composition. Regardless of the method of deposition and reaction pathway, the important feature is the phase change between solid and liquid during the anneal step.

During the bonding step the device wafer and the cap wafer will be pressed together and heated. As the alloy melts the interface is planarized and surface roughness and small particles are encapsulated within the seal. It is this feature that makes the eutectic alloy an excellent replacement method for the glass frit process. Additional benefits of the eutectic alloy sealing method include the ability to reduce the seal ring geometries, increase hermeticity levels, and shrink device feature size. Glass frit seals are generally 70-200µm wide and equally thick. The metal eutectic seal geometry is typically 1-5µm thick and 10-15µm wide.

The bonds are generally performed using a reducing atmosphere of 4% hydrogen mixed with inert carrier gas like nitrogen. The most important consideration for the bonding equipment is the thermal uniformity and pressure uniformity across the wafer. With proper control of these parameters the viscosity of the melt will be consistent and the applied force will press perpendicular to the interface. Resulting seal lines are uniformly compressed and create a gasket-like seal. Shearing of the interface will be negligible and post bond alignment accuracies of ≤2µm are achievable.

Silicon Fusion or Silicon Direct Bonding

In theory the most hermetic seal is the single crystal bond. This drives the research efforts in the development of fusion or direct bonding technologies for MEMS fabrication. Silicon direct bonding does not involve intermediate layers between the device wafer and the cap wafer. However without these layers the interface is incapable of accommodating surface roughness, particles or thickness variations.

In short the interface must be perfectly clean, flat and smooth.

Wafers are prepared for fusion bonding by making the surface hydrophilic via a plasma activation step or immersion in wet chemistries containing [OH] groups. The [OH] groups attach to the surface and enable silanol bridges to form between the two wafers when placed in contact.[7] In fact the van der Waals attractions between the two substrates is strong enough to pull the wafers together and expel the air from the interface in a reaction called the "spontaneous bond wave". In order for the bond wave to propagate the surface roughness must be on the order of 1nm or less and the bow/warp needs to be <40µm.

In MEMS fabrication very few device wafers can achieve this level of surface quality and wafer flatness.

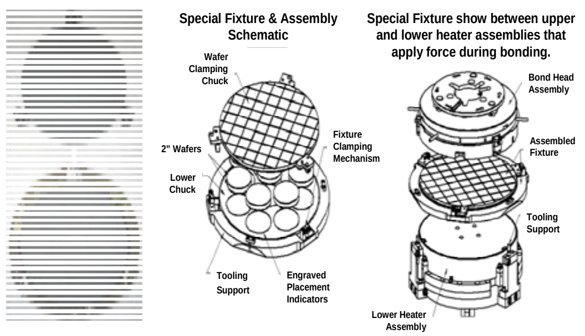

Figure 7. Multiple substrate bond fixture for use in SUSS MicroTec SB8e bond chambers.[xx]

Polymer Bonding

While hermeticity is a requirement for many automotive applications there are many consumer products including image sensors, microfluidic devices and others that primarily require prevention of moisture penetration of the seal. Polymer bonds are completed at 190-320°C and can be formed with epoxies, adhesives and photo-sensitive resist materials.[8,9] In some cases the polymer can even become part of the device itself as in many SU8 applications.[10] The most common materials for wafer level bonding with polymers are BCB, SU8, WL5300, HD3003, PMMA, Polyimides and several AZ resists

The advantages of polymer bonds include self planarization and tolerance to particles, wafer topography and particles. Some of the materials are stable up to above 300°C and enable post bond processing such as wafer thinning, etching and deposition after the bond.

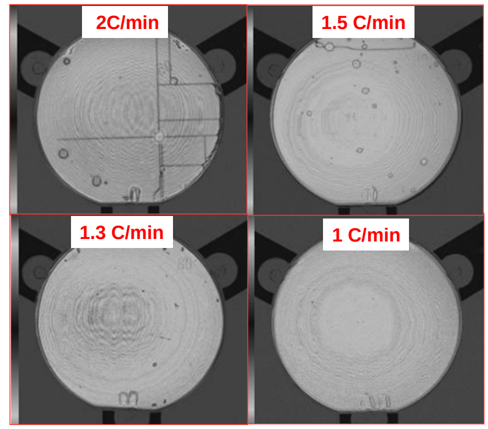

Figure 8. Effects of cooling rate on the cracking of GaAs bonded to Si. Only slow cooling rates eliminate substrate cracks.

Examples

Figure 7 illustrates an excellent packaging solution for LEDs.[11] The multiple substrate fixture allows for systems with extreme thermal mismatch in CTE (coefficient of thermal expansion) to be bonded simultaneously. This mediates the long processing times that result from requirements on cooling rates.

As shown in figure 8, many LED applications require combinations of materials that can not tolerate rapid cooling at the end of the bond cycle. In this example of GaAs to Si LED bonding the cooling must be done at ≤1°C/min to avoid material dislocation and cracking. This takes several hours and manufacturing would not be economical or competitive without the use of multiple substrate processing.

Aluminum diffusion bonding is a relatively new process to appear in the wafer bonding "toolbox". This metallurgy is used extensively for metallization in devices and therefore is compatible with almost any process flow. Shown in figure 9 is a 200mm example using blanket layers of aluminum as a bond interlayer material and also a successfully aligned and bonded 150mm device wafer. The device wafer was aligned using ISA alignment methods and resulting overlay accuracy was <2µm.

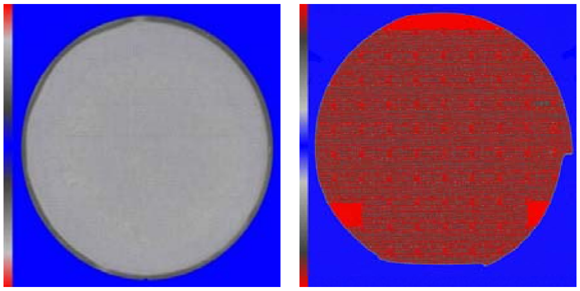

Figure 9. Left is a blanket layer of aluminum on a 200mm wafer successfully bonding with Al diffusion techniques. On the right is a 150mm device wafer also bonded with aligned Al to Al diffusion methods.

Polymer materials are used extensively in wafer level packaging. Materials like BCB are used in high end applications such as 3D IC's and CIS (CMOS image sensors) because of its compatibility with high alignment accuracy and post processing demands such as dry etching and CMP. Figure 10 shows 200mm device wafers bonded using BCB.[8.9]

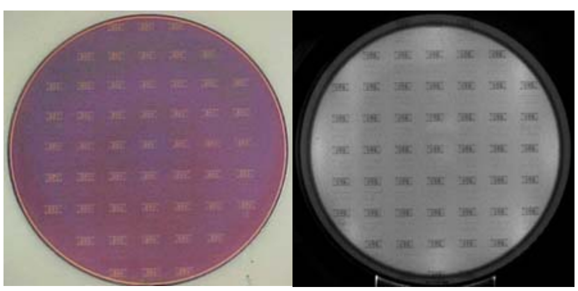

Figure 10. Left image is a view of the image sensor through the glass substrate. Right is an IR image showing void free results. Wafer size is 200mm and bond interface is BCB.

Summary

The balancing of device requirements and materials properties is challenging but a large variety of bonding options and equipment choices provide excellent solutions. The adage "anything on anything" is truly becoming reality through high technology wafer level bonding and no longer applies to the fusion bonding techniques only.

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