UMW IR21271STR

300V Current Sensing Single Channel MOSFET/IGBT Driver

1.Description

UMW IR21271STR is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable rug-gedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs, down to 3.3V. The protection circuity detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain FAULT signal is provided to indicate that an over-current shutdown has occurred. The output driver features a high pulse current buffer stage designed for minimum cross-conduction.The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side or low side configuration which operates up to 300 volts.

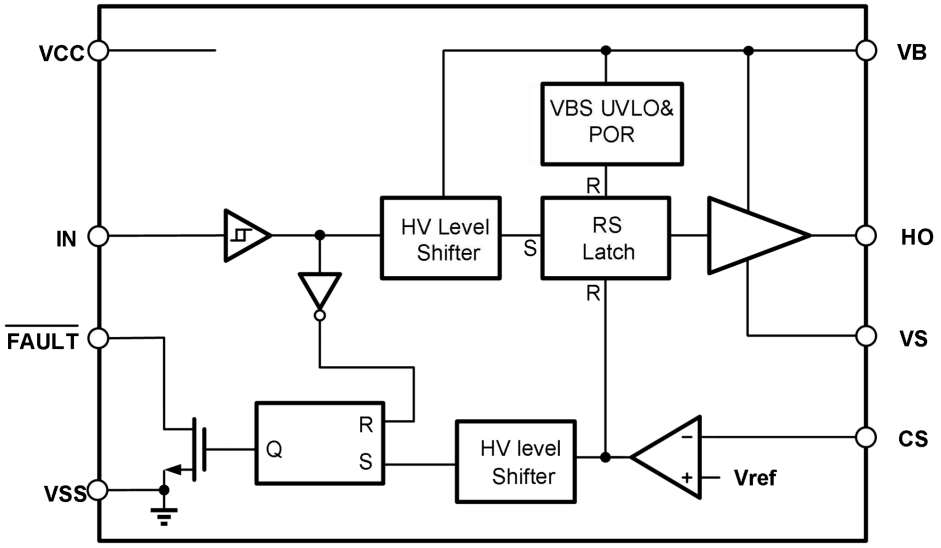
2.Features

- Floating channel designed for bootstrap operation
- Fully operational to +300 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ±50 V/nsec
- Allowable negative Vs capability: -5V
- Output in phase with input
- Gate drive supply range from 8V to 22V
- Undervoltage lockout for both channels
  --UVLO 6.8V/7.2V
- Propagation delay
  --Ton/Toff =150ns/150ns
- Wide operating temperature range:
  -40°C ~125°C
- Fault lead indicates shutdown has occurred
- RoSH compatible
- SOIC8(S)

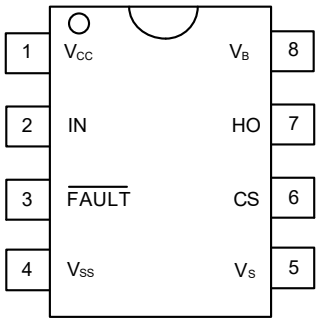
3.Applications

- Motor control and drive
- Robot technology
- Fast charging of electric vehicles

4.Functional Block Diagram



5.Pinning Information



SOP-8

Lead Definitions

Number	Symbol	Description
1	VCC	Power supply
2	IN	Logic input for high side gate driver output (HO), in phase
3	$\overline{\text{FAULT}}$	Indicates over-current shutdown has occurred,negative logic
4	V_{SS}	Logic ground
5	V_S	High side floating supply return
6	CS	Current sense input to current sense comparator
7	HO	High side gate drive output
8	V_B	High side floating supply

6.Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to V_{SS} and an ambient temperature of 25°C.

Parameter	Symbol	Min	Max	Units
High side floating supply	V_B	-0.3	322	V
High side floating supply return	V_S	V_B-22	V_B+0.3	V
High side gate drive output	V_{HO}	V_S-0.3	V_B+0.3	V
Low side and main power supply	V_{CC}	-0.3	22	V
Logic input of IN	V_{LO}	-0.3	V_{CC}+0.3	V
$\overline{\text{FAULT}}$ output voltage	V_{FLT}	-0.3	V_{CC}+0.3	V
Current sense voltage	V_{CS}	V_S-0.3	V_B+0.3	V
Allowable Offset Supply Voltage Transient	dV_S/dt	-	50	V/ns
HBM Model	ESD	2		kV
Machine Model		500		V
Package Power Dissipation @ T_A ≤25°C	P_D		0.625	W
Thermal Resistance.,Junction to Ambient	Rth_{JA}		200	°C/W
Junction Temperature	T_J		150	°C
Storage Temperature	T_S	-55	150	°C
Lead Temperature (Soldering, 10 seconds)	T_L		300	°C

7.Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Parameter	Symbol	Min	Max	Units
High side floating supply	V_B	V_S + 8	V_S + 20	V
High side floating supply return	V_S	-5	300	V
High side gate drive output	V_{HO}	V_S	V_B	V
Low side and main power supply	V_{CC}	8	20	V
Logic input of IN	V_{IN}	0	V_{CC}	V
$\overline{\text{FAULT}}$ output voltage	V_{FLT}	0	V_{CC}	V
Current sense signal voltage	V_{CS}	V_S	V_S+5	V
Ambient temperature	T_A	-40	125	°C

Note1： Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design.

8.Dynamical Electrical Characteristics

T_A=25°C, V_{CC}=V_B=15V, C_L=1nF, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Turn-on propagation delay	t_{ON}	V_S=0V		150	250	ns
Turn-off propagation delay	t_{OFF}	V_S=300V		150	250	ns
Turn-on rise time	t_R			80	130	ns
Turn-off fall time	t_F			40	70	ns
Start-up blanking time	t_{BL}		550	750	950	ns
CS shutdown propagation delay	t_{CS}			65	360	ns
CS to FAULT pull-up propagation delay	t_{flt}			270	510	ns
Logic “1”(IN) input voltage	V_{IH}	V_{CC}=10Vto 20V	2.5			V
Logic “0” (IN) input voltage	V_{IL}				0.8	V
CS input positive going threshold	V_{CSTH+}		1.5	1.8	2.1	V
V_{BS} supply UVLO threshold	V_{BSUV+}		6.3	7.2	8.2	V
	V_{BSUV-}		6	6.8	7.7	V
High-side floating supply leakage current	I_{LK}	V_B=V_S=300V			50	μA
Quiescent V_B supply current	I_{QBS}	V_{IN}=0V or 5V		300	800	μA
Quiescent V_{CC} supply current	I_{QCC}	V_{IN}=0V or 5V		60	120	μA
“High"CS bias current	I_{CS+}	CS=3V			5	μA
“High"CS bias current	I_{CS-}	CS=0V			5	μA
High level output voltage, V_{BIAS} -V_O	V_{OH}	I_O=2mA			0.2	V
Low level output voltage, V_O	V_{OL}				0.1	V
Logic “1”input bias current	I_{IN+}			7	15	μA
Logic “0” input bias current	I_{IN-}			0	5	μA
Output high short circuit pulsed current	I_{O+}		200	300		mA
Output low short circuit pulsed current	I_{O-}	V_O=0V, PW≤10us	420	600		mA
FAULT-low on resistance	$R_{on,FLT}$	V_O=15V, PW≤10us		125		Ω

9.Function Description

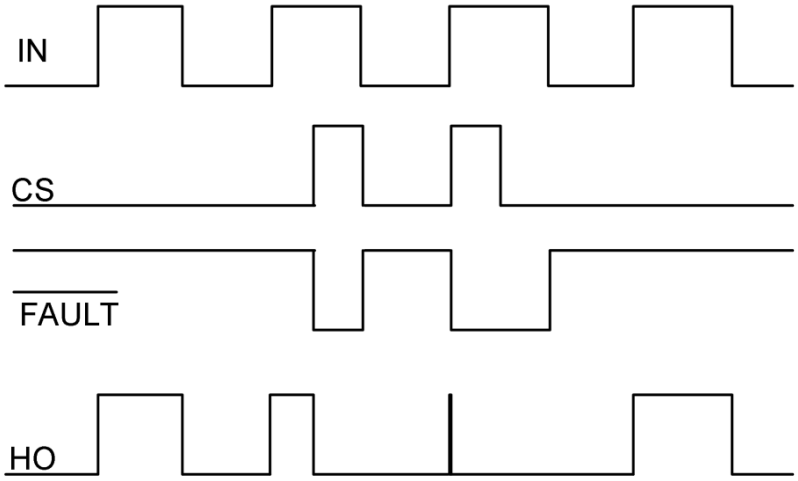


Figure 1. IR21271STR Input and output timing waveform

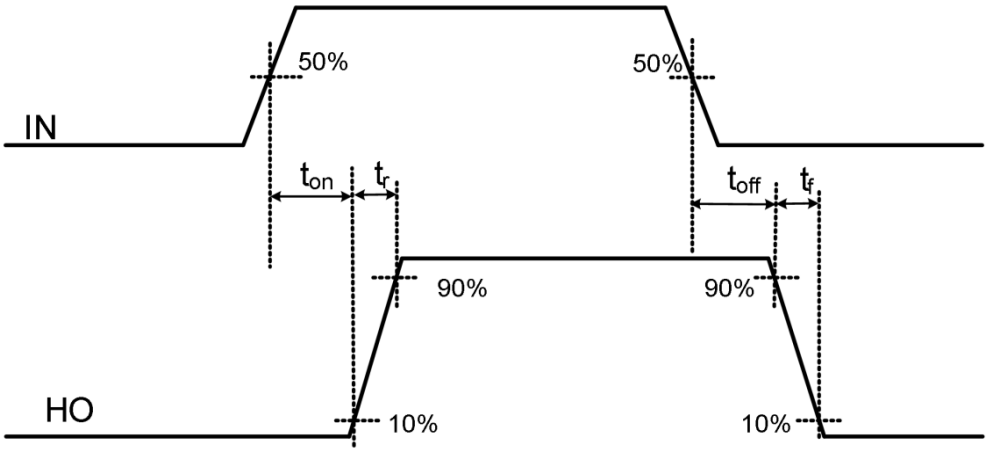


Figure 2. Switching Time Waveform Definition

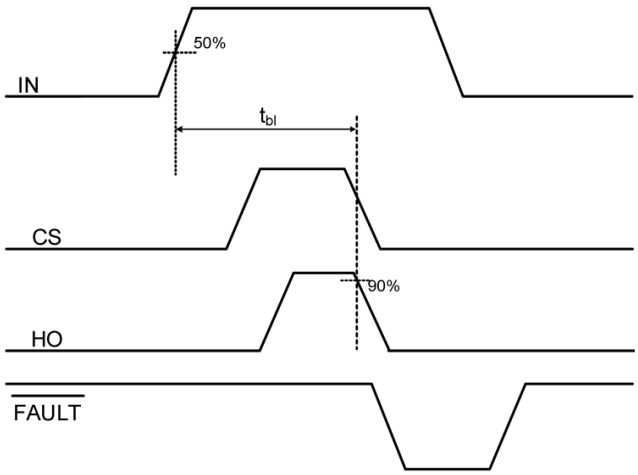


Figure 3. Start-up Blanking Time Waveform Definitions

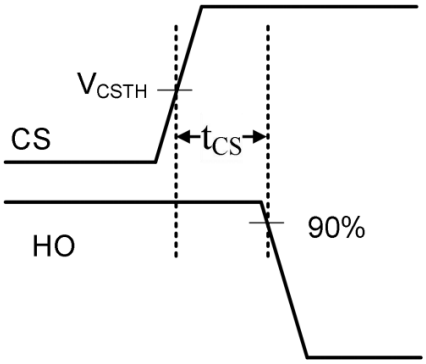


Figure 4. CS Shotdown Waveform Definitions

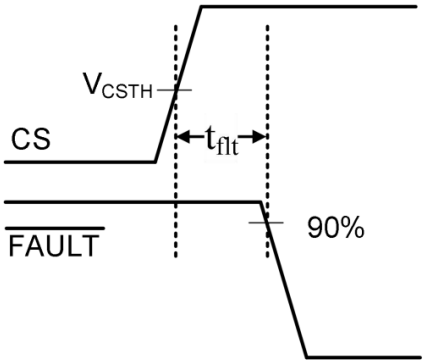


Figure 5. CS to FAULT Waveform Definitions

10.Function Block Diagram

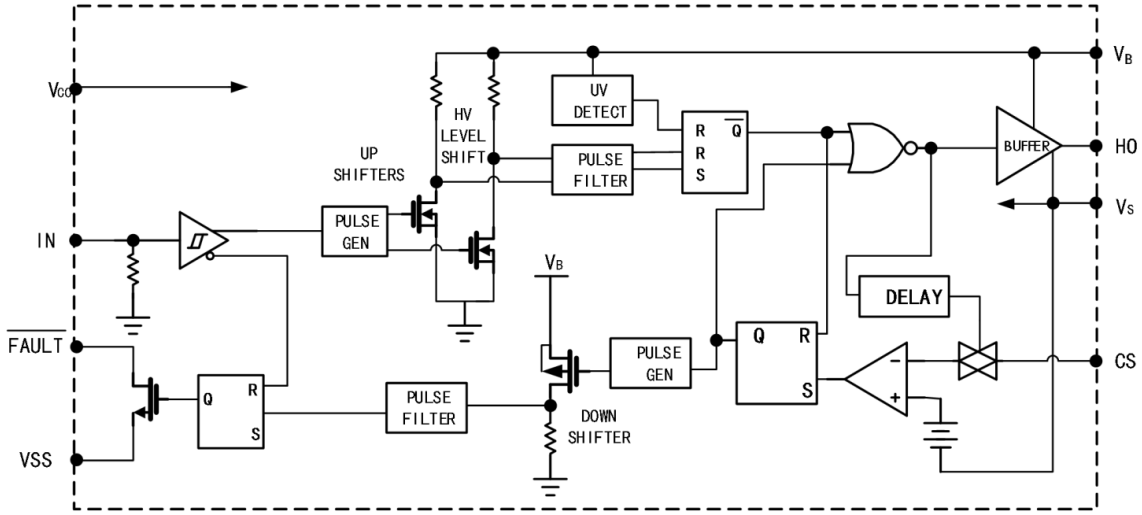


Figure 6. Function Block Diagram of IR21271STR

11.Application Message

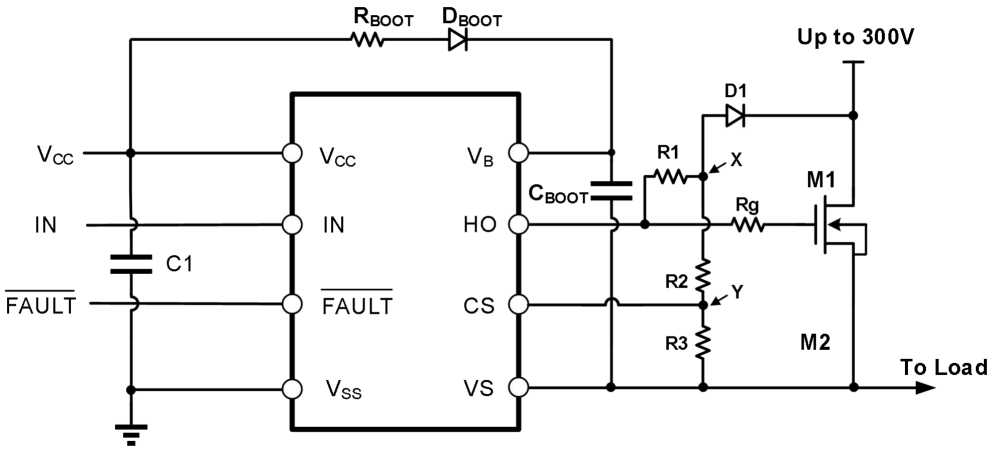


Figure 7. Typical application circuit of IR21271STR

To Calculate the resistor values use the following guidelines.

Rg is the gate resistor, and the value is chosen to optimize switching speed and switching losses.R1 is typically chosen to be 10k (12V Vbs)/22k (15V Vbs)/33k (18V Vbs); this high value helps to minimize the increased miller capacitance effect from diode D1, and makes sure there is not significant current being drawn from the HO output. Note diode D1 must have the same characteristics as the bootstrap diode. When the HO output goes high MOSFET (or it could be an IGBT) Q1 turns on. Now point X in fig 10-2) will be pulled down to a voltage which equals the voltage across the FET (V_{DS}) plus the voltage across diode D1. Therefore in an overload condition we want to shut down the driver output when the voltage across the FET (or IGBT) Q1 equals a set limit that indicates on overload condition has occurred (for example 8V). Therefore with a 8V Vds on Q1. V_{D1} is typically 1.2V for a small 1A ultra fast recovery diode.

$$V_X=V_{D1}+V_{DS}$$

$$V_X=1.2+8$$

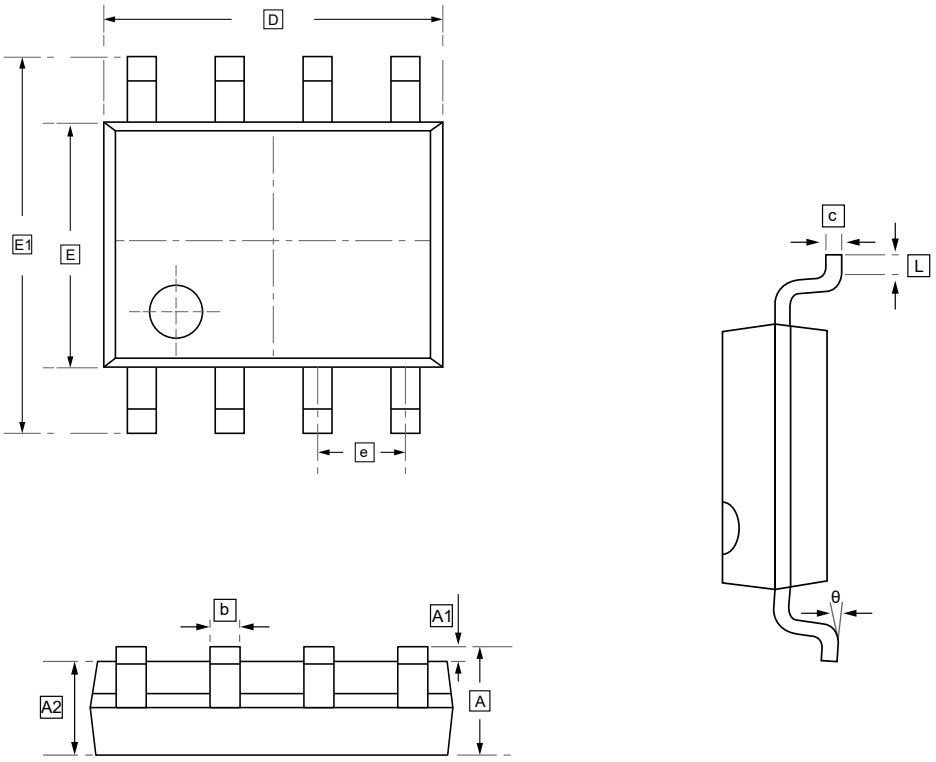
$$V_X=9.2V$$

For a UMW IR21271STR the CS pin threshold is 1.8V,therefore we need to divide V_X,so that when V_X=11.2V,then V_Y=1.8V.

$$V_Y=V_X\cdot R3/(R2+R3) \qquad \text{let } R2=33k$$

$$R3=6.319K$$

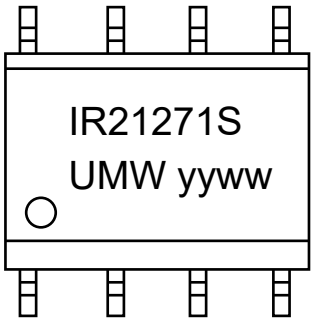
12.SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

13.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IR21271STR	SOP-8	2500	Tape and reel

14.Disclaimer

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