Total Pages—5

Set-21(I)

B.Tech.- 4th (IT)

Computer Organization and Architecture

Full Marks : 50

Time : $2\frac{1}{2}$ hours

Answer **all** questions

The figures in the right-hand margin indicate marks

Symbols carry usual meaning

1. Answer *all* questions : 2×5

   (*a*) Differentiate between Computer Organization and Computer Architecture ?

   (*b*) What is Compaction ? Why it is required ?

   (*c*) What do you mean by Locality of Reference ? Explain different types of Locality of Reference with example.

   (*d*) Whether internal Interrupt is synchronous

(*Turn Over*)

with the program while external Interrupt is asynchronous ? Justify with example.

(c) Whether Pipeline system is better than Non-pipeline system for single instruction execution ? Justify.

2. (a) What is Booth's multiplication algorithm ? Perform the multiplication 13 X -5 step by step using Booth's multiplication algorithm. 5

(b) What is Stack pointer ? Is it different from Instruction pointer ? Justify. 3

Or

(a) Draw a neat diagram of Extended IAS Architecture. Describe the functionalities of its Registers. 4

(b) Represent $(-2.5)_{10}$ in single precision floating point format. 4

3. (a) Write the Two Address and One Address Instructions to evaluate the expression -

$$Y = A - B + C * (D + E)$$ 4

(b) What is polish notation ? Convert the following expression into RPN. Explain diagrammatically the STACK operation step by step to evaluate this. 4

$$(3+4)[10(2+6)+8]$$

Or

(a) What will be the Control sequences for execution of a complete instruction ADD R1, [R2] ? 5

(b) What is Instruction Cycle ? Draw Instruction cycle State diagram and explain each State. 3

4. (a) Suppose a computer using direct mapped cache has 2^{20} bytes of byte-addressable main memory and a cache of 32 blocks, where each cache block contains 16 bytes. 5

(i) How many blocks of main memory are there ?

(ii) What are the bit sizes of the tag, block and word fields ?

(b) What is Pseudo-static RAM ? How it is different from DRAM ? 3

Or

Consider the following page requests occur during a time interval: 4, 2, 0, 1, 2, 6, 1, 4, 0, 1, 0, 2, 3, 5, 7. Show diagrammatically step by step the page position in the main memory after each page reference using the following replacement algorithms in a virtual memory system if there are four frames in the main memory. 8

(i) LRU (ii) LFU

5. (*a*) What is an Interrupt ? Explain the function of Daisy Chaining Priority interrupt with diagram. 5

(*b*) Distinguish and differentiate between I/O mapped I/O and Memory mapped I/O. 3

Or

(*a*) What is Asynchronous data transfer ? Explain Serial asynchronous data transfer technique. 4

(*b*) What is DMA data transfer ? Differentiate between Cycle stealing mode and Burst mode of data transfer ? 4

(Continued)

6. Consider a Non-pipeline system takes 50 *ns* to complete the process an instruction. The same instruction can be processed in a Six-segment Pipeline system with a clock cycle of 10 *ns*. Determine the Speedup, Efficiency and Throughput of the pipeline system for 100 instructions. What is the maximum Speedup that can be achieved ? 8

Or

(*a*) Whether Loosely coupled multiprocessor is MSISD ? Justify your answer with diagram. 4

(*b*) Distinguish and differentiate between CISC and RISC architecture. 4