Total Pages : 8

B.Tech-3rd (EE)

Analog and Digital Electronic Circuits

Full Marks : 50

Time : 2.30 hours

Answer **all** questions.

The figures in the right-hand margin indicate marks.

Symbols carry usual meaning.

1. Answr *all* questions : 2 × 5

(*a*) Draw the hybrid equivalent model of a transistor in common emitter configuration.

(*b*) State the characteristics of an ideal OPAMP.

(*c*) Draw the transfer characteristic of FET.

(*d*) Design a half adder circuit with truth table.

(*Turn Over*)

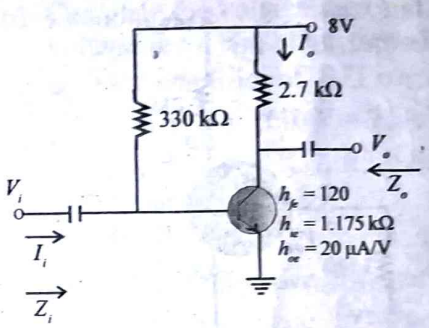
(*e*) Differentiate between combinational and sequential logic circuits.

2. (*a*) For a DC bias with voltage feedback circuit of $V_{CC} = 10$ V, $\beta = 90$, $R_C = 4.7$ kΩ, $R_E = 1.2$ kΩ, resistance across collector and base = 250 kΩ. Draw the circuit and find I_{BQ}, I_{CQ}, V_{CE}, V_B, V_C, V_E, I_{Csat}. 4

(*b*) Draw an emitter follower circuit and derive the expression for input impedance Z_i of the circuit. 4

Or

(*a*) For the network below determine (*i*) Z_i, (*ii*) Z_0, (*iii*) A_v, (*iv*) A_i. 4



(*b*) Draw the frequency response curve and explain the Miller effect on gain at high frequencies. 4

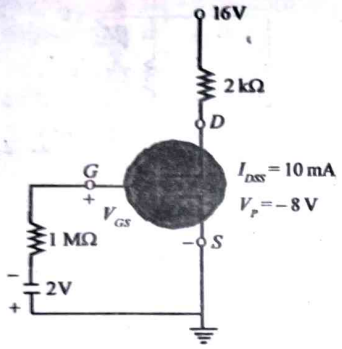
3. (*a*) Determine the following for the network given below 4

(*i*) V_{GS}

(*ii*) I_D

(*iii*) V_{DS}

(*iv*) V_G



(*b*) Discuss the magnitude of gain response curve of a RC coupled amplifier and find out its bandwidth. 4

Or

(*a*) With a neat diagram analyze an FET in Self-bias configuration. 4

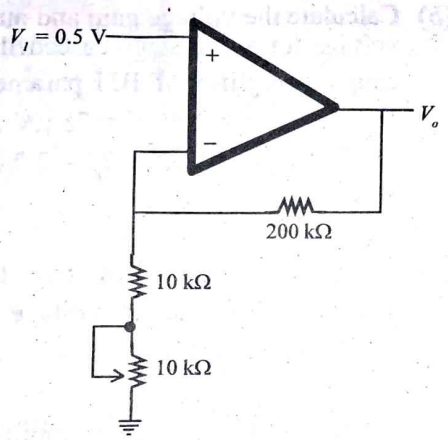
(*b*) Calculate the voltage gain and output voltage for a two stage cascaded RC coupled amplifier of BJT parameters $V_{CC} = 20$ V, $\beta = 200$, $V_i = 25$ μV, $R_1 = 15$ KΩ, $R_2 = 4.7$ KΩ, $R_C = 2.2$ KΩ, $R_E = 1$ KΩ. 4

4. (*a*) Design a first-order, low-pass filter using OPAMP. State its voltage gain and cutoff frequency. 4

(*b*) What is a class A power amplifier ? Derive its conversion efficiency. 4

Or

(*a*) What range of output voltage is developed in the circuit below. 4



(*b*) Discuss OPAMP as an integrator and differentiator. 4

5. (*a*) Simplify the following Boolean function F, together with the don't care conditions d. 4

$F(A,B,C,D) = \Sigma_m(1,3,5,7,9,15)$

$d(A,B,C,D) = \Sigma_m(4,6,12,13)$

(*b*) Given the Boolean function 4

$F = xy'z + x'y'z + w'xy + wx'y + wxy$

(*i*) Obtain the truth table of the function.

(*ii*) Simplify the expression.

(*iii*) Draw the logic diagram using logic gates.

Or

(*a*) Explain the BCD addition rules and perform the BCD addition for the decimal number 72 + 35. 4

(*b*) Convert the following expressions into sum of products and product of sums : 4

(*i*) $(AB+C)(B+C'D)$

(*ii*) $x' + x(x+y')(y+z')$

6. (*a*) What are the different types of shift register. Discuss the operation of 4-bit SISO shift register using J-K flip-flop. 4

(*b*) What is Race-around Condition of J-K flip-flop ? Describe J-K flip-flop operation with logic diagram and truth table. 4

Or

(*a*) Implement the following expressions using a multiplexer. 4

(*i*) $Y(A,B,C) = \Sigma_m(0,1,2,6,7)$

(*ii*) $Y(A,B,C) = \prod_M(0,1,4,5)$

(*b*) Implement a 4:16 decoder using 2:4 decoders. 4