VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY (VSSUT), ODISHA

Odd Mid Semester Examination for session 2024-25

COURSE NAME: SEMESTER: 3rd

BRANCH NAME: EEE

SUBJECT NAME: Analog Electronics Circuit

FULL MARKS: **30** TIME: **90 Minutes**

Answer **All** Questions.

The figures in the right hand margin indicate Marks. *Symbols carry usual meaning.*

Q1. Answer all Questions. **[2 × 3]**

a) What are the biasing conditions for different operating regions of BJT?

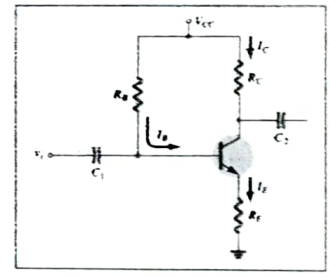
b) Explain Emitter follower circuit.

c) Write output current equation for Depletion and Enhancement type MOSFET.

Q2. a) What is biasing? Explain Emitter-biasing circuit with neat diagram. **[8]**

b) For emitter bias network, determine I_C, V_{CE}, V_C, V_E

Given $R_B = 430\ k\Omega$, $V_{cc} = 20v$
$R_C = 2\ k\Omega$,
$R_E = 1\ k\Omega$,
$\beta = 50$



OR

a) Explain fixed bias circuit with neat diagram. Compare the stability criteria with Emitter bias.

b) What is quiescent point? What is the preferred location of the operating point for faithful amplification and why?

[8]

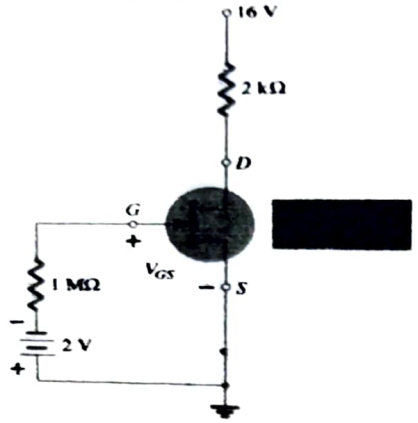
Q3. Explain the h-parameter model and find Av Ai Zi Zo for common emitter fixed bias configuration.

OR

Explain the r_e–model and compute the parameters for common emitter fixed bias configuration.

Q4. a) Sketch the transfer characteristics of an n-channel depletion type MOSFET with $I_{DSS} = 10mA$ and $V_p = -4V$. **[8]**

b) Determine the following for the circuit. Given I_{DSS} = 10 mA, V_P = -8V
i) V_{GSQ}, ii) I_{DQ}, iii) V_{DS}, iv) V_D



OR

Compare fixed bias and emitter bias for n-channel JFET using DC analysis.