國立交通大學 102 學年度碩士班考試入學試題

科目：計算機系統(1003)　　考試日期:102 年 2 月 4 日 第 3 節

系所班別：資訊聯招　　第 1 頁,共 10 頁

【不可使用計算機】＊作答前請先核對試題、答案卷(試卷)與准考證之所組別與考科是否相符！！

單一選擇題，共 12 題，每一題答對給 4 分，未答得 0 分，答錯倒扣 1.5 分。請使用答案卡作答

1. According to the following program with fork() system call, explain what the output will be at Line A. Suppose all fork() system calls succeed.

```
#include <sys/types.h>
#include <stdio.h>
#include <unistd.h>

int main()
{
     int value = 5;
     pid_t pid;
     pid = fork();
     value +=10;
     pid = fork();
     value +=10;

     if (pid==0) {
       value +=15;
       return 0;
     } else if (pid > 0) {
       wait(NULL);
       printf("%d\n",value); /* LINE A */
       return 0;
     }
}
```

(a) 5.
(b) 15.
(c) 25.
(d) 40.
(e) 45.

2. The following program uses the Pthreads API. What would be the output from the program at LINE C. Suppose the system program executes in a Linux system (kernel 3.2.0, x86_64) and with a very light load.

```
#include <pthread.h>
#include <stdio.h>

int value=0;
void *runner(void *param);
int main(int argc, char *argv[])
{
   int pid;
   pthread_t tid, tid2;
   pthread_attr_t attr;

   pid = fork();
   value++;
   if (pid==0) {
      pthread_attr_init(&attr);
      pthread_create(&tid, &attr, runner, NULL);
      pthread_create(&tid2, &attr, runner, NULL);
      pthread_join(tid, NULL);
      pthread_join(tid2, NULL);
      printf("%d",value); /*LINE C*/
```

```
    } else if (pid >0) {
        wait(NULL);
        return(0);
}

void *runner(void *param) {
    int temp=value;
    temp += 5;
    sleep(2);
    value = temp;
    pthread_exit(0);
}
```

(a) 1.
(b) 5.
(c) 11.
(d) 6.
(e) 10.

3. Which of the following statements is in*correct*?
   (a) The Mac OS X kernel is based on the Mach microkernel.
   (b) Windows XP's architecture is more monolithic than microkernel.
   (c) Linux kernel is based on the microkernel approach.
   (d) The guest OS must be modified to run on the paravirtualized hardware.
   (e) If a guest OS can be booted from an image file in the host operating system, we can simply copy the image file to another location and boot another guest OS.

4. Which of the following statements is *incorrect* regarding disks?
   (a) Performing a logical formatting on a disk means that we create a file system on it.
   (b) A soft error of disk means that some data bits in a sector have been corrupted but can be corrected.
   (c) The operation system can treat each partition of a disk as though it were a separate disk.
   (d) A network-attached storage is a private network connecting servers and storage units.
   (e) Compared with SCAN scheduling algorithm, C-SCAN provides a more uniform wait time.

5. Which of the following statements is *correct* regarding allocating space to files?
   (a) Indexed allocation supports direct access but suffers from external fragmentation.
   (b) Linked allocation allows the blocks of a file to be scattered anywhere on the disk and is very efficient in performing random access in a file.
   (c) Contiguous allocation suffers from internal fragmentation but is very efficient in performing random access in a file.
   (d) The file-allocation table (FAT) can result in a significant number of disk head seeks, unless the FAT is cached.
   (e) Regarding pointer overhead, linked allocation suffers from wasted space more severely than indexed allocation.

6. The ideal one way hash function is collision free. Given y=h(x). Suppose x is of infinite length and y is of 8 bits. What is the probability that two different inputs, x and x', of the hash function collide?
   (a) 0
   (b) 1
   (c) 1/8
   (d) 1/128

(e) 1/256

7. Consider the following program:

```
#include <stdio.h>
#define BUFFER_SIZE 256
int main(int argc, char *argv[])
{
    char buffer[BUFFER_SIZE];
    if (argc < 2)
        return -1;
    else {
        _____; /*fill in the right instruction herein*/
        return 0;
    }
}
```

To avoid the security problem, what will be the best choice of instruction to fill in the empty slot in the program?

(a) strcopy(buffer, argv[1]);
(b) strcopy(buffer, argv[2]);
(c) strncpy(buffer, argv[1], sizeof(buffer));
(d) strncpy(buffer, argv[1], sizeof(buffer)-1);
(e) strncpy(buffer, argv[1], sizeof(buffer)+1);

8. Which one of the following statements is TRUE?
   (a) From the point of view of a network service provider, latency is a suitable metric to measure the performance of the network service server.
   (b) Mini-computer has disappeared from the computer market since main-frame computers have been well designed to have much more computing power than mini-computers.
   (c) The CPU operating clock rate has not been continuously and significantly improved these years because Moor's law has been invalidate since several years ago.
   (d) CPU and RF/analog designs are generally regarded as two main streams/representatives that can represent the semiconductor technology level of a nation.
   (e) With the fixed number of defects per area, a small die-area IC design has better manufacture yield than the big die-area one.

9. Which one of the following statements is incorrect?
   (a) With the same ISA and circuit design, the CPU with higher clock rate does not necessarily run through a program in shorter runtime than the CPU with lower clock rate.
   (b) Million Instructions Per Second (MIPS) is not a unfair metric to compare the performances of two computers because MIPS metric only counts the number of executed instructions but does not consider the CPU idle time for stalling CPU requested by cache miss.
   (c) Programming languages and compilers heavily influence the number of executed machine instructions per operation.
   (d) Algorithms determine the number of executed operations.

(e) Computer *A* runs through program *B* with 50 seconds, where 20 and 30 seconds are for integer and floating computations respectively. Computer *A* is promoted by replacing a new CPU running faster by two times and three times in integer and floating point operations respectively. New computer *A* can run through program *B* faster than the old one by 2.5 times.

10. Given the values of registers $t0 and $t1 in the table below, which of following statements is **correct**.

$t0 = 0xAAAAAAAA
$t1 = 0x22222222

(a) For the initial values of registers in the table above, the value of $t2 will become 0x55555552 after the execution of code sequence below.

```
sll  $t2, $t0, 3
or   $t2, $t2, $t1
```

(b) For the initial values of registers in the table above, the value of $t2 will become 0x37777777 after the execution of code sequence below.

```
srl  $t2, $t0, 3
or   $t2, $t2, $t1
```

(c) For the initial values of registers in the table above, the value of $t2 will become 0xF7777777 after the execution of code sequence below.

```
srl  $t2, $t0, 3
or   $t2, $t2, $t1
```

(d) For the initial values of registers in the table above, the value of $t2 will become 0 after the execution of instruction below.

```
slt  $t2, $t0, $t1
```

(e) For the initial values of registers in the table above, the value of $t2 will become 1 after the execution of instruction below.

```
sltu  $t2, $t0, $t1
```

11. Suppose the program counter (PC) is at address 0x80000000, which of following statements is **incorrect**.

(a) It is possible to use one branch instruction to get to address 0x7fffff00
(b) It is possible to use one jump instruction to get to address 0x7fffff00
(c) It is possible to use one branch instruction to get to address 0x80000040
(d) It is possible to use one branch instruction to get to address 0x80010000
(e) It is possible to use one jump instruction to get to address 0x8fff0000

12. Consider the following sequence of actual outcomes for a branch, where ***T*** means the branch is taken, ***N*** means not taken, which of following statements is **incorrect**?

T-T-N-T-N-N-N-T-N

(a) It will be mispredicted *five* times if we always predict the branch outcomes as **taken**.
(b) It will be mispredicted *four* times if we always predict the branch outcomes as **NOT taken**.
(c) It will be mispredicted *four* times if a **1-bit** predictor is used and this predictor is initialized as taken.
(d) It will be mispredicted *five* times if **1-bit** predictor is used and this predictor is initialized as taken.
(e) It will be mispredicted *four* times if a **2-bit** predictor is used and this predictor is initialized as taken.

複選題，共 13 題，每題全對得 4 分，只答錯一個選項得 2 分，答錯兩個以上選項、或未答得 0 分。

13. Which of the following statements are correct?

(a) Java interpreter interprets the java bytecode operations one at a time.
(b) The CLR is the implementation of the .NET virtual machine. It interprets the Microsoft intermediate language instructions one at a time.
(c) You can use printf() function in the Linux system call implementation.
(d) Normal instructions for the virtual machine can execute directly on the hardware and only the privileged instructions must be simulated.
(e) Named pipes are referred to as FIFOs in UNIX systems. Once created, they appear as typical files in the file system.

14. When implementing the monitor with the signal and wait execution method, which of the following statements are *correct*? Assume for each monitor, a semaphore mutex (initialized to 1) is provided. Two semaphore variables next and x_sem are initialized to 0 and two integers next_count and x_count are initialzed to 0.

Each external procedure F is replaced by:	x.wait() is implemented as:	x.signal() is implemented as:

wait(mutex);
...
Body of F
...
if (next_count>0)
signal(next);
else
signal(mutex);
	x_count++;
	if (next_count>0)
	/* Line A*/
	else
	/* Line B*/
	wait(x_sem);
	x.count--;
		if (x_count>0) {
		next_count++;
		/* Line C*/
		wait(next);
		next_count--;
		}

(a) The statement of Line A is signal(mutex);
(b) The statement of Line B is signal(next);
(c) The statement of Line B is signal(mutex);
(d) The statement of Line C is signal(x_sem);
(e) The statement of Line A is wait(mutex);

15. Which of the following statements are *correct*?
(a) Absolute code can be generated if we know where the process will reside in memory at compile time.
(b) A logical address is generated by CPU while a physical address is an address seen by the memory unit.
(c) Inverted page table is very efficient in searching for a match but inefficient in space used for storing page tables.
(d) Paging may suffer from external fragmentation while segmentation may suffer from internal fragmentation.
(e) Paging is a memory-management scheme that allows the physical address space of a process to be noncontiguous.

16. Which of the following statements are *incorrect*?
(a) CPU utilization is low when thrashing happens. Therefore, when thrashing happens, we should increase the degree of multiprogramming.
(b) The Optimal page-replacement algorithm results in the lowest page-fault rate of all algorithms but is difficult to implement because it requires future knowledge.
(c) The copy-on-write mechanism decreases the used physical memory shared between two processes, of which one is parent and the other is child.
(d) For a memory-mapped file, we can use the memory read/write instructions to access its content.
(e) The page fault rate of a running process has nothing to do with the program structure of the running

process.

17. Consider a group of n users and each user shares a secret key with every other user using a symmetric cryptosystem. In other words, each pair of users will share a unique key. Choose the correct ones in the following statements:
(a) Each user need to keep n-1 keys.
(b) Each user need to keep n keys.
(c) The total number of different keys kept in the group is n(n-1)/2.
(d) The total number of different keys kept in the group is n(n-1).
(e) The total number of keys kept in the group is n(n-1).

18. In the RSA asymmetric cryptosystem,
$n = pq$;
$ed \bmod (p-1)(q-1) = 1$, where e is the public key, and d is the private key.
Encrypting plaintext: $C = M^e \bmod n$;
Decrypting ciphertext: $M = C^e \bmod n$;
Choose the correct statements:
(a) n is public information
(b) p is public information
(c) q must be a prime number
(d) M must be relatively prime to n
(e) (p-1)(q-1) is public information

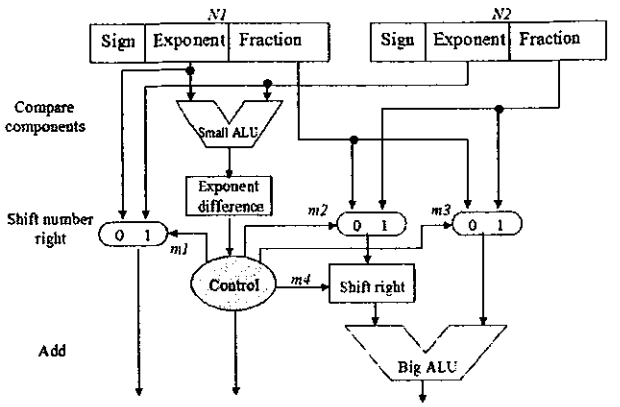
19. Each bit's carry out of a carry lookahead adder (CLA) is a function of each bit's *generate*, *propagate*, and *carry in* signals. Consider a two-level 9-bit CLA that is composed of several 3-bit CLA units with c_0 as the carry in and c_1 to c_9 as the carry outs. Each CLA unit realizes 3-bit group generate and group propagate functions based on 3-bit inputs. A signal is regarded validate if its value is correct; or, it is regarded as invalidate. Signals g_i and p_i are the *generate* and *propagate* signals at bit i while G_{i-j} and P_{i-j} are the *group generate* and *group propagate* signals associated with bits i to j. Assume all input signals have been available, which ones of the following statements are correct ?
(a) A number of 4 CLA units in total are required to assemble the two-level 9-bit CLA.
(b) Carry outs c_1 , c_2 and c_3 become validate earlier than other carry out signals.
(c) $G_{0-2} = g_2 + p_2g_1 + p_2p_1g_0$ and $P_{0-2} = p_2p_1p_0$.
(d) Carry outs c_4 and c_5 become validate earlier than c_6.
(e) Assume the delays of each *NOT*, isolated *AND*, *XOR*, *AND-OR* structure gates are 1, 2, 2, and 3 time units respectively, and the *sum* is realized by 2 *XOR* gates while the *propagate* is realized by a *XOR* gate. Then the longest delay of the 2-level 9-bit CLA is the 12 time units.

20. Which ones of the following statements are correct?
(a) The biased exponents in IEEE standard 754 demand signed number exponent comparison.
(b) The number with all bits in exponent and fraction fields being 1 is referred to as infinity in IEEE standard 754.

(c) The fraction and exponent parts of the smallest positive single precision denormalized number in IEEE standard 754 are both 0.

(d) The right figure shows partial design for the first three steps of a floating-point adder. Assume $N1=3.63\times10^{10}$ and $N2 = 2.28\times10^{7}$. $(m1,m2,m3,m4) = (0,1,0,3)$.

(e) Floating-point unit (FPU) was called co-processor before because CPU and FPU were manufactured into two independently chips. Currently modern CPU and FPU have been designed and integrated together in a single chip.



21. Which ones of the following statements are correct?

(a) Consider the code sequence {k=10; **while** (k >= 1) {$Dat[k] = Dat[k] + 2$; k-- ;}}; spatial locality occurs on accessing variable k.

(b) Consider the above code sequence; spatial locality occurs on accessing array Dat.

(c) Assume a compiler does not have any optimization technique; Consider two sequential code sequences: Code 1: **for** (i=0; i<$maxX$;i++) **for** (j=0; j<$maxY$;j++) $Dat[i][j]$++;
Code 2: **for** (j=0;j<$maxY$;j++) **for** (i=0; i<$maxX$;i++) $Dat[i][j]$++;
The performances of two sequential codes are the same since modern cache design has very high cache hit rate (almost near 100%) and thus memory access time can be reduced significantly.

(d) Consider 32-bit word-addressing and a 32-word (only data) direct-mapped cache with 4-word blocks. The address sequence for data accessing is (0, 40, 80, 340, 56, 68, 172, 348, 48, 80). A conflict miss occurs for the last access (address 80).

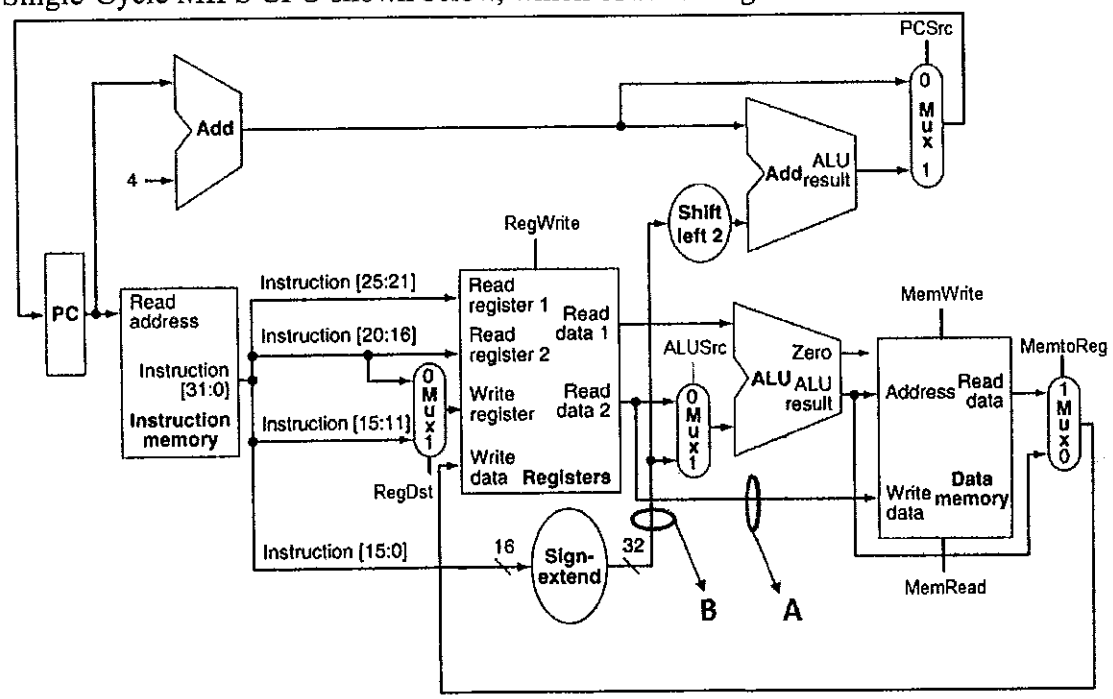
(e) Continue statement (d). If the cache size is increased by 4 words (36 words in total), a cache hit occurs for the last access (address 80). As compared to the accessing result of 36-word cache, the miss for the last access to the 32-word cache (in statement (d)) can be regarded as a capacity miss.

22. A system has a 16-bit virtual address size with 256B pages and a 16-bit byte addressing physical memory with physically index 2-way set associative data cache (LRU replacement policy) of 512B cache size and 16B blocks. The first six accesses to the page table are: **0x1332, 0xad58, 0x0162, 0x2ea9, 0x813d, 0x9f5a.** The system uses a single level page table. Assume the TLB and data cache are initially empty and their contents have been updated accordingly by the first six accesses (page table is shown below; VPN: virtual page number, PPN: physical page number). The CPU includes a fully associative TLB with 2 entries and an LRU replacement policy. Data reads from the following virtual addresses are performed (in the order listed): **0x813f, 0x136f, 0x2e5f, 0x9f50, 0x1370.** Which ones of following statements are correct?

VPN	PPN	VPN	PPN
0x01	0x27	0x81	0x8a
0x13	0x45	0x9f	0xcd
0x2e	0xe8	0xad	0x7e

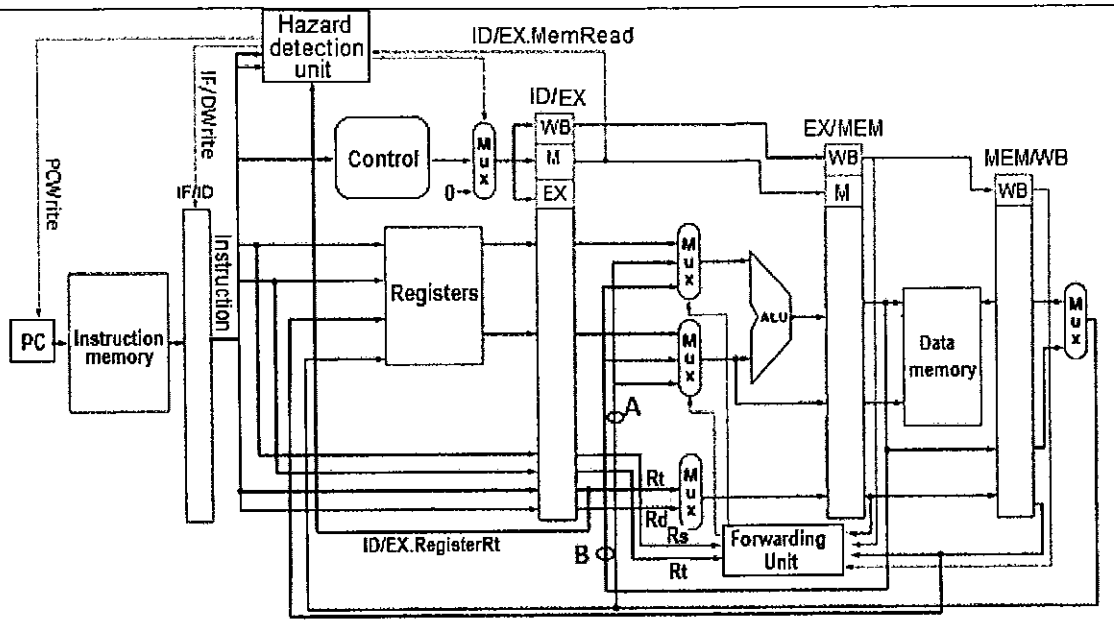
(a) The required numbers of bits for virtual page number and page offset in virtual address are all 8 bits.
(b) The required number of bits for index and tag in physical address are 4 and 8 bits respectively.
(c) Data access to 0x813f has access hit in TLB and cache.
(d) Data access to 0X9f50 has access miss in TLB and access hit in cache.
(e) Data access to 0X1370 has access miss in TLB and cache.

23. For the Single-Cycle MIPS CPU shown below, which of following statements are correct?



(a) If the path labeled A has been cut, the instructions **add**, **slt**, and **sw** still can run correctly.
(b) If the path labeled B has been cut, the instructions **lw**, **sw** and **beq** may fail.
(c) If the control signal *ALUsrc* is stuck on 0, the instructions **lw**, **sw**, and **beq** may fail to run correctly.
(d) If the control signal *RegDst* is stuck on 0, the instructions **lw** and **sw** still can run correctly.
(e) If the control signal *MemToReg* is stuck on 1, the instructions **add**, **sub**, **lw**, and **slt** may fail to run correctly.

24. Given the pipelined MIPS CPU below where assume both forwarding and stall mechanisms have been designed, which of following statements are correct?



(a) Assume the path labeled A has been cut, the following code snippet will fail.

```
add $s2, $s0, $s1
add $s3, $s0, $s2
```

(b) Assume the path labeled A has been cut, the following code snippet will fail.

```
add $t1, $t1, $s2
add $t1, $t0, $t2
add $s2, $s1, $t1
```

(c) Assume the path labeled B has been cut, the following code snippet will fail.

```
add $t1, $t1, $s2
add $t1, $t0, $t2
add $s2, $s1, $t1
```

(d) Assume the path labeled A has been cut, the following code snippet will fail.

```
lw  $s0, 4($t1)
add $s2, $s0, $s1
```

(e) Assume the path labeled B has been cut, the following code snippet will fail.

```
lw  $s0, 4($t1)
add $s2, $s0, $s1
```

25. Consider the code sequence below, where we predict **beq** as taken, but actually it is **NOT** taken, which of following statements are correct?

```
lw  $s0, 0($t0)
lw  $s1, 0($t0)
beq $s0, $s1, L1
add $s2, $s0, $s1
```

(a) For the pipelined MIPS CPU which has data forwarding mechanism and the branch outcome is determined in **MEM** stage, it takes *8* cycles to complete the execution of the above code sequence.

(b) For the pipelined MIPS CPU which has data forwarding mechanism and the branch outcome is determined in **MEM** stage, it takes *12* cycles to complete the execution of the above code sequence.

(c) For the pipelined MIPS CPU which has data forwarding mechanism and the branch outcome is determined in **ID** stage, it takes *7* cycles to complete the execution of the code sequence.

(d) For the pipelined MIPS CPU which has data forwarding mechanism and the branch outcome is determined in **ID** stage, it takes *11* cycles to complete the execution of the above code sequence.

(e) For the pipelined MIPS CPU which has data forwarding mechanism and the branch outcome is determined in **ID** stage, it takes *10* cycles to complete the execution of the above code sequence.