國立交通大學 104 學年度碩士班考試入學試題

科目：計算機系統(1003)　　考試日期:104 年 2 月 7 日 第 3 節

系所班別：資訊聯招　　第 1 頁,共 9 頁

【不可使用計算機】＊作答前請先核對試題、答案卷(試卷)與准考證之所組別與考科是否相符！！

一、單一選擇題，共 10 題，每一題答對給 4 分，未答得 0 分，答錯倒扣 1.5 分。請使用答案卡作答

1. Assume there are 1,000 processes of ProgramX (Figure 1) running on a system equipped with an Intel Core i5 processor. If we randomly pick one of the processes, which of the following CPU states (a~e as shown in Figure 1) is the most likely one that the process will be at?

```
int main()
{
    while(1);
    return 0;
}
```

Figure 1. ProgramX

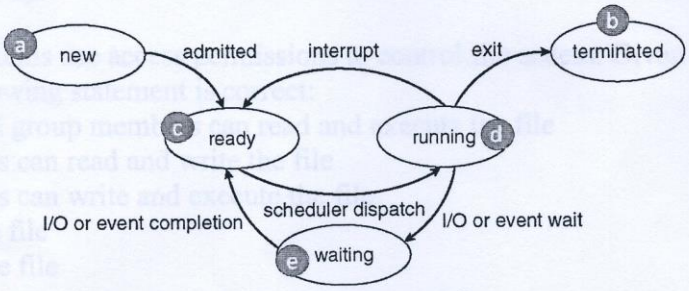

Figure 1. CPU scheduling state of a process

2. Which of the following inter-process communication mechanisms requires explicit synchronization in general?
   (a) Shared memory
   (b) Message queue
   (c) Signal
   (d) TCP/IP
   (e) Pipe

3. Which of the following statements about memory management is correct?
   (a) To allocate contiguous memory from free holes, the best-fit algorithm is the optimum solution in memory utilization.
   (b) Pure segmentation suffers from internal fragmentation.
   (c) A system can detect thrashing by using a figure, in which CPU utilization is plotted against the execution time.
   (d) For first-in-first-out page replacement, the page-fault rate will definitely not increase as the number of frames increases.
   (e) None of the above is correct.

4. Suppose that we use a three-level paging system, and it takes 20 ns to search the TLB (translation look-aside buffer) and the TLB hit ratio is 90 percent. The effective memory-access time by the probability is 202 ns. If we speed up the memory and the new memory access time is 50% of the original one (other conditions are the same), the new effective memory-access time is T ns. Please choose the correct value of "(round(T) mod 5)".
   (Hint: round(T) returns the nearest integer of T. You do not have to consider page faults.)
   (a) 0
   (b) 1

(c) 2
(d) 3
(e) 4

5. A large file M of size 3 Giga byes needs to be transferred from Alice to Bob over the Internet. Alice's RSA public key, secret key, one-time DES key are Kpa, Ksa, and Kda, respectively. Bob's RSA public key, secret key, are Kpb and Ksb, respectively. To achieve both confidentiality and authentication, what will be the best way for Alice to send the file M? $\{M\}_K$ represents the encryption of M using K. Checksum function is already embedded in the operations.
   (a) $\{\{M\}_{Ksa}\}_{Kpb}$
   (b) $\{\{M\}_{Kpb}\}_{Ksa}$
   (c) $\{\{M\}_{Kpb},\{Kda\}_{Kpb}\}_{Ksa}$
   (d) $\{\{M\}_{Kda},\{Kda\}_{Ksa}\}_{Kpb}$
   (e) $\{M\}_{Kda}, \{\{Kda\}_{Ksa}\}_{Kpb}$

6. Unix-like operating systems use access permissions to control file access. Given an access permission 0751, which of the following statement is correct:
   (a) Both the owner and group members can read and execute the file
   (b) The group members can read and write the file
   (c) The group members can write and execute the file.
   (d) Others can read the file
   (e) Others can write the file

7. Which of the following statement is *correct*?
   (a) Instructions *addi*, *beq*, and *j* (jump) all need to perform sign extension.
   (b) The most significant bit of 2's complement representation is the sign bit - a sign bit of 1 indicates a positive number.
   (c) The range of numbers represented by *n*-bit 2's complement is: $-(2^{n-1})+1 \sim \pm 0 \sim (2^{n-1})-1$.
   (d) Consider an addition of two 32-bit signed integers with a 32-bit ripple-carry adder, which consists of 32 1-bit full adders connected in series: if the carry-in and the carry-out of the most-significant-bit (MSB) full adder have different logic values, then there is an overflow due to the addition.
   (e) The operation of adding one very large positive integer and one very small negative integer may produce an overflow.

8. Which of the following statement is *correct*?
   (a) Pipelining improves the performance of a processor by decreasing the latency of a job (e.g., an instruction) to be done.
   (b) The more balanced pipeline stages a specific datapath has, the higher performance this pipelined datapath can achieve.
   (c) Every single instruction, when being executed in a *n*-stage pipelined datapath, consistently needs *n* clock cycles before its execution is completely done.
   (d) It is likely to have fewer hazards and less severe impact of hazards with deeper design of pipelining (i.e., more pipeline stage).
   (e) The number of pipeline stages monotonically grows with technology advance such as shrinking transistor size.

9. Which of the following statement is *correct*?
   (a) For write-back cache, both cache and memory will be updated on data-write hit.
   (b) For write-through cache, multiple writes within a block may require only one write to the memory.
   (c) Write-through is widely used in virtual memory in order to keep memory and disk consistent.

(d) First-level caches are more concerned about hit time, and second-level caches are more concerned about miss rate.
(e) Increase associativity may increase miss rate due to conflict misses

10. In a memory system, there is one TLB, one physically addressed cache, and one physical main memory. Assuming all memory addresses are translated to physical addresses before the cache is accessed. Which of the following events is *impossible* in memory system (Note: PT stands for page table)?
(a) TLB: hit, PT: hit, Cache: miss
(b) TLB: miss, PT: hit, Cache: hit
(c) TLB: miss, PT: hit, Cache: miss
(d) TLB: miss, PT: miss, Cache: miss
(e) TLB: hit, PT: miss, Cache: hit

二、複選題，共十題，每題全對得 4 分，答錯一個選項得 2 分，答錯兩個以上選項、或未答得 0 分。

11. Assume the processor of a Windows 8 laptop is executing some user-mode code. Which of the following events will cause a user-mode to kernel-mode transition (i.e. involving execution of kernel-mode code)?
(a) Process context switch
(b) Thread context switch (the threads are native Windows threads)
(c) Interrupt handling
(d) Open a file on the disk
(e) Page fault handling

12. Which of the following statements about file systems are correct?
(a) A remote directory can only be mounted over the root directory through the network file systems.
(b) Linked allocation does not suffer from external fragmentation.
(c) If the size of a block is 1024 bytes and a pointer require 32 bits, in a two-level index system, a file associated with a first-level index block can have a size of up to 256MB.
(d) Using on-line compaction can efficiently conquer the fragmentation problem of contiguous allocation.
(e) Compared with conventional lined allocation, caching the file-allocation tables (FAT) in memory can improve the efficiency of random access.

13. Which of the following statements are true?
(a) Smartphones normally do not have hard disk drives (HDDs).
(b) Solid state drives (SSDs) are replacing HDDs where speed, power consumption and durability are more important considerations.
(c) Secondary storage is normally non-volatile.
(d) Cloud storage has become a popular way for data storage.
(e) Wearable devices are normally equipped with hard disk drives to increase its storage space.

14. Which of the following are true?
(a) Android applications on Google Play (formerly known as Google Android Market) are trustworthy.
(b) Firewall can filter network traffic.
(c) Intrusion detection system (IDS) can analyze malicious network traffic.
(d) VPN (virtual private network) gateways can be used to establish confidential tunnels between two network gateways.
(e) Many routers are equipped with firewall and VPN functions.

15. Which of the following 32-bit *hexadecimal* data will have identical storage sequence in the (byte-addressable) memory no matter the machine is big-endian or little-endian?

(a) $AABBAABB_{hex}$
(b) $ABBAABBA_{hex}$
(c) $ABBBBBAB_{hex}$
(d) $ABCDCDAB_{hex}$
(e) $ABCDDCBA_{hex}$

16. Which of the following statements are *correct*?
(a) Given that every 1-bit ALU has a propagation delay of 1 unit, the cumulative propagation delay for an SLT (set-on-less-than) operation is 32 units in the worst case.
(b) The operation of 00110011 (multiplicand) * 11011011 (multiplier) based on the Booth's algorithm requires 2 additions and 3 subtractions.
(c) The Booth's algorithm is always better than traditional multiplication in terms of the total number of required additions and subtractions.
(d) $0.3125*2^{130}$ can be represented by the IEEE 754 single-precision floating-point standard format without any loss of accuracy.
(e) IEEE 754 double-precision floating-point representation is exactly 2X more precise than the single-precision counterpart.

17. Which of the following statements are *correct*?
(a) Trying to allow some instructions to take fewer cycles does not help, since the throughput is determined by the clock cycle; the number of pipeline stages per instruction affects latency, not throughput.
(b) Instead of trying to make instructions take fewer cycles, we should explore making the pipeline longer (deeper), so that instructions take more cycles, but the cycles are shorter. This could improve performance.
(c) A data hazard between two adjacent R-type instructions can always be resolved with forwarding.
(d) Perfect branch prediction (i.e., 100% prediction accuracy) combined with data forwarding would allow a processor to always keep its pipeline full.
(e) If we use an instruction from the fall-through (untaken) path to fill in a delay slot, we must duplicate the instruction.

18. Suppose you have a machine which executes a program spending 50% of execution time in floating-point multiply, 20% in floating-point divide, and 30% in integer instructions. Which of following statements are correct?
(a) If we make the floating-point divide run 3 times faster, the speedup relative to original machine is about 0.87.
(b) If we make the floating-point multiply run 8 times faster, the speedup relative to original machine is about 1.78.
(c) If we make both divide and multiply run faster as described in (a) and (b), the speedup relative to original machine is about 2.33.
(d) If we can make all the floating-point instructions run 15 times faster, the percent of floating-point instructions need to be about 90.36 in order to achieve a speedup 4.
(e) The rule stating that the performance enhancement possible with a given improvement is limited by the amount that the improved feature is used is called Moore's law.

19. Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 80MHz and M2 has a clock rate of 100MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as the table below. Which of following statements are correct (Note, the MIPS in these statements stand for Millions of Instruction Per Second)?

Instruction class	Machine M1 – Cycles/instruction class	Machine M2 – Cycles/instruction class	Frequency
A	1	2	60%
B	2	3	30%
C	4	4	10%

(a) The average CPI for M1 is 1.6
(b) The average CPI for M2 is 2.5
(c) M2 has higher MIPS rating than M1.
(d) If we change CPI of instruction class A for M2 to 1, M2 has higher MIPS rating than M1.
(e) If we increase the clock rate of M1 to 100MHz without affecting the CPI of A, B, and C. The speedup of M1 is 0.8.

20. Assume a 128KB direct-mapped cache with a 32-byte block. Consider a video streaming workload that accesses a 64KB working set sequentially with the following address stream: 0, 2, 4, 6, 8, 10, 12, 14, 16, …etc. Which of the following statements are correct?
(a) The miss rate is 1/32.
(b) All the misses are compulsory misses based on the 3Cs model.
(c) The miss rate is sensitive to the size of the cache.
(d) The miss rate is sensitive to the size of the working set.
(e) The miss rate is sensitive to the block size.

三、題組，共四個題組，題組內小題完全答對得 5 分，答錯任一小題或未作答得 0 分。題組 A 包含題號 21~23，題組 B 包含題號 24~28，題組 C 包含題號 29~33，題組 D 包含題號 34~38。

A. Consider the execution of the following set of processes on a single-core processor:

Process	Creation Time	Required Execution Time
P_1	0	30
P_2	10	10
P_3	20	20
P_4	20	10
P_5	90	10

21. Assume we use first-come-first-served (FCFS) scheduling. How long will it take for the four processes to complete?
(a) 60
(b) 70
(c) 80
(d) 90
(e) 100

22. Find a non-preemptive scheduling that minimizes the average waiting time. The minimal average waiting time is a two-digit number D_1D_0. Please select from the following the value of D_1.
(a) 0
(b) 1

(c) 2
(d) 3
(e) 4

23. Continue from previous question. Please select from the following the value of D_0.
(a) 1
(b) 2
(c) 3
(d) 4
(e) 5

B. A system provides users paging-based virtual-memory space of 2^{16} bytes, it has 3 physical frames and the page size is 2^{10} bytes. When a process accesses a sequence of the hexadecimal virtual addresses: 0x0A08, 0x012C, 0x05DF, 0x0722, 0x08A6, 0x0B33, 0x0428, 0x0CF2, 0x0160, 0x0D5F. The physical memory address of the last access "0x0D5F" is "X" by the LRU algorithm. $X/4= X_4*5^4+X_3*5^3+X_2*5^2+X_1*5^1+X_0$ ($0 \leq X_0, X_1, X_2, X_3, X_4 < 5$). Please choose the correct values of X_4, X_3, X_2, X_1, and X_0 in the following.

24. X_4=? (a) 4, (b) 3, (c) 2, (d) 1, (e) 0

25. X_3=? (a) 4, (b) 3, (c) 2, (d) 1, (e) 0

26. X_2=? (a) 4, (b) 3, (c) 2, (d) 1, (e) 0

27. X_1=? (a) 4, (b) 3, (c) 2, (d) 1, (e) 0

28. X_0=? (a) 4, (b) 3, (c) 2, (d) 1, (e) 0

C. Consider the following MIPS code in a 5-stage pipelined CPU (see Figure 1)

```
# memory address: instruction in the memory
36:  sub  $1, $4, $8
40:  beq  $1, $3, 7
44:  and  $12, $2, $5
48:  or   $13, $2, $6
...
72:  lw   $4, 50($7)
76:  add  $14, $4, $2
80:  slt  $15, $6, $7
...
```

Figure 2 shows the pipeline state (in clock cycle 3) when the branch instruction (beq $1, $3, 7) is in the ID stage. Assume that (*i*) this branch will be taken, (*ii*) branch outcome are to be determined in the ID stage, and (*iii*) although not shown in the figure, forwarding to the ID stage (from EX/MEM pipeline registers) is available.

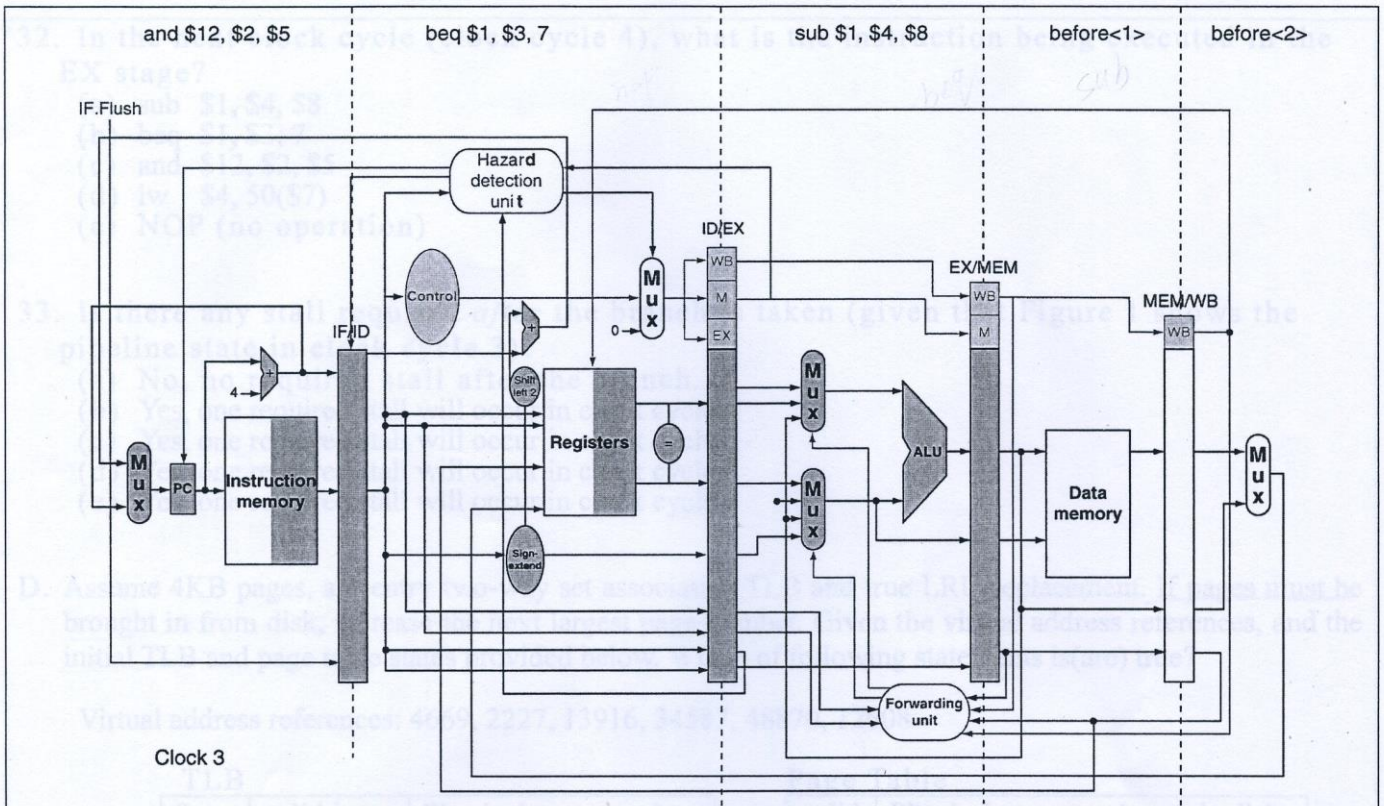

Figure 2: A pipeline datapath

29. In the next clock cycle (clock cycle 4), what is the output value of the ALU (for program counter addition) in the IF stage?
    (a) 40
    (b) 44
    (c) 48
    (d) 72
    (e) 76

30. In the next clock cycle (clock cycle 4), what is the output value of the ALU (for program counter addition) in the ID stage?
    (a) 40
    (b) 44
    (c) 48
    (d) 72
    (e) 76

31. In the next clock cycle (clock cycle 4), what is the instruction being executed in the ID stage?
    (a) sub $1, $4, $8
    (b) beq $1, $3, 7
    (c) and $12, $2, $5
    (d) lw $4, 50($7)
    (e) NOP (no operation)

32. In the next clock cycle (clock cycle 4), what is the instruction being executed in the EX stage?
(a) sub $1, $4, $8
(b) beq $1, $3, 7
(c) and $12, $2, $5
(d) lw $4, 50($7)
(e) NOP (no operation)

33. Is there any stall required *after* the branch is taken (given that Figure 1 shows the pipeline state in **clock cycle 3**)?
(a) No, no required stall after the branch.
(b) Yes, one required stall will occur in clock cycle 4
(c) Yes, one required stall will occur in clock cycle 5
(d) Yes, one required stall will occur in clock cycle 6
(e) Yes, one required stall will occur in clock cycle 7

D. Assume 4KB pages, a 4-entry two-way set associative TLB and true LRU replacement. If pages must be brought in from disk, increase the next largest page number. Given the virtual address references, and the initial TLB and page table states provided below. Which of following statements is(are) true?

Virtual address references: 4669, 2227, 13916, 34587, 48870, 12608

TLB

Set	valid	tag	Physical page number
0	0	11	12
0	1	3	6
1	1	7	4
1	0	4	9

Page Table

valid	Physical page number or in disk
1	5
0	Disk
0	Disk
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

34. For the given address references, list the corresponding virtual page numbers.
(a) 0, 0, 0, 2, 2, 0
(b) 1, 0, 3, 0, 3, 3
(c) 1, 0, 3, 8, 11, 3
(d) 0, 0, 1, 4, 5, 1
(e) 1, 0, 1, 0, 1, 1

35. For the given address references, the corresponding indexes to the TLB are
(a) 0, 0, 0, 2, 2, 0
(b) 1, 0, 3, 0, 3, 3
(c) 1, 0, 3, 8, 11, 3
(d) 0, 0, 1, 4, 5, 1

(e) 1, 0, 1, 0, 1, 1

36. For the given address references, the corresponding tags to the TLB are
(a) 0, 0, 0, 2, 2, 0
(b) 1, 0, 3, 0, 3, 3
(c) 1, 0, 3, 8, 11, 3
(d) 0, 0, 1, 4, 5, 1
(e) 1, 0, 1, 0, 1, 1

37. For the given reference, accesses to TLB are
(a) miss, miss, miss, miss, miss, miss
(b) miss, hit, miss, miss, miss, miss
(c) miss, miss, hit, hit, hit, hit
(d) miss, miss, miss, miss, miss, hit
(e) miss, hit, hit, miss, hit, hit

38. For the given reference, how many page faults in total?
(a) None
(b) 1
(c) 2
(d) 3
(e) 4