國立陽明交通大學 114 學年度碩士班考試入學招生試題

科目：計算機系統(含作業系統及計算機組織)(8103)

考試日期：114 年 2 月 6 日　第 3 節

系所班別：資訊聯招

【不可使用計算機】＊作答前請先核對試題、答案卷(試卷)與准考證之所組別與考科是否相符！！

一、複選題(80%)，共二十題，每題全對得 4 分，答對一個選項得 1 分(答對兩個選項得 2 分，以此類推)，答錯一個選項倒扣 1 分(答錯兩個選項倒扣 2 分，最多扣至本科目計算機系統 0 分為止)，整題未作答不給分。(舉例每題有 a、b、c、d 四個選項，某題答案為 a、b，而作答時選 a、b、c，則三個選項正確一個錯誤，該題得 3−1=2 分)

請使用答案卡作答

1. In virtual memory management, which of the following are features of paging?
   (a). To increase the size of the physical memory.
   (b). To divide a process's address space into fixed-size blocks and load only necessary pages into physical memory.
   (c). To reduce the CPU clock speed.
   (d). To prevent processes from accessing each other's memory spaces.

2. Which of the following statements on memory management is (are) true?
   (a). Managing memory via the slab allocator not only minimizes internal and external fragmentations but also efficiently handles the frequent allocation and deallocation of kernel objects.
   (b). As page tables are per-process data structures, the page table and the other register values (like the instruction pointer) are together stored in the process control block of each process.
   (c). The x86 64-bit CPU architecture currently provides a 48-bit virtual address with support for page sizes of 4 KB, 2 MB, or 1 GB. Larger page sizes help reduce the overhead of page table traversal.
   (d). After enabling the memory-management unit (MMU), the user program never accesses the real physical addresses. That is, the user program can only work on the virtual address space.

3. Which of the following statements on virtual memory is (are) true?
   (a). If the required page data is not in the memory, the user process raises a page fault and the CPU runs the page fault handler to transfer the corresponding data into the memory.
   (b). Adopting copy-on-write during process creation allows the parent and child processes initially to share the same pages. If either process writes to a shared page, a copy of the page is created.
   (c). In Linux, the swap space is used for pages not associated with a file (known as anonymous memory); these pages include the stack and heap for a process.
   (d). In x86 systems, when a CPU encounters a virtual address that results in a TLB miss, the operating system performs page table walking for translating a virtual address to a physical address.

4. Which of the following statements on process is (are) true?
   (a). A process control block serves as the repository for all the data needed to start, or restart, a process. It contains scheduling information, local variables and kernel data structure.
   (b). Interrupts cause the operating system to change a CPU core from its current task and to run a kernel routine. The system needs to save the current context of the process running on the CPU core so that it can restore that context when its processing is done.
   (c). Traditional UNIX systems identify the init process as the root of all child processes. In UNIX systems, a process clones itself to create new processes. Thus, all the processes in the system are the descendants of the init process , either directly or indirectly.

(d). A user program must use system calls to access files stored in storage devices. But a program can directly access the allocated heap data from memory without the help from operating systems.

5. Consider a system with the following resource allocation state. There are five processes P1~P5 and three resource types. The resource allocation tuple (x, y, z) means x instances of resource type 1, y instances of resource type 2, and z instances of resource type 3.

Process	Max Demand	Allocated	Available
P1	(7, 5, 3)	(0, 1, 0)	(3, 3, 2)
P2	(3, 2, 2)	(2, 0, 0)	
P3	(9, 0, 2)	(3, 0, 2)	
P4	(2, 2, 2)	(2, 1, 1)	
P5	(4, 3, 3)	(0, 0, 2)	

Given the current system state, which of the following is/are true when checking the safety of granting Process P2 a request of (1, 0, 1) according to the Banker's Algorithm?

(a). After granting the request, the system will remain in a safe state.
(b). If the system enters an unsafe state, there is still the possibility that no deadlock will actually occur.
(c). There are enough resources available to grant the request.
(d). The current system state is unsafe.

6. Which of the following statements are true regarding interrupt handling in operating systems?

(a). Interrupts are signals that inform the processor of an event that needs immediate attention.
(b). Interrupts can only be generated by hardware, not software.
(c). When an interrupt occurs, the processor stops executing the current program and transfers control to the interrupt handler.
(d). Interrupts are prioritized, meaning the operating system may choose to delay handling a lower-priority interrupt in favor of a higher-priority one.

7. Following is the memory map of the Linux utility program `/usr/bin/cat`. Which of the following statement(s) is/are true?

```
00400000-0040b000 r-xp 00000000 fd:01 1234567  /usr/bin/cat
0060a000-0060b000 r--p 0000a000 fd:01 1234567  /usr/bin/cat
0060b000-0060c000 rw-p 0000b000 fd:01 1234567  /usr/bin/cat
00e7a000-00e9b000 rw-p 00000000 00:00 0        [heap]
7f8b6c000000-7f8b6c021000 rw-p 00000000 00:00 0
7f8b6c021000-7f8b70000000 ---p 00000000 00:00 0
7f8b71a8d000-7f8b71aa3000 r-xp 00000000 fd:01 2345678  /lib/x86_64-linux-gnu/libgcc_s.so.1
7f8b71aa3000-7f8b71ca2000 ---p 00016000 fd:01 2345678  /lib/x86_64-linux-gnu/libgcc_s.so.1
7f8b71ca2000-7f8b71ca3000 r--p 00015000 fd:01 2345678  /lib/x86_64-linux-gnu/libgcc_s.so.1
7f8b71ca3000-7f8b71ca4000 rw-p 00016000 fd:01 2345678  /lib/x86_64-linux-gnu/libgcc_s.so.1
7ffc445e7000-7ffc44608000 rw-p 00000000 00:00 0        [stack]
7ffc446da000-7ffc446dd000 r--p 00000000 00:00 0        [vvar]
7ffc446dd000-7ffc446df000 r-xp 00000000 00:00 0        [vdso]
ffffffffff600000-ffffffffff601000 --xp 00000000 00:00 0        [vsyscall]
```

(a). The CPU architecture is 32-bit.
(b). The program contains C library code.
(c). If we put shellcode on a buffer allocated by `malloc()`, the shellcode will be non-executable.
(d). The program has three child processes.

8. Which of the following statements about the Round Robin (RR) scheduling algorithm is/are correct?

(a). It can lead to starvation of certain processes.
(b). It ensures quicker process completion for all processes.
(c). Decreasing the RR time quantum will increase the turnaround time.
(d). It ensures that all processes receive equal CPU time.

9. Which of the following statements on process scheduler and thread is (are) true?

(a). Context switching is typically faster between threads than between processes. The reason is that threads share resources, including page table and user stack, of the process to which they belong.
(b). In Linux, Completely Fair Scheduler (CFS) allocates a larger time quantum to higher-priority processes. Processes with the same priority will receive the same time quantum.
(c). The dispatcher involved in the process scheduler switches process contexts between the current and the next-scheduled user processes in the user mode so as to minimize the dispatching latency.
(d). In contrast, during thread creation, the new thread shares many data structures (like memory space and file descriptors) with the parent process instead of copying them.

10. Which of the following statements on I/O system is (are) true?

(a). For most computers, the bootstrap is stored in Non-Volatile Memory (NVM) flash memory firmware on the system motherboard and mapped to a known memory location.
(b). In Linux, if the requested file is not already open, the directory structure is searched to locate the file by its name. The directory structure may reside in the memory or on the storage devices.
(c). In Linux, page cache usually caches file in DRAM because DRAM is faster than storage devices and data can be retained in DRAM after the system powers down.
(d). To concurrently support multiple types of file systems, Virtual File System (VFS) layer separates file-system-generic operations from their implementation by defining a VFS interface.

11. In a pipelined processor, a program has 5% instructions belonging to load and store instructions. This program spends 20% of its execution time for load instructions and 10% of its execution time for store instructions. Since the data cache miss rate is high shown in this program, the processor architect proposes a new data cache architecture that improves the 4x execution time of load instructions (4x faster) and 2x execution time of store instructions (2x faster). Then, this new processor will achieve 1.25x speedup. Which statements are correct when using the processor with this new cache architecture?

(a) This new cache architecture helps the increase of processor's clock frequency
(b) The value of cycle per instruction (CPI) becomes small after using this new cache architecture in the processor
(c) This new cache architecture increases the instruction counts (ICs)
(d) This new cache architecture helps the reduction of the cache miss penalty

12. Given a pipelined processor that includes a directed-mapped data cache where the length of memory

address is 32 bits. The size of tag, index, and offset fields in such a directed-mapped data cache are 26 bits, 4 bits, and 2 bits for each. This processor executes the program 1 and observes its cache miss rate is high. What kind of cache misses causes such a problem when using a directed-mapped cache in this processor?

```
        addi    $t0     $0          3
loop:   beq     $t0     $0          done
        lw      $t1     0x4($0)
        lw      $t2     0x8($0)
        lw      $t3     0xC($0)
        lw      $t4     0x10($0)
        addi    $t0     $t0         -1
        j       loop
done:
```

Program 1

(a) Compulsory cache miss
(b) Conflict cache miss
(c) Capacity cache miss
(d) Cold start cache miss

13. A data cache usually has multiple cache blocks. The set-associative cache includes tag, index, and offset fields to manage each cache block. What are impacts when increasing the size of cache blocks in a data cache?

(a) The large cache block facilitates the usage of temporal locality on the data cache
(b) Large cache miss penalty
(c) Reducing the tag overhead
(d) Decreasing the cache miss rate

14. A data cache in a processor employs 2-way set associative cache where the word size is 32 bits. The size of tag, index, offset fields in this set associative cache are 26 bits, 4 bits, and 2 bits for each. Which statements are correct when this processor executes the program 2?

```
        addi    $t0     $0          4
loop:   beq     $t0     $0          done
        lw      $t1     0x6($0)
        lw      $t2     0x46($0)
        addi    $t0     $t0         -1
        j       loop
done:
```

Program 2

(a) The cache miss rate is 25%
(b) Increasing the size of the cache can reduce the cache miss rate
(c) The cache miss rate will be increased when using the directed-mapped cache where its tag, index,

and offset is 27 bits, 3 bits, and 2 bits for each.

(d) The cache miss rate will be increased when using the fully associative cache

15. A processor runs at 4 GHz and has a CPI of 1.4 without including the stall cycles due to cache misses. Load and store instructions count 30% of all instructions. The processor has an I-cache and a D-cache. The hit time is 1 clock cycle. The I-cache has a 3% miss rate. The D-cache has a 5% miss rate on load and store instructions. The miss penalty is 50 ns, which is the time to access and transfer a cache block between main memory and the cache. Which following statement are correct?

(a) The miss penalty of this processor is 200 clock cycles
(b) The average memory access time (AMAT) for instruction access is 6 clock cycles
(c) The number of stall cycles per instruction is 10 clock cycles
(d) The overall IPC of this processor is 0.096

16. Which of the following statements are true?

(a) In 2's complement, the value 0 has a unique representation
(b) In IEEE 754 single-precision format, the value 0 has two different representations.
(c) Overflow will never occur when adding two 2's complement numbers of different signs.
(d) Storing the 32-bit number 0xABCDDCBA in memory results in the same outcome regardless of whether little endian or big endian is used.

17. Given an IEEE754 single-precision representation format in the table below and the bias value as 127. Which of the following statements are correct?

(a) The number $-1.1_2 \times 2^{-1}$ has the single precision representation as:
Sign = -1, Exponent = $0111\ 1110_2$, Fraction = $100\ 0000\ 0000\ 0000\ 0000\ 0000_2$
(b) The number $101.1_2 \times 2^{-131}$ has the single precision representation as:
Sign = 0, Exponent = 00000000_2, Fraction = $001\ 0110\ 0000\ 0000\ 0000\ 0000_2$
(c) The smallest positive single-precision normalized number is: $1.0_2 \times 2^{-126}$.
(d) The smallest positive single-precision denormalized number is: $1.0_2 \times 2^{-127}$.

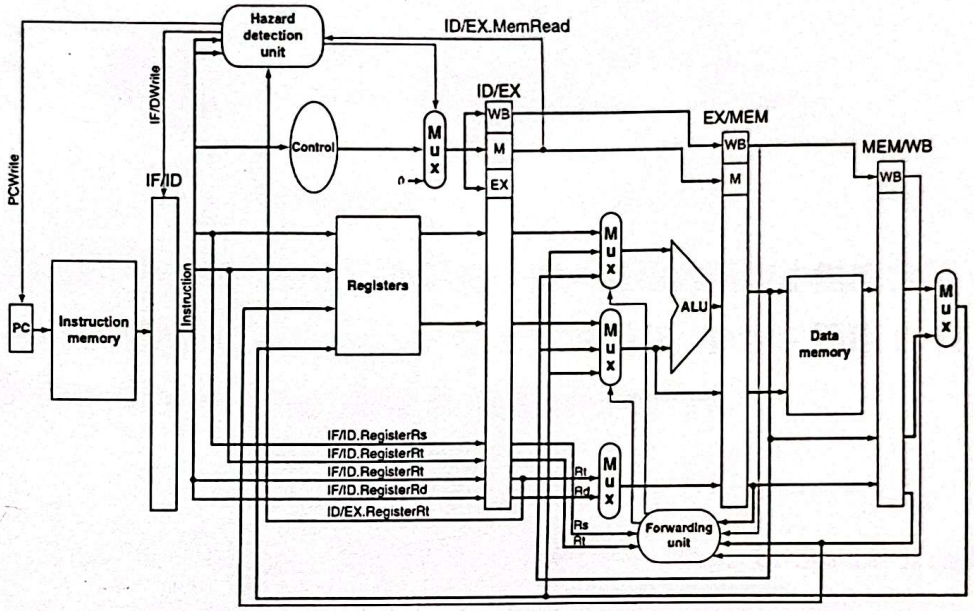
	8 bits	23 bits
S	Exponent	Fraction

Values (single precision)		Meaning
Exp.	Fraction	
0	0	0
0	Non-zero	+/- de-normalized number
1-254	Anything	+/- floating-point number
255	0	+/- infinity
255	Non-zero	NaN (Not a number)

18. Consider the execution of the following code on the 5-stage pipelined processor. The processor has both the hazard detection unit and the forwarding unit for data hazard. Assume that the following code sequence executes starting from clock cycle 1. At clock cycle 8, where do the two ALU inputs come from?

(a) both are from ID/EX
(b) one from ID/EX and one from EX/MEM
(c) one from ID/EX and one from MEM/WB
(d) one from EX/MEM and one from MEM/WB

```
add x28, x31, x29
ld x31, 32(x29)
and x30, x29, x31
sd x5, 20(x30)
sub x5, x5, x30
or x29, x29, x30
```



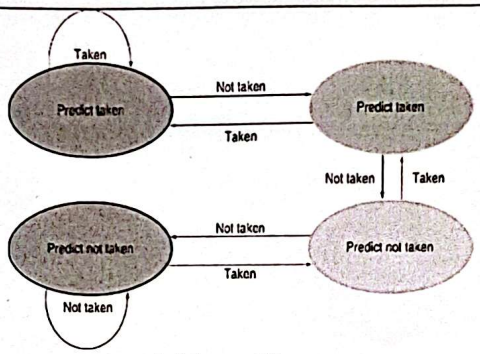
The pipelined processor

19. Consider a pipeline CPU with five stages: IF, ID, EX, MEM, WB. Stall cycles due to mis-predicted branches increase the CPI of pipeline. Given a code sequence with instruction mix as: R-type: 50%, beq: 25%, lw & sw: 25%. Assume branch prediction accuracy is 20% and there are no data hazards and cache misses. It is clear that the system suffers from extra CPIs due to mis-predicted branches. Which of the following statements about the extra CPI are correct?

(a) The extra CPI is 0.4 if the mis-predicted branch outcomes are corrected in MEM stage.
(b) The extra CPI is 0.6 if the mis-predicted branch outcomes are corrected in MEM stage.
(c) The extra CPI is 0.4 if the mis-predicted branch outcomes are corrected in ID stage.
(d) The extra CPI is 0.2 if the mis-predicted branch outcomes are corrected in ID stage.

20. Consider the 2-bit predictor shown in the Figure below, and assume the predictor starts at the top-left state (i.e., the "strongly predict taken" state). Given the branch outcome sequence: N, T, N, N, T, (where T = taken, N = not-taken), which of the following statements are correct?

(a) The accuracy rate is 1/5
(b) The overall accuracy rate is 2/5 if the pattern repeats twice (i.e., N, T, N, N, T, N, T, N, N, T).
(c) The overall accuracy rate is 1/3 if the original pattern repeats three times.
(d) The overall accuracy rate is about 1/3 if the original pattern repeats 10000 times



2-bit predictor

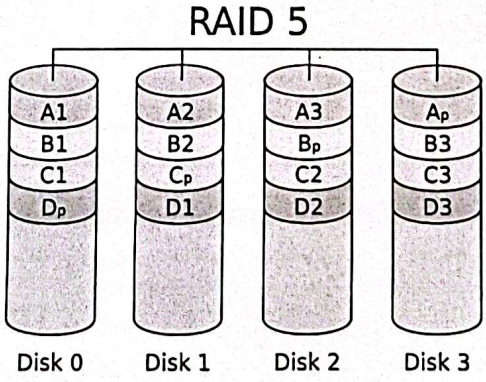
二、題組(20%)，共四個題組，各題組下的小題為單選，每一題組內所有小題完全答對得 5 分，答錯任一小題或未作答得 0 分。題組 A 包含題號 21~24，題組 B 包含題號 25~27，題組 C 包含題號 28~30，題組 D 包含題號 31~34

請使用答案卡作答

題組 A

Consider the following RAID 5 configuration using four identical disks (Disk 0–3). The specification of each disk is

Capacity: 1 TB
Read throughput: 100MB/s
Write throughput: 100MB/s.



21. How much data can be stored in the disk array?

(a). 1TB
(b). 2TB
(c). 3TB
(d). 4TB

22. What is the maximum read throughput when an application reads data from the disk array?

(a). 100 MB/s
(b). 200 MB/s

(c). 300 MB/s
(d). 400 MB/s

23. What is the maximum number of failed disk(s) that can be tolerated?

(a). 0
(b). 1
(c). 2
(d). 3

24. Assume that none of the disk data is cached in the memory. What is the minimum number of disk(s) that need to be involved in a write to the disk array?

(a). 1
(b). 2
(c). 3
(d). 4

題組 B

Assuming a custom CPU adopting multi-level page tables, where the page size, virtual address space size and the page table entry size are set to 32KB, 2^{64}B, 16B, respectively. This custom CPU only has one register to hold the physical address of the topmost level of the multi-level page tables.

25. What is the minimum level of this multi-level page tables?

(a). 3
(b). 4
(c). 5
(d). 6

26. If the number of levels is set to the minimum, what is the maximum number of pages in the bottom level?

(a). 2^{39}
(b). 2^{38}
(c). 2^{37}
(d). 2^{36}

27. If the number of levels is set to the minimum, how many pages are there in the top level?

(a). 4
(b). 3
(c). 2
(d). 1

題組 C

A pipelined processor contains 64 KB L1 data cache, where the length of memory address is 32 bits, the block size is 64 bytes. This data cache employs 4-way set associative cache architecture. The size of physical memory on this processor is 4 GB.

28. How many cache blocks are having in the 64 KB L1 data cache?

(a) 0.5K cache blocks
(b) 1K cache blocks
(c) 1.5K cache blocks
(d) 2K cache blocks

29. How many bits are used in tag of such a data cache?

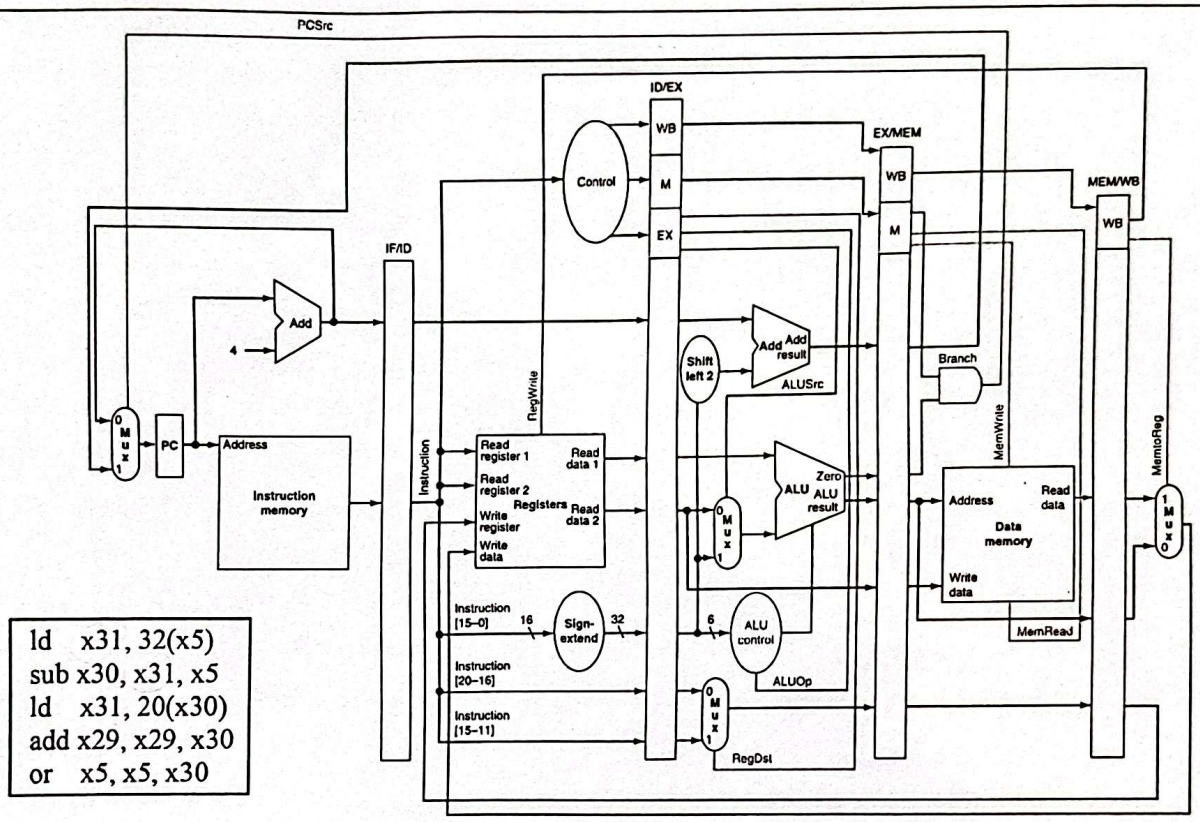
(a) 14 bits
(b) 15 bits
(c) 17 bits
(d) 18 bits

30. Which fields in the data cache will be increased when increasing the length of memory address from 32 bits to 64 bits?

(a) Tag
(b) Index
(c) Offset
(d) Valid bit

題組 D

Consider the execution of the following code on a 5-stage pipelined processor, shown in the Figure below. Note that the processor includes both a hazard detection unit and a forwarding unit for data hazard, though these components are not shown in the figure. Assume the code sequence starts execution at clock cycle 1. Please answer the following questions.



The 5-stage pipelined processor

31. What instruction is in the EXE stage at clock cycle 5?
    (a) ld
    (b) sub
    (c) add
    (d) bubble

32. What instruction is in the MEM stage at clock cycle 5?
    (a) ld
    (b) sub
    (c) add
    (d) bubble

33. What instruction is in the WB stage at clock cycle 5?
    (a) ld
    (b) sub
    (c) add
    (d) bubble

34. What are the values of signals ALUsrc and MemToReg, respectively, at clock cycle 5?
    (a) 0,0
    (b) 0,1
    (c) 1,0
    (d) 1,1