

# Dylan Stow

Ph.D Candidate, University of California at Santa Barbara (UCSB)  
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U.S. Citizen

## Education

2015 - Present	<b>University of California, Santa Barbara</b> Ph.D. Candidate in Electrical and Computer Engineering M.S. in Electrical and Computer Engineering (2017) Major: Computer Architecture Minor: Very Large Scale Integration (VLSI) and Computer Aided Design (CAD) Advisor: Yuan Xie GPA: 4.0	<b>Santa Barbara, CA</b>
2009 - 2013	<b>Harvey Mudd College</b> B.S in Engineering Humanities Concentration: Economics Advisor: David M. Harris GPA: 3.64	<b>Claremont, CA</b>

## Professional Experience

2013 - 2015	<b>Advanced Micro Devices (AMD)</b> Design Engineer I/II, high-performance microprocessor circuit design for Zen core	<b>Fort Collins, CO</b>
<b>Primary role:</b> VLSI physical design lead for Zen floating point datapath Design closure for setup time, hold time, low power, correctness, and yield Trailblazing of new EDA methodology and state-of-the-art process technologies		
<b>Secondary role:</b> Floating point component lead Management of timing closure and correctness for full floating point unit Primary team contact between other design and methodology teams		

## Research Summary

Dylan Stow's research interests include the areas of computer architecture, VLSI circuit design, machine learning, and design automation. Dylan has an interdisciplinary educational background that includes electrical engineering, computer science, and economics, as well as 2 years of professional engineering experience as a physical design engineer at AMD. His current research interests are (1) Architecture and design for emerging die-integration packaging methodologies (e.g. 3D, 2.5D, FOWLP) with a focus on cost-driven design, IP reuse, and die-stacked memory architecture, (2) Hardware security, with an emphasis on side-channel masking and secure manufacturing, and (3) Deep learning-based design automation for physical design circuit optimization. Previously, he researched floating point microarchitectures for Intel and Oracle Labs and near-threshold CMOS cell design for yield-driven ultra-low power circuits.

**Software Proficiencies:** Linux, Synopsys CAD, SPICE, GPGPU-Sim, gem5, DRAMPower, McPAT, CACTI, NVSim, Xilinx Vivado and SDK, Altera Quartus, Labview, TensorFlow, PyTorch, Matlab, Mathematica, Microsoft Office

**Computer Languages:** SystemVerilog HDL, C/C++, Python, Java, Perl, Tcl, OpenGL, CUDA, MIPS/x86/ARM, SQL

## Research Projects

**Deep Learning-Assisted Architecture and Design Optimization** (*EDA, Machine Learning, Architecture, since 2018*)  
Non-recurring costs for integrated system design and circuit optimization have steeply increased over the last decade as systems have grown in scope and heterogeneity and transistor size has shrunk. To combat this trend, recent advances in machine learning, namely deep neural networks and reinforcement learning, may be employed to automate engineering tasks like design exploration, global route optimization, and partition management. These methods may be able to extract semantic information from hardware description language to perform post-placement optimization beyond the capability of traditional automation methodologies.

**Architectures for Future Die-Stacked Memories** (*Comp. Architecture, Circuit Design, EDA, since 2017*)

To improve bandwidth, latency, capacity, efficiency, and footprint, 3D die-integration has recently been adopted to package greater amounts of memory within close proximity of the processor die. To better guide the development of the next generations

of die-stacked memories, this work developed a validated architectural memory power model to understand fine-granularity thermal and power constraints of the stacked memory layout for real HPC workloads. This research has also investigated the impact of reduced-latency memory configurations on GPU compute efficiency, leading to GPU microarchitecture restructuring.

- *Three papers pending submission and review.*

### **3D/2.5D Integrated Circuit Design and Cost Analysis** (*Comp. Architecture, Circuit Design, EDA, since 2015*)

Die-stacked 3D packaging and interposer-based 2.5D packaging offer continued transistor count scaling, increased system integration, and heterogeneous process integration. However, wide-spread adoption of these technologies requires cost-effectiveness that accounts for the increased thermal challenges and performance optimization. This work explores cost-driven design strategies and the novel architectures that are enabled through design reuse and expanded integration opportunities, with emphasis on high performance, scalable processors.

- *GOMACTech'18*
- *ICCAD'17*
- *ICCAD'16*
- *ISVLSI'16*

### **Hardware Security** (*Circuit Design, since 2015*)

Modern encryption algorithms and other secure computations are vulnerable to information leakage from their hardware implementations, which can reveal calculations or stored keys through side-channels. Hardware techniques, including 3D die stacking, can be used to prevent side-channel leakage through thermal, EM, and power channels. Die stacking technology can also be leveraged for split fabrication to secure circuit IP against reverse engineering attacks when manufacturing through untrusted foundries.

- *GOMACTech'18*
- *GLSVLSI'17*
- *GLSVLSI'16*
- *ICCD'16*

### **Near-Threshold Voltage Cell Design** (*EDA, 2011-2013*)

Ultra-low power devices in the Internet of Things will require circuit-level techniques to minimize power and preserve batteries and harvested energy. This project investigates standard cell design under yield constraints in the near-threshold and sub-threshold voltage range to minimize active power.

- *Asilomar '12.*

## **Industry Projects**

### **AMD: Power modeling of 3D HBM memory for exascale systems** (*Comp. Architecture, Circuit Design, 2017*)

Development of validated power models for 3D High Bandwidth Memory technologies. Projection of future memory standard power, based on discussion with key memory vendors, to provide design insight into future exascale node architectures. Trace-based power analysis of key exascale workloads. Related publications are in development.

### **Qualcomm: Ultra-Low Power Embedded Deep Learning Acceleration with 3D-Integrated MRAM** (*Comp. Architecture, Machine Learning, Circuit Design, 2016*)

Self-directed summer research project with the goal of reducing energy cost of deep neural network inference to ultra-low power levels and chip area necessary for emerging embedded devices. Weight storage power reduction achieved with 3D integration of STT-MRAM for high density, low read energy, and minimal leakage power.

### **Intel: Fused Multiply-Add Division Microarchitecture** (*Circuit Design, 2012-2013*)

Team leader for a one year project to optimize a IEEE-compliant floating point unit for low latency division algorithms. Project deliveries includes multiple SystemVerilog microarchitectures with different performance/area tunings. Final designs were verified for full IEEE compliance with full denormal and special case support. The designs were tailored for the limited energy/area of Intel's Knights Corner many-core architecture.

### **Oracle Labs: Oracle NUMBER Adder Microarchitecture** (*Circuit Design, 2012*)

Design project to develop adder hardware architectures for the Oracle NUMBER floating point format employed in Oracle SPARC servers. Personally implemented a minimum-area multicycle adder microarchitecture. Final designs were verified and synthesized to provide Oracle with area and power projections.

### **Viasat: Embedded Heater Research and Design** (*2012*)

Team leader on an interdisciplinary research and development project for new PCB heater technology used in extreme environments. Delivered highly improved design process with research report and software design tool.

## Cricket Communications: Verification Tool for Mobile Message Protocols (2011)

Development of Perl application with GUI to perform cellular device testing. The project resulted in improved productivity for the Device Engineering team during product debugging.

## Teaching Experience

Spring 2017 Lead Teaching Assistant and Substitute Lecturer - *ECE152A: Digital Design Principles*  
Fall 2016 Guest Lecturer - *ECE594BB: Advanced Topics in Computer Engineering*  
Spring 2016 Teaching Assistant - *ECE152A: Digital Design Principles*

## Awards and Honors

2017 ICCAD Best Paper Nomination  
2017 NSF Graduate Research Fellowship: Honorable Mention  
2015 AMD Spotlight Award Winner  
2013 Graduation with Distinction  
2013 Harvey S. Mudd Merit Award  
2012 ASHMC Student Council and Dorm President

## Publications

- [1]. Xing Hu, **Dylan Stow**, Yuan Xie “Die Stacking Is Happening” *IEEE Micro*, 2018.
- [2]. **Dylan Stow**, Yuan Xie “Navigating the Die-Integration Design Space: System Yield and Cost Analysis of 3D and 2.5D Packaging.” *Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, 2018.
- [3]. Peng Gu, **Dylan Stow**, Yuan Xie “Circuit Obfuscation and Thermal Side-Channel Masking using 3D Die-Stacking.” *Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, 2018.
- [4]. **Dylan Stow**, Yuan Xie, Taniya Siddiqua, Gabriel H. Loh “Cost-Effective Design of Scalable High Performance Systems using Active and Passive Interposers.” *Proceedings of the 2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2017. **Best Paper Nomination**.
- [5]. Jaya Dofe, Peng Gu, **Dylan Stow**, Qiaoyan Yu, Eren Kursun, Yuan Xie “Security Threats and Countermeasures in Three-Dimensional Integrated Circuits.” *Great Lakes Symposium on VLSI (GLSVLSI)*, 2017.
- [6]. **Dylan Stow**, Itir Akgun, Russell Barnes, Peng Gu, Yuan Xie “Cost Analysis and Cost-Driven IP Reuse Methodology for SoC design Based on 2.5D/3D Integration.” *Proceedings of the 2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2016.
- [7]. Peng Gu, **Dylan Stow**, Russell Barnes, Eren Kursun, Yuan Xie “Thermal-aware 3D Design for Side-channel Information Leakage.” *the 34th IEEE International Conference on Computer Design (ICCD)*, 2016.
- [8]. **Dylan Stow**, Itir Akgun, Russell Barnes, Peng Gu, Yuan Xie “Cost and Thermal Analysis of High-Performance 2.5D and 3D Integrated Circuit Design Space.” *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2016.
- [9]. Peng Gu, Shuangchen Li, **Dylan Stow**, Russell Barnes, Liu Liu, Eren Kursun, Yuan Xie “Leveraging 3D Technologies for Hardware Security: Opportunities and Challenges.” *Great Lakes Symposium on VLSI (GLSVLSI)*, 2016.
- [10]. Max Korbel, **Dylan Stow**, Craig R. Ferguson, David Money Harris “Yield-Driven Minimum Energy CMOS Cell Design.” *Asilomar Conference on Signals, Systems and Computers (ASILOMAR)*, 2012.

## Personal Interests

Dylan is a curious, lifelong learner that is passionate about a number of technical and social subjects. Much of his personal reading and self-education centers around the field of bio-inspired algorithms, including the topics of genetic algorithms, artificial life simulation, and especially neuro-inspired learning algorithms (both traditional deep neural networks for image recognition and natural language processing as well as bio-inspired spiking neuromorphic networks). Much of his education in this field is self-developed through Coursera, podcasts, books, the reading of >200 research papers, and personal project work on deep network training and pruning in TensorFlow.

Dylan is additionally interested in the economics and social implications of the semiconductor and artificial intelligence industries, including potential applications for the modern medical community. He collaborates on research with his wife and surgeons at the University of Colorado and University of Toronto to apply computational methods to assist in the diagnosis and study of pediatric craniofacial surgery. These tools are currently being applied to collect new machine learning datasets, which will then be used to train novel tools that will better guide surgical decisions for craniofacial syndromes. Because

reconstructive surgery has subjective success criteria, these tools will capture public and expert sentiment to provide better outcome guidance than classical measurement-based metrics.

When not engaged in academic work, Dylan is a prolific chef (for his busy M.D. wife), hiker, soccer player, rock climber, gardener, and father to a wonderful daughter and two lovable dogs.