Subject Code-(BEC-207)

B.TECH. Year: 2nd Semester: 3rd
MINOR TEST (EXAMINATION): 2025-2026
Digital Electronics

Time: 2 Hr. **Max. Marks: 20**

Note- Answer all questions

Q1.		Attempt any **Two** parts of the following.	Marks	CO	BL	PO	PI Code
	a)	What do you understand by Universal logic gates? Define truth table and expression for the XOR and XNOR gates. Implement XOR and XNOR gates by using NAND and NOR gates.	4	CO1	3	PO1	1.3.1
	b)	What are the different Boolean laws in digital logic design? Explain duality theorem with example. Prove that ABCD + ABC'D' + ABCD' + ABC'D + ABCDE + ABC'D'E' + ABC'DE can be simplified to A*B.'	4	CO1	4	PO1	1.3.1
	c)	What is significance of Priority encoder over normal encoder? Explain 4:2 Priority encoders with the help of its truth table, logical expression and logic diagram.	4	CO2	4	PO1	1.3.1
Q2.		Attempt any **Two** parts of the following.					
	a)	Convert the following numbers as indicated: (F3A7C2)16 to binary, decimal and octal Decimal (23.15) to BCD Binary equivalent of (43.85). Hexadecimal equivalent of (92.20). Octal equivalent of (53.55).	3	CO1	2	PO1	1.3.1
	b)	Minimize the 4-variable function F (A, B, C, D) =Σ (0,2,5,6,7,8,10,13, 15) Simplify using a K-map and draw the minimized circuit using logic gates.	3	CO1	3	PO1	1.3.1
	c)	Explain and draw the internal circuit of a TTL NAND gate using multiple-emitter transistors.	3	CO1	4	PO1	1.3.1
		Attempt any Two parts of the following.					
Q3.							
	a)	What is a Full Adder? Derive the Boolean expressions & truth table for the Sum and Carry outputs of a Full Adder and construct Full Adder using NAND gates.	3	CO2	1	PO1	1.3.1
	b)	Define a magnitude comparator. Explain the working principle of a 1-bit magnitude comparator with the help of its truth table, logical expression and logic diagram.	3	CO2	2	PO1	1.3.1
	c)	Realize the Boolean function F (A, B, C, D) = Σ m (0,2,5,7,8,10,13, 15) using an 8-to-1 multiplexer with proper selection lines and input lines.	3	CO2	3	PO1	1.3.1

BL – Bloom's Taxonomy Levels (1- Remembering, 2- Understanding, 3 – Applying, 4 – Analysing, 5 – Evaluating, 6 - Creating)

CO – Course Outcomes

PO – Program Outcomes (As per Examination Reform Policy by AICTE Page No. 15) PI Code – Performance Indicator Code

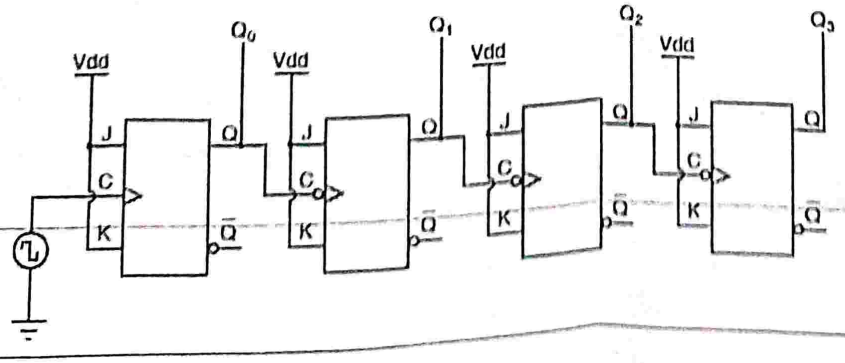
Sub Code: BEC 207

Roll No. | 2 | 0 | 2 | 4 | 0 |

B. Tech. ECE, ECE-IoT & EE
Year: II Semester: III
Major Examination: 2025-2026
Subject Name: Digital Electronics

Time: 3 Hrs. **Max. Marks: 50**

Note: Attempt All questions.

Q1.	**Attempt any five parts of the following.**	Marks	CO	BL	PO	PI Code
a)	Convert the hexadecimal number $(F3A7C2)_{16}$ into binary and octal and decimal number $(245)_{10}$ into (a) Binary (b) Octal.	2	CO1	1,3	1,2,3	1.3.1
b)	Draw and explain the circuit diagram, working of a DTL NAND gate.	2	CO1	2,4	1,2,3	1.3.1
c)	Simplify using K-map: F (A, B, C, D) = Σ m (0,2,5,6,8,10,13,14) and find the minimized expression.	2	CO1	1,3	1,2,3	1.3.1
d)	Write the truth table and logic expression of a 4-bit Binary-to-Gray code converter.	2	CO2	2,3	1,2,3	1.3.1
e)	Implement the function F (A, B, C) =Σ m (0,1,2,4,6) using a 4:1 MUX taking A as select input.	2	CO2	1,3,4	1,2,3	1.3.1
f)	Design and discuss the working principle of a 2-bit binary multiplier.	2	CO2	1,3,4	1,2,3	1.3.1
g)	Write short notes on: (a) Encoder & Decoder (b) Multiplexer & Demultiplexer	2	CO2	1,2	1,2,3	1.3.1
Q2.	**Attempt any two parts of the following.**					
a)	Differentiate between a flip-flop and a latch in brief. Describe the step-by-step procedure for converting a JK flip-flop to a T flip-flop. Show the truth table and simplification for each step.	5	CO3	1,2,3	1,2,3	1.3.1
b)	Define shift registers and types. Implement a 4-bit Serial-In Parallel-Out (SIPO) shift register. Explain its operation with a timing diagram and truth table.	5	CO4	1,2,4	1,2,3	1.3.1
c)	Explain the race-around condition in a JK flip-flop. Deduce the characteristics table and characteristics equation for SR and JK flip-flops.	5	CO3	1,2,3	1,2,3	1.3.1
Q3.	**Attempt any two parts of the following.**					
a)	What are hazards in digital logic circuits? Distinguish between static 1 and static 0 hazards with a suitable example.	5	CO5	1,2,3	1,2,3	1.3.1
b)	Design a synchronous 3-bit up/down counter using JK flip-flops. Explain mode control, excitation table, and timing diagram.	5	CO4	2,3,4	1,2,3	1.3.1
c)	Differentiate between synchronous and asynchronous sequential circuits. From the given circuit diagram, find the counting sequence. Where Q_0 is LSB and Q_3 is MSB, and the initial state is 0000. 	5	CO4	2,3,4	1,2,3	1.3.1

Q4. Attempt any two parts of the following.						
a)	Consider a combinational logic circuit that has 3 inputs and 2 outputs. The logic functions for the outputs are given below. Implement this circuit using a PLA and a PAL. $X(A, B, C) = \Sigma m(1, 2, 4, 6)$ and $Y(A, B, C) = \Sigma m(0, 1, 3, 6, 7)$	5	CO6	1,2,3	1,2,3	1.3.1
b)	Design a state machine to detect the overlapping pattern "1011". Show state diagram, state table, and output logic.	5	CO6	1,2,3	1,2,3	1.3.1
c)	Differentiate between SRAM, DRAM, and PROM memory based on their architecture, speed, power consumption, and applications. Explain the working mechanism of DRAM.	5	CO6	1,2	1,2,3	1.3.1
Q5. Attempt any two parts of the following.						
a)	Find the logical expression for Sum and Carry in a Full Adder using a K-map. Draw and implement a PROM-based design for generating Sum and Carry outputs.	5	CO6	1,2,3	1,2,3	1.3.1
b)	Draw and explain the working of a 6T SRAM cell in detail. Describe its Read and Write operations with a neat diagram.	5	CO5	1,2,4	1,2,3	1.3.1
c)	What is an FPGA? Explain its basic architecture with the help of a neat diagram and describe the roles of Configurable Logic Blocks (CLBs) and Look-Up Tables (LUTs) in its operation.	5	CO5	1,2	1,2,3	1.3.1

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