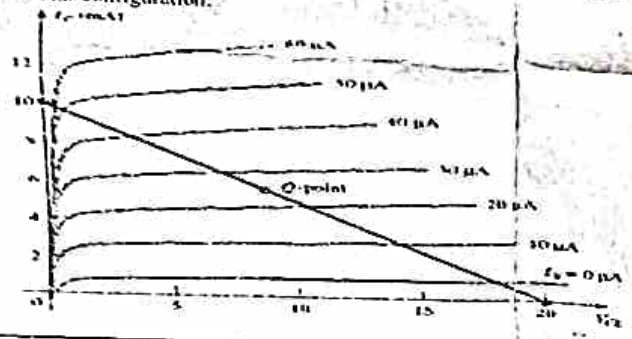
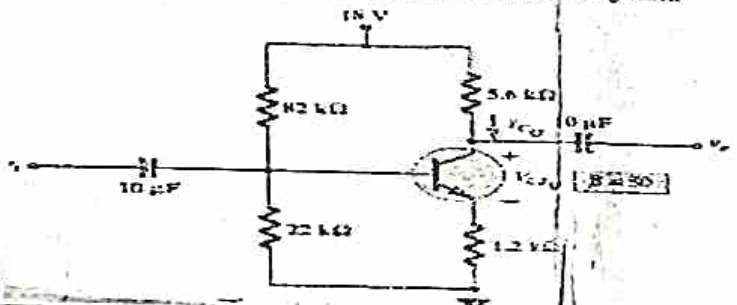
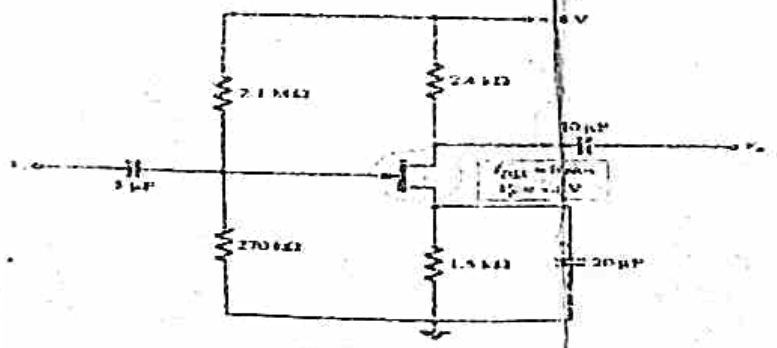
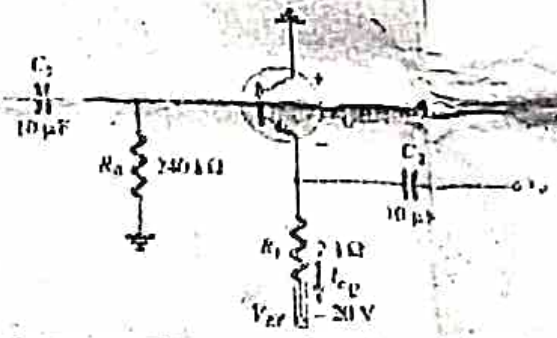
INSTITUTE OF ENGINEERING AND TECHNOLOGY, LUCKNOW
1st MID SEMESTER (CLASS TEST) EXAMINATION 2024-25
IEC-301 Electronic Devices & Circuits

TIME 1 HOURS

MAXMARKS-30

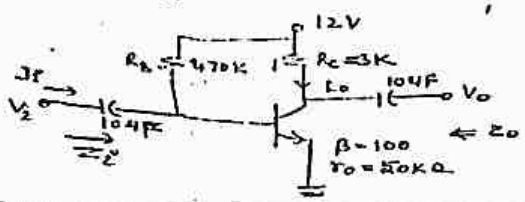
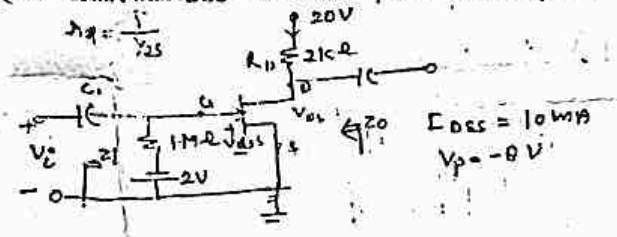
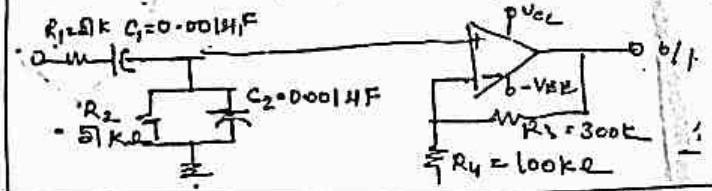
Note: Attempt all questions.

Ques No.	Question Paper Based on Course Outcomes According to Bloom's Cognitive Level	Marks	CO	BL
1	A) Explain and show the energy bands in Intrinsic Si & Ge Semiconductor. B) Describe the phenomenon of Optical absorption, luminescence along with excess carriers. C) Draw and explain the Junction properties of a Diode .	6	Co.1	BL1
2	Given the load line of figure and the defined Q point , determine the required values of Vcc,Re,Rb for fixed bias configuration: 	6	Co.2	BL2
3	Determine the V_{CE} and the I_C for the given voltage- divider configuration 	6	CO2	Bl 3
4	Determinethe following for the network of I_{DQ} and V_{GSQ} 2. V_D 3. V_S 4. V_{DS} 5. V_{DG}& Plot transfer curve: 	6	Co.2	BL3
5	Determine V_{CE}& I_{CQ} for network 	6	Co.2	BL2

INSTITUTE OF ENGINEERING AND TECHNOLOGY, LUCKNOW
2nd MID SEMESTER (CLASS TEST) EXAMINATION 2024-25
IEC-301 Electronic Devices & Circuits

TIME 1 HOURS **MAXMARKS-30**

Note: Attempt all questions.

Q. No.	Question Paper Based on Course Outcomes According to Bloom's Cognitive Level	Marks	CO	BL
1	Derive the expressions and model for two port network devices and thehybrid model with proper Notations.	6	Co.2	BL1
2	For the given Network : Determine: a) Re b)Zi c)Zo d)Av e)Ai f) Repeat part c through e including Ro = 50KΩ only and for above partstake Ro=∝Ω 	6	Co.3	BL3
3	The circuit has operating point VGSQ = -2V & IDQ =5.625mA with IDSS = 10mAand Vp= -8V. Vi ac input is applied across the circuit where Yos = 40μs. 	6	CO3	BL3
4	Explain basic oscillator operation and state the necessaryconditions with feedback circuit. Calculate the resonant frequency of Wein bridge oscillator foriven figure : 	6	Co.4	BL3
5	Determine the following power amplifiers in details : a) Class A b)Class AB c) Class C d) Class D	6	Co.5	BL2

Printed pages:02

Subject Code: IEC-301 Roll No.:

B.Tech.

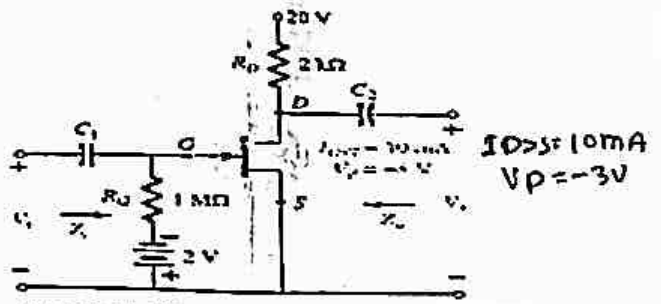
(SEM III) ODD SEMESTER EXAMINATION 2024-25

ELECTRONIC DEVICES AND CIRCUITS

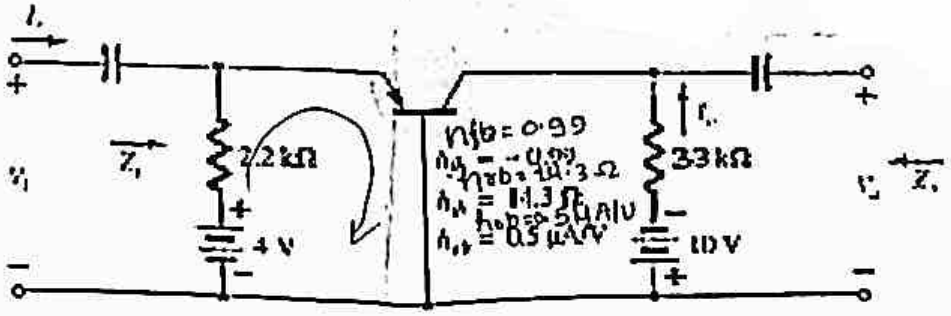
[TIME: 3 hrs.] [Max. Marks: 70]

Note: *Attempt All Questions. All Question carry equal marks.*

		Marks
Q1.	Answer ALL parts.	
(a)	Explain the following terms.	3.5
	(i) Explain the phenomena of Luminescence and its different types .	
	(ii) Describe the working principle of Optical Absorption	
	OR	
	Explain and show the energy bands in Intrinsic Si & Ge Semiconductor in detail.	
(b)	Explain the operation and characteristics of N-Channel Enhancement type MOSFET along with transfer curve.	3.5
	OR	
	Draw the AC equivalent circuit for JFET and explain their parameters.	
(c)	Draw and Explain the DC bias circuit for class A amplifier.	3.5
(d)	Explain the working of Oscillator and Barkhausen criterion for sustained oscillation.	3.5
Q2.	Answer ALL parts.	
(a)	Derive the hybrid parameter model for BJT and derive the following parameters:	7
	(i) current gain	
	(ii) voltage gain	
	(iii) Input Impedance	
	(iv) output admittance	
	OR	
	The fixed bias configuration had an operating point defined by V_{GSQ} = -2V & I_{DQ} = 5.625mA, with I_{DSS} = 10 mA & V_P = -8V Determine (i) g_m, (ii) R_d (iii) Z_i (iv) Z_o (v) A_v (vi) Determining A_v ignoring the effect of R_d. The network is redrawn as given figure with applied voltage V_i. The value of Y_{os} is provided as 40 μS.	



(b) For the network, Determine: i) Z_i ii) Z_o iii) A_v. iv) A_i 7



Printed pages:02

Q3. Answer **ALL** parts.

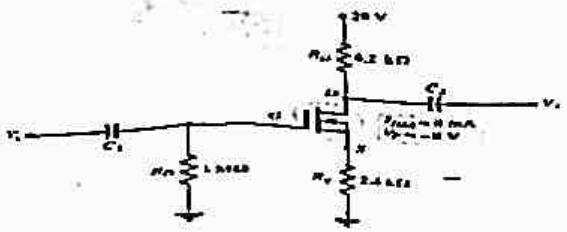
(a) Define Miller effect Capacitance. Draw the following circuits and explain its working principle. 7

(i) Wein bridge oscillator
(ii) LC oscillator
(iii) Phase shift oscillator

OR

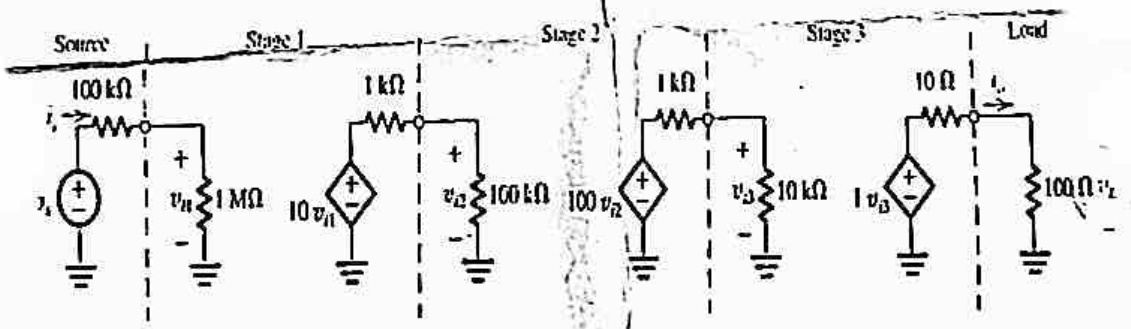
Explain the various classes of operation of Power Amplifiers (class A, B, AB and C) also calculate their power efficiency and its linearity issues.

(b) Determine the following for the network of Figure shown below: 7
(i)V_{GSQ}, (ii) I_{DQ} (iii) V_D



Q4. Answer **ALL** parts.

(a) Figure shown below depicts an amplifier composed of a cascade of 3 stages. The amplifier is fed by a signal source with a source resistance of 100 KΩ and delivers its output into a load resistance of 100Ω. 7
The first stage has a relatively high input resistance and a modest gain factor of 10. The second stage has a higher gain factor but lower input resistance. Finally, the last, or output resistance. Evaluate the overall voltage gain, that is V_L / V_S, the current gain and power gain.



(b) Explain the basic feedback concept with schematic of feedback amplifier circuit . Discuss the four basic feedback topologies with the help of Schematic Diagram. 7

OR

For a class B amplifier providing a 20 V peak signal to a 16 Ω load and a power supply of V_{cc} =30V, determine the input power, output power and circuit efficiency.

Q5. Answer **ALL** parts.

(a) Calculate the voltage gain with and without feedback for a voltage shunt feedback amplifier using FET with values of G_m = 5mS, R_D = 5.1KΩ , Rs= 1KΩ , Rf = 20KΩ. Breifly discuss the Phase and gain margins of FET feedback amplifiers. 7

(b) A Common Emitter amplifier uses a voltage source having internal resistance Rs = 800 ohm and load resistance is R_L = 1000 ohm. 7
H parameters are: h_{ie} = 1K, $h_{re} = 2*10^{-4}$ h_{fe} = 50, h_{oe} = 25 microA/v.
Calculate current gain, input resistance R_i and Voltage gain A_v.

OR

Define transistor bias stabilization and stability factors. Describe the reason why voltage divider bias circuit is more stabilized than fixed bias circuit with the help of circuit diagram.