

1st MID SEMESTER (CLASS TEST) EXAMINATION 2024-25
IEC -302 DIGITAL LOGIC DESIGN

TIME 1.0 HOUR

MAX. MARKS: 20

Note: Attempt Any FOUR questions. Question no. 5 is compulsory.

Q. N	Question Paper Based On Course Outcomes According To Bloom's Cognitive Level	Marks	CO	BL
1	(a) Obtain the truth table of the function: $F = xy + xy' + y'z$	2.5	CO1	BL2
	(b) Design a counter with the following binary sequence: 0, 1, 3, 7, 6, 4 and repeat. Use T FF.	2.5	CO3	BL3
2	(a) Draw the logic diagram that implements the following function: $F(A,B,C,D) = \sum m (0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 29, 31)$.	2.5	CO1	BL3
	(b) Implement the following function with multiplexer: $F = \sum m (0, 1, 3, 4, 8, 9, 15)$	2.5	CO2	BL4
3	(a) Minimize the given Boolean function using K-Map. $F(A,B,C,D) = \sum m (1, 3, 7, 11, 15) + d(0, 2, 5)$.	2.5	CO1	BL5
	(b) Design a 16:1 multiplexer using 4:1 multiplexer.	2.5	CO2	BL4
4	(a) Design a 3-bit combinational circuit which produce logic 1 output when more than one input variables are at logic 1.	2.5	CO1	BL5
	(a) Construct a 5x32 line decoder with 3x8 decoders and 2x4 decoder.	2.5	CO2	BL3
5	A sequential ckt has two flip flops (A and B), two inputs (x and y), and an output (z). Their functions are as follows: $J_A = xB + y'B'$ $K_A = xy'B'$ $J_B = xA'$ $K_B = xy' + A$ and $z = xyA + x'y'B$ Obtain ckt diagram, state table, and State diagram.	5	CO2	BL6
	OR Minimize the following function using tabular method: $F(w, x, y, z) = \sum m (0, 1, 2, 8, 10, 11, 14, 15)$.	5	CO1	BL5

2nd MID SEMESTER (CLASS TEST) EXAMINATION (2024-25)
DIGITAL LOGIC DESIGN (IEC - 302)

TIME 1.0 HOUR

MAX. MARKS: 20

Note: Attempt ALL questions.

Q.	Question Paper Based On Course Outcomes According To Bloom's Cognitive Level	Mark	CO	BL
1	(a) Write all the characteristics of digital logic families with diagrams if required.	2.5	CO3	BL5
	(b) Draw the circuit of a DTL NAND gate with suitable values of components. Explain its working with truth table. Also calculate the fan out of it.	2.5	CO3	BL3
2	(a) Classify and explain the various types of semiconductor memories used in digital systems.	2.5	CO3	BL3
	(b) Draw the circuit of a TTL NAND gate with suitable values of the components. Explain its working. Also calculate its propagation delay.	2.5	CO3	BL4
3	(a) Draw an inverter circuit using a BJT and Explain its working using numerical values of $R_C = 1K\Omega$, $R_B = 22K\Omega$, $h_{FE} = 50$, $V_{CC} = 5V$, $V_{BE} = 0.7V$ and $V_{CE} = 0.2V$.	2.5	CO3	BL4
	(b) Implement the following function with a PLA:- $F = \sum (0, 5, 6, 7)$	2.5	CO3	BL3
4	(a) The conversion rate of a 8-bit ADC is 12 micro seconds. Find the maximum frequency of the input sine wave that can be digitized.	2.5	CO4	BL4
	(b) Draw the weighted register DAC circuit and explain its working. Also calculate the number of resistors required in a 12-bit weighted resistor DAC.	2.5	CO4	BL3

B. TECH.
(SEM-III) ODD SEMESTER EXAMINATION 2024-25
DIGITAL LOGIC DESIGN

Time: 3.0 Hours

Maximum Marks: 70

Note: Attempt All Questions. All Question carry equal marks.

- Q1. Answer ALL parts.** Marks
- (a) What do you understand by the error detecting codes and the reflected codes? 3.5
- (b) Represent the decimal number 8630 (i) in BCD (ii) in excess-3 code (iii) in 2421 code. 3.5
- (c) Simplify the Boolean function : $F(w, x, y, z) = \sum m(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$ 3.5
- OR
- Simplify the following function by means of the tabulation method:
 $F(A, B, C, D, E, F, G) = \sum m(20, 28, 52, 60)$
- (d) Implement the Boolean function: : $F(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15)$ using 8×1 multiplexer with A, B, and D connected to selection lines s_2, s_1 , and s_0 , respectively. 3.5
- OR
- Design the circuit that compares two 4-bit numbers, A and B, to check if they are equal. The circuit has one output x, so that $x = 1$ if $A = B$, and $x = 0$ if $A \neq B$.
- Q2. Answer ALL parts.**
- (a) What do you understand by 4-bit shift register? Explain with neat diagram and wave forms for all types of shift registers. 7
- (b) Write the excitation table of J-K flip flop and T flip flop. Design a counter that counts the decimal digits (0-9) according to the 2421 codes. 7
- OR
- A sequential circuit has two flip – flops (A and B), two inputs (x and y), and one output (z). The flip flop input functions and the circuit output function are as follows:
- $$\begin{aligned} J_A &= xB + y'D' & K_A &= xy'B' \\ J_B &= xA' & K_B &= xy' + B \\ z &= xyA + x'y'B \end{aligned}$$
- Q3. Answer ALL parts.**
- (a) Draw the circuit diagram of RTL NOR gate using BJT with suitable components values and calculate the Fan-out and noise margins. 7
- OR
- (a) Draw the logic circuit diagram of 3-Input TTL NAND gate and explain its working and verify the truth table of the NAND gate.
- (b) Explain the various semiconductor memories used in digital systems. What do you understand by the Programming Logic Array? Implement the function $F_1 = \sum(0, 1, 2, 5, 7)$ and $F_2 = \sum(0, 3, 5, 6)$ using PLA. 7
- Q4. Answer ALL parts.**
- (a) Write the specifications of DAC/ADC. Find the resolution and dynamic range in dB of a D/A converter, if the maximum peak to peak output voltage is 5V and the input signal is a 10 bit word. 7
- (b) Explain the working of a flash type A/D converters with neat diagram. Also give the truth table for a flash type A/D converter. 7
- OR
- List the specifications of a D/A converter. Draw and Explain R-2R Ladder D/A converter. Also give any two advantages over weighted resistor D/A converter.
- Q5. Answer ALL parts.**
- (a) What do you understand by Hardware Description Language (HDL) explain in brief. Also give the digital system design process with suitable diagram. 7
- (b) Explain the various types of modelling schemes used in HDL/VHDL in detail. 7
- OR
- Implement the combinational circuits like Adder, Subtractor and MUX using HDL/VHDL.