1st MID SEMESTER (CLASS TEST) EXAMINATION 2024-25

IEC -401 Computer Organization and Architecture

TIME 1.0 HOUR MAX. MARKS: 20

Note: Attempt ALL questions.

Q. No.	Question Paper Based On Course Outcomes According To Bloom's Cognitive Level	Marks.	CO	BL
1	(a) Draw the block dingram of n Van-Neumann Architecture? Explain in detail.	2	CO1	BL1
	(b) What are the functional units of a computer? Explain each units in detail.	2	CO1	BL2
2	(c) Explain the addition and subtraction of two floating point numbers with suitable flow chart.	2	CO1	BL3
	(d) Multiply two binary numbers (-13) and (+17) using Booth's Algorithm with flowchart.	2	CO1	BL4
3	(c) Divide a number '9' by another number '6' using restoring method of division.	2	CO1	BL5
	(d) What is an instruction cycle? Give the various phases of Instruction cycle.	2	CO2	BL4
4	(c) What are the various computer registers? How are they are organized for proper function in a computer system? Explain with neat diagram.	2	CO2	BL5
	(d) Draw the timing diagram for a fetch instruction.	2	CO2	BL3
5	(c) Explain the various types of addressing modes with suitable examples.	2	CO2	BL4
	(d) Explain the arithmetic pipe-line Architecture with example and suitable space-time diagram and Calculate the performance parameters like Sk, f, Ek and Hk.	2	CO2	BL5

2nd MID SEMESTER (CLASS TEST) EXAMINATION 2024-25

IEC -401 Computer Organization Architecture

TIME 1.0 HOUR **MAX. MARKS: 20**

Note: Attempt All questions.

Q. N	Question Paper Based On Course Outcomes According To Bloom's Cognitive Level	Mark	CO	BL
1	How register transfer is taken place in RTL? Explain with diagram. Draw a bus system for four line using three state -buffers.	5	CO3	BL3
2	Explain 4 bit arithmetic circuit with diagram. Also make function table of it. What do you understand by shift micro-operations? Also implement its hardware	5	CO3	BL4
3	Draw the micro-instruction format. Specify seven distinct micro-operations Give the effective address for memory of 1k chip uses A_{10} to A_{15} for chip select.	5	CO4	BL5
4	Explain the mechanism of DMA with a suitable neat diagram. What is a cache memory? Explain any one procedure of mapping.	5	CO4	BL6

Roll No.

B. Tech.

(SEM IV) EVEN SEMESTER EXAMINATION 2024-25

COMPUTER ORGANISATION AND ARCHITECTURE

[TIME: 3 Hrs.] [Max. Marks: 70]

Note: *Attempt All Questions. All Question carry equal marks.*

Q1. Answer **ALL** parts.

		Marks
(a)	List the various units of a microprocessor used in a computer system.	3.5
(b)	Draw the hardware architecture for addition and subtraction of signed-magnitude numbers.	3.5
(c)	Explain the register arrangements required for floating point Arithmetic operations	3.5

OR

(d)	Draw the flowchart for multiplication of two numbers using Booth's Algorithm. Differentiate between Van-Neumann and Harvard Architecture with diagram.	3.5

OR

Divide a number 8 by a divisor 3 using a restoring method.

Q2. Answer **ALL** parts.

(a)	What is Instruction code? Explain the computer registers with their word lengths. Draw and explain the connections of all registers with a common bus system.	7
(b)	Draw the basic computer instruction code formats. Explain the timing signals and design of a control unit of a basic computer organization.	7

OR

Explain the various phases of instruction cycle and the registers involved in each instruction cycle in detail.

Q3. Answer **ALL** parts.

(a)	Draw and Explain an efficient scheme for transferring information between registers in a multiple –register configuration 4x1 multiplexer.	7

OR

What do you understand by logic micro-operations? Also implement its hardware with function table.

(b)	Explain the designing of a micro-program control unit for a computer with neat diagram with a micro-program-sequencer for a control memory.	7

Q4. Answer **ALL** parts.

(a)	Explain the memory Hierarchy used in a computer system. List the various types of memories with their features.	7
(b)	Draw the RAM and ROM chips with function table. Explain the memory address mapping for microprocessor assuming that a computer needs 512 bytes of RAM and 512 bytes of ROM. Also draw the connection of these memory if RAM chips are of 128 x 8 and ROM chip is 512 x 8 to a CPU.	7

Give the various types of auxiliary memories used in a computer system with their features and neat diagrams.

OR

Q5. Answer **ALL** parts.

(a) What is cache memory? Give its advantages and disadvantages. Also define hit ratio and miss ratio. Explain any two methods of mapping techniques with neat diagram and suitable example. 7

(b) Explain the tightly coupled and loosely coupled multiprocessors from the viewpoint of hardware organization and programming techniques. 7

OR

How many switch points are there in a crossbar switch network that connects **p** processors to **m** memory modules?

CO-BL Mapping

Even Semester Examination 2024-25			
Subject Code: IEC-401			
Subject Name: COMPUTER ORGANISATION AND ARCHITECTURE			
Q. No.	Marks	CO	BL
1(a)	5	1	2
1(b)	5	1	3
1(c)	5	1	3
1(d)	5	1	4
2(a)	10	2	4
2(b)	10	2	3
3(a)	10	3	4
3(b)	10	3	4
4(a)	10	4	5
4(b)	10	4	6
5(a)	10	5	5
5(b)	10	5	4