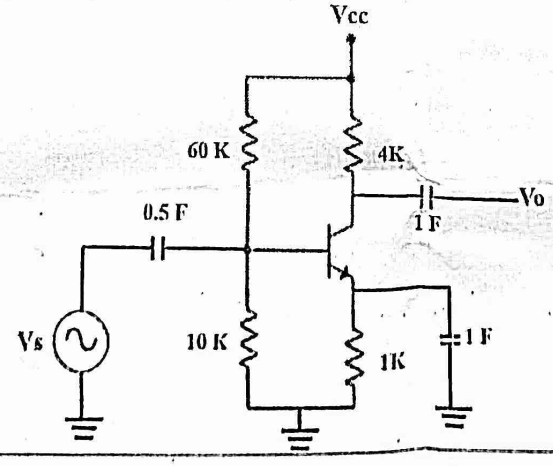
Printed Pages: 2

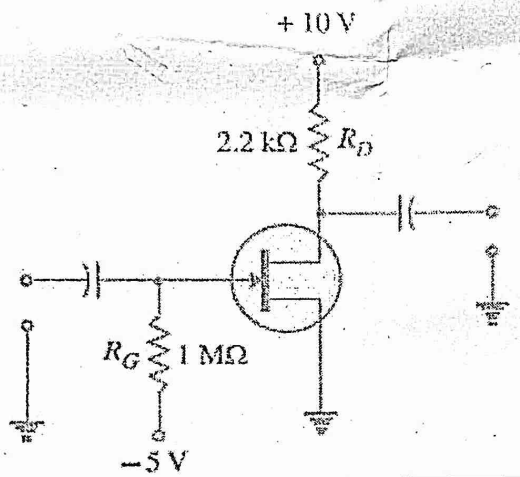
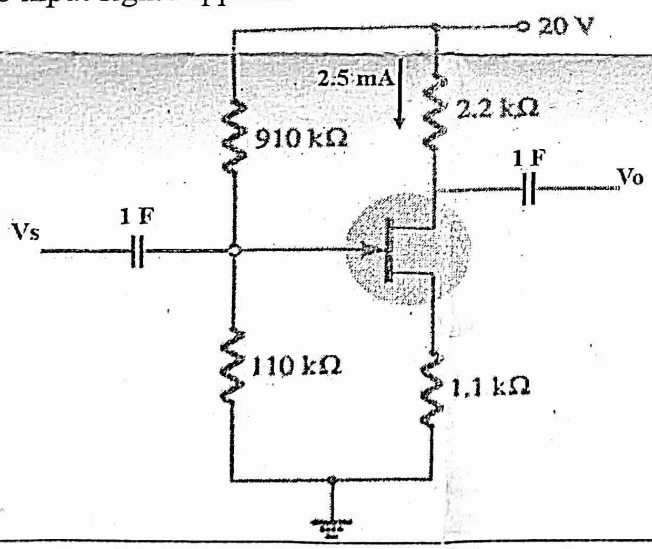
Subject Code
BEC-210

B. TECH.
Year: 2nd, Semester: III
MINOR TEST (EXAMINATION): 2025-26
Electronic Devices & Circuits Theory

Time: 2 Hr. **Max. Marks: 30**

Note: Answer all questions

Q1.		Attempt any **Three** parts of the following. Q.1 (a) is compulsory. **(Unit-1 & Unit-2)**	Marks	CO	BL	PO	PI Code
	a)	With the help of a circuit diagram, explain the collector-to-base bias method. How does it improve stability compared to fixed bias method?	4	1	2		
	b)	An N-channel JFET has I_{DSS} = 2 mA and Vp = -4 V. Calculate its drain current and transconductance for an applied gate-to-source voltage of -2V.	3	2	3		
	c)	With the help of suitable diagram, explain the input and output characteristics of Common Emitter configuration.	3	1	2		
	d)	Explain the operation of NMOS with drain and transfer characteristics.	3	2	2		
Q2.		*Attempt any* ***Three*** *parts of the following. Q.2 (a) is compulsory.* ***(Unit-1)***					
	a)	*Explain the terms stability factor. Why is it important? Derive its expression for voltage divider bias in npn transistor.*	4	1	3		
	b)	*Discuss the differences between BJT and FET devices. Highlight the importance of FET devices.*	3	1	3		
	c)	In amplifier shown, transistor has h_{fe} = 75, h_{ie} = 2.5kΩ, h_{re} = 0 and h_{oe}=20 μ℧. Calculate current gain, voltage gain input impedance. 	3	1	2		

	d)	Derive the relations among α, β, and γ. Also, write output current equations in each configuration.	3	1	2		
Q3.		Attempt any Three parts of the following. Q.3 (a) is compulsory. (Unit-2)					
	a)	Draw the drain and transfer characteristics of N-channel JFET. Also, explain the condition of pinch-off.	4	2	2		
	b)	Explain the self bias scheme for FET.	3	2	2		
	c)	In the circuit diagram shown below, a JFET has values of V_{GS} (off) = – 7 V and I_{DSS} = 14 mA. Determine the values of V_{GS}, I_D and V_{DS}. 	3	2	3		
	d)	For the circuit shown below, find VDS and VGS with zero input signal applied. 	3	2	3		

BL – Bloom's Taxonomy Levels (1- Remembering, 2- Understanding, 3 – Applying, 4 – Analyzing, 5 –Evaluating, 6 - Creating)

CO – Course Outcomes

PO – Program Outcomes

PI Code – Performance Indicator Code

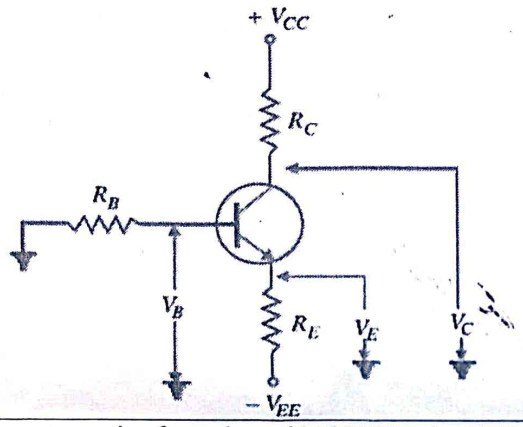
Sub Code: BEC-210

B. Tech.

Year: II Semester: III
Even Semester 2025-2026
Subject Name: Electronic Devices & Circuits Theory

Time: 3 Hr. **Max Marks: 50**

Note: Attempt All questions.

Q1	**Attempt any five parts of the following. (Unit I and II)**	Marks	CO	BL	PO	PI Code
a)	Discuss the hybrid parameter model of *npn* transistor.	2	1	2	1	1.3.1
b)	Explain Darlington pair with neat and clean diagram.	2	1	2	1	1.3.1
c)	From the given figure, find (i) emitter voltage (ii) base voltage (iii) collector voltage w.r.t. ground. 	2	1	3	1	1.3.1
d)	Derive the drain current equation for n-channel MOSFET using GCA method.	2	2	2,3	1	1.3.1
e)	Explain the operation of voltage divider based n-channel MOSFET amplifier.	2	2	2,3	1	1.3.1
f)	A JFET has a gate current of 2.5 nA and the reverse gate voltage is 10 V. What is the input resistance of the JFET?	2	2	3	1	1.3.1
g)	Mention the features of BJT, JFET, and MOSFET devices.	2	2	2	1	1.3.1
Q2.	**Attempt any two parts of the following. (Unit III only)**					
a)	Discuss the negative and positive feedback amplifiers and their advantages and disadvantages in detail.	5	3	2	1	1.3.1
b)	Determine the voltage gain, input impedance, and output impedance with feedback for current series configuration having A = -100, Ri = 10kΩ, Ro = 20 kΩ for feedback factor of -0.5.	5	3	3	1	1.3.1
c)	Discuss Transconductance feedback amplifier. Also, compare the input and output impedances of different feedback amplifiers.	5	3	2,3	1	1.3.1
Q3.	**Attempt any two parts of the following. (Unit III only)**					
a)	Explain voltage series feedback amplifier with the impact on feedback gain, input impedance, output impedance.	5	3	2,3	1	1.3.1
b)	Draw the transistor level diagram of voltage shunt amplifier and explain its operation.	5	3	2	1	1.3.1
c)	Draw and explain the operation of FET amplifier stage with voltage series feedback.	5	3	2,3	1	1.3.1
Q4.	**Attempt any two parts of the following. (Unit IV only)**					
a)	What are the conditions for sustained oscillations? Highlight the features of oscillators.	5	4	2	1	1.3.1
b)	Draw the circuit and explain the operation of Hartlay Oscillator. Also, determine the expression for frequency of oscillation.	5	4	2,3	1	1.3.1
c)	What do you mean by tuned oscillator? Explain in detail.	5	4	2	1	1.3.1
Q5.	**Attempt any two parts of the following. (Unit IV only)**					
a)	Discuss the operation of Wein Bridge oscillator neat and clean diagram. Also, determine its frequency of oscillation.	5	4	2,3	1	1.3.1

b)	Describe the working of crystal oscillator with diagram. Also explain the operating modes of the crystal oscillator.	5	4	2,3	1	1.3.1
c)	Explain the operation of RC phase shift oscillator. A phase shift oscillator uses 5 pF capacitors. Find the value of R to produce a frequency of 800 kHz.	5	4	3	1	1.3.1

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