

Operating Manual: Two-SCR General Purpose Gate Firing Board FCRO2100 Revision H

Introduction

This manual describes the salient features and specifications of the FCOG2100 firing board, including typical firing circuit signal waveforms and a checkout procedure.

Product Description

1.0 Application

The FCOG2100 board is a two-SCR firing board suitable for use with single-phase AC controllers and center-tap rectifiers. The firing board responds to a voltage or current delay angle command signal (SIG HI) to produce two delayed, isolated, 180°-spaced high-current SCR gate firing pulses. An optional regulator circuit provides voltage or current regulation.

2.0 ASIC-Based Firing Circuit

All firing circuit logic is contained in a custom 20-pin ASIC. Additional detail on the firing circuit theory is contained in a separate engineering society paper¹.

3.0 Board Mounted Connectors

3.1. Gate/Cathode and Control Power Connector

The SCR gate/cathode interface is provided by 8-position Mate-N-Lok™ vertical connector J2 at positions 1 and 2 (+X SCR, load connected cathode) and 4 and 5 (-X SCR, line connected cathode).

The board-mounted 6 VA power supply transformer (T1) is normally energized by connecting the mains voltage between positions 7 and 8 of J2. The gate firing signals are locked to the mains waveform through transformer T1, hence, the board power source must be in phase with the mains voltage.

Transformer T1 has a center-tapped 115/230 Vac or 240/480 Vac primary winding. The secondary winding is connected to a bridge rectifier to generate the unregulated 30 Vdc board supply which feeds a +12 V regulator.

3.2. Control Signal Connector

The delay angle command (SIG HI), instant and soft inhibit controls, voltage and current feedback signal, and auxiliary power connections are available through J1, a 12-position Mate-N-Lok™ connector. The pinout of this connector is detailed in drawing E211 Rev H.

3.3. Operating Frequency Selection

The FCRO2100 board may be set for operation at 50 or 60 Hz by making the appropriate jumper selection at J3. In 60 Hz operation, R24 is paralleled with the VCO timing resistor R12. In 50 Hz operation, R24 is not connected which maintains the appropriate VCO response.

4.0 Gate Delay Command

The SIG HI delay angle command signal is inversely proportional to the delay angle. When SIG HI is at a maximum, the delay angle is at a minimum value, corresponding to maximum rectifier or controller output. When SIG HI is at a minimum, the delay angle is at a maximum value, corresponding to a minimum rectifier or controller output.

¹ Bourbeau, F. J., "Phase Control Thyristor Firing Circuit: Theory and Applications", Power Quality '89, Long Beach, California.

The delay command signal, SIG HI, may be configured as a voltage (0 to 5 Vdc) or current signal. When SIG HI is a current signal, R23 is selected to provide 5.0 Vdc at the maximum delay angle command signal current, typically 249 ohms for a 4 to 20 mA or 0 to 20 mA range.

The maximum effective full-scale delay angle command range is limited to approximately $6^\circ \leq \alpha \leq 174^\circ$; the SIG HI range may be adjusted via the bias and span potentiometers (see section 5.0) to achieve narrower full-scale ranges.

5.0 Bias and Span Potentiometers

Two 5 k Ω potentiometers (designated R4 and R5) are used to control the bias and span of the delay angle command signal. This affords the user a convenient means to “fine tune” a board in a specific application.

With the FCRO2100 board connected to the SCRs, set the SIG HI command to its minimum value. Enable firing and gradually bring the SIG HI command up until the inhibit LED, P2, extinguishes. Adjust the bias potentiometer, R4, to achieve the desired minimum output voltage or current. Increase SIG HI to its maximum value and adjust the span potentiometer, R5, to obtain the maximum desired output. Decrease SIG HI again to the level used to set the bias potentiometer and check that the desired minimum output voltage or current has remained the same after adjusting R5. Depending upon the application, the potentiometers may need to be incrementally adjusted in this manner several times to achieve the exact range required by the user.

Figure 1 shows the phase detector (TP8) waveforms for maximum delay angle (SIG HI = 0.5 V) and minimum delay angle (SIG HI = 5.0 V). Calculate the delay angle from the duty cycle of the waveform at TP8 as $\alpha = 180^\circ(1 - D)$. The approximate minimum duty cycle of $D = 0.06$ corresponds to a maximum delay angle of $\alpha_{\max} = 180^\circ(1 - 0.06) \approx 169^\circ$. The approximate maximum duty cycle of $D = 0.96$ corresponds to a minimum delay angle of $\alpha_{\min} = 180^\circ(1 - 0.96) \approx 12^\circ$.

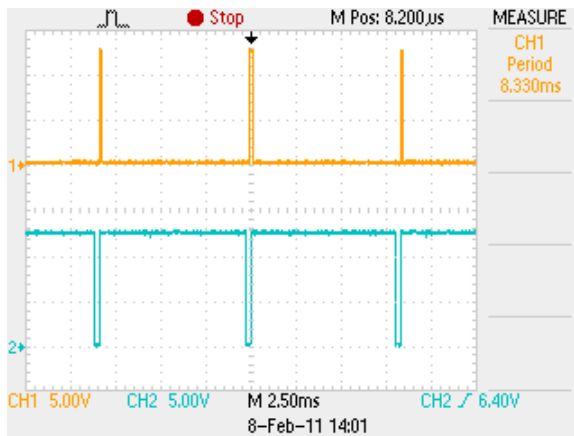


Figure 1. Maximum and Minimum Delay Angle Calculation
 Channel 1: Phase Detector (TP8), SIG HI = 0.5 Vdc, $D = 0.06$, $\alpha = 169^\circ$
 Channel 2: Phase Detector (TP8), SIG HI = 5.0 Vdc, $D = 0.96$, $\alpha = 12^\circ$

6.0 Regulator Circuit

The FCRO2100 board includes an optional regulation circuit for ac voltage or current feedback as supplied by a voltage or current transformer. A burden resistor R3, connected to the output of bridge rectifier BR2, is selected to provide 1.0 Vdc at the desired full load current or voltage.

7.0 Gate Inhibits

SCR gating is enabled by pulling the instant inhibit, \bar{I}_1 to 12 V and pulling the soft inhibit, \bar{I}_2 to ground. These signals are located at J1 pin 4 and J1 pin 12, respectively.

The instant inhibit signal \bar{I}_1 is normally pulled to ground through resistor RN4D (1.50 k Ω). The user typically connects the \bar{I}_1 signal to +12 Vdc to enable firing. This arrangement ensures that SCR gating is inhibited if plug P1 is inadvertently disconnected. A jumper may be installed between pins 4 and 6 of P3 to hold \bar{I}_1 at +12 Vdc at all times in applications where the instant inhibit is not needed.

The soft inhibit signal \bar{I}_2 is normally pulled to +12 Vdc through resistor RN4B (1.50 k Ω). The user then grounds \bar{I}_2 to soft-stop SCR firing. In this mode, the delay angle is ramped from the setpoint value determined by SIG HI to the largest angle possible, after which firing is completely inhibited. This is termed the soft-stop shutdown mode. When the user opens the connection at \bar{I}_2 , gating is enabled with the delay angle set to the maximum value. The delay angle then ramps to the value determined by SIG HI. The soft-stop and soft-start time constants are independently configurable via two timing resistors (R13 and R14 respectively) and a capacitor (C3).

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$$\begin{aligned}t_{\text{soft-stop}} &= 1.84(R13)(C3) \\t_{\text{soft-start}} &= 0.58(1.5 + R13 + R14)(C3)\end{aligned}$$

8.0 Power-On Reset

A power-on reset circuit inhibits SCR gating until the onboard regulator establishes the 12 Vdc rail voltage. This circuit has the added benefit of inhibiting SCR gating during severe line voltage transients or dropouts.

9.0 Gate Pulse Profile

The firing circuit uses a phase-locked loop (PLL) circuit locked to the single phase mains voltage. A series of counters divide the PLL's oscillator output and a decoder section then generates two 180°-wide delayed logic signals. These logic signals are modulated by the PLL's voltage controlled oscillator (VCO) output signal which operates at 256 times the line frequency.

The gate logic signals are amplified by a Darlington transistor array, which excites the primary windings of two isolated pulse transformers. The primary winding of each pulse transformer is also connected to a current-limiting resistor and a speed-up capacitor; this provides an initial hard-firing gate pulse followed by sustaining, lower amplitude picket fence pulses. Figures 3 and 4 show a single gate pulse burst profile and the detail of the first hard-firing pulse.

Each pulse module consists of a 2:1 ratio pulse transformer tested for 3500 V_{RMS} isolation, two secondary diodes, noise suppression resistors across the primary and across the gate drive output, and a fusible link in series with the output. Each pulse module is potted in a silicone insulating material.

The DDFO2100 (delay determinator fiber optic) is a version of the FCOG2100 with fiber optic outputs replacing the pulse transformers. Two FO1024 modules are installed which feature Avago HFBR-1412Z fiber optic transmitters in lieu of the EP1024 modules. The transmitters feature ST (bayonet) style connectors, operate at 820 nm and are directly compatible with the MVTB series of medium voltage trigger boards. Each module has an LED to indicate that the fiber optic transmitter is operational. Please specify this configuration on your ordering documents or contact Enerpro for additional information.

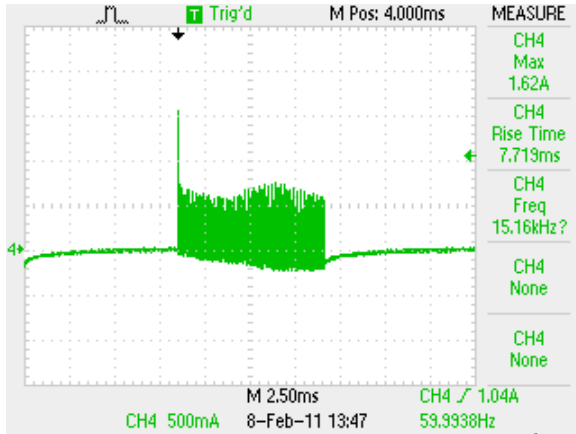


Figure 2 Gate Pulse Profile (into 1Ω)².

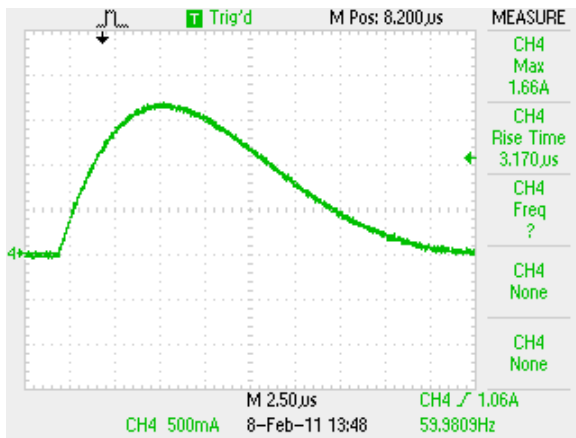


Figure 3 Initial pulse profile detail (into 1Ω)

² Current waveforms obtained using a Pearson model 2877 current transformer (1.0 A/V) with 4 primary turns. The current transformer is terminated by the scope's 1.0 M Ω input impedance.

10.0 Installation and Checkout

The following procedure should be followed to ensure proper operation prior to the application of mains power to the SCRs. The following equipment will be required:

Oscilloscope (100 MHz two-channel model or better)

Digital multimeter

DC supply or potentiometer for SIG HI input

Mate-N-Lok™ crimp tool (AMP Service Tool II #29004-1 or equivalent)

Mate-N-Lok™ extraction tool (AMP Extraction Tool 458994-2 or equivalent)

Wire strippers

10.1. *Ensure that the mains are not energized.* Wire a plug, P2, with the mains voltage connected to positions 7 and 8. Insert plug P2 into connector J2.

10.2. Install plug P1 with the delay angle command signal, signal common, and instant/soft inhibit controls wired to the plug.

10.3. Make the appropriate selection at J3 for 50 or 60 Hz mains.

10.4. Energize the mains voltage. Ensure that PD1, the power on LED, illuminates.

10.5. Enable firing via the enable commands and bring SIG HI slightly above 0.5 Vdc. Ensure that the inhibit LED, PD2, extinguishes.

10.6. Verify the presence of regulated 12 Vdc \pm 5% at J1-6 and regulated 5 Vdc \pm 5% at J1-7 with a multimeter.

10.7. Adjust the BIAS and SPAN potentiometers to achieve the required delay angle command signal response (see Section 5 of this document).

10.8. Observe the voltage at TP2 to verify that the PLL is in lock. The TP2 voltage should be centered at 5 Vdc with a variable amount of ripple dependent on the SIG HI signal. The TP2 ripple will be at its minimum value at the minimum and maximum SIG HI voltages, as in Figures 4 and 5, respectively. The TP2 ripple will be at its maximum value when the delay angle command is near $\alpha = 90^\circ$ as in Figure 6. Sweep the SIG HI voltage over the full range to ensure that the average voltage does not deviate from 5 Vdc.

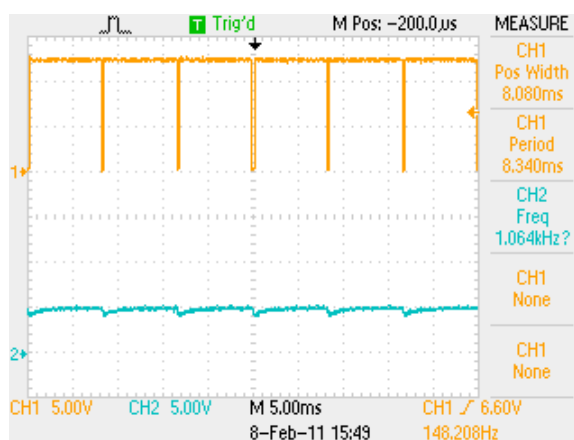


Figure 4 VCO control voltage and phase detector waveform, SIG HI = 0.5 Vdc
Channel 1: TP8
Channel 2: TP2

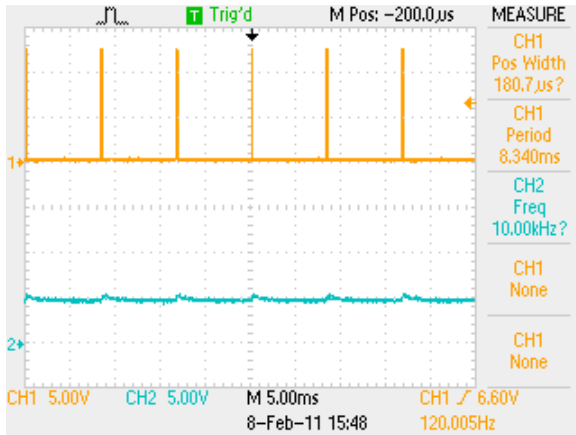


Figure 5 VCO control voltage and phase detector waveform, SIG HI = 5.0 Vdc
 Channel 1: TP8
 Channel 2: TP2

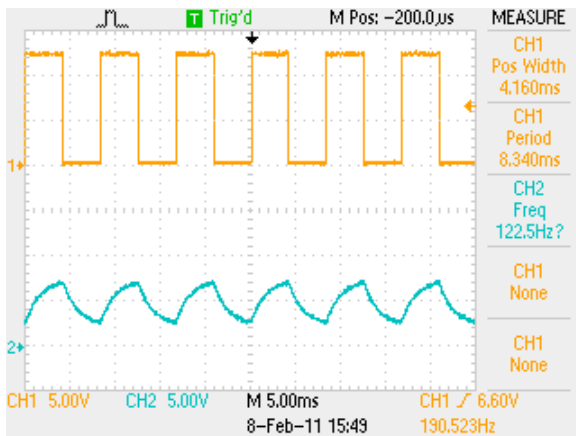


Figure 6 VCO control voltage and phase detector waveform, SIG HI = 2.75 Vdc
 Channel 1: TP8
 Channel 2: TP2

11.0 Electrical Specifications

Table 1. Specifications.

Maximum Ratings	
AC mains voltage	480 Vac
Pulse transformer hipot	3500 Vac (60 seconds)
Operating temperature range	0-65 C
Board ac supply voltage	28 Vac (24 Vac nominal)
12 V regulator output current	20 mA (30 Vdc supply)
5 V reference output current	5 mA (30 Vdc supply)
Auxiliary control power output from 24 Vac/30 Vdc	2 W
Delay angle range	$6^\circ \leq \alpha \leq 174^\circ$
Electrical Characteristics	
Delay angle command signal, SIG HI	Voltage: 0-5 Current: 4-20 mA
Control signal isolation from ground	Galvanic isolation provided by pulse transformers and control power transformers
Gate delay steady-state transfer function	Delay angle decreases as SIG HI increases
Gate delay dynamic transfer function bandwidth	-3 dB at 67 Hz, phase shift -45° at 57 Hz
Gate drive phase balance	$\pm 1^\circ$ (max)
Delay angle variance	$\Delta(\alpha)/\Delta(f) = 1.5^\circ/\text{Hz}$ 50/60 Hz compensation via J3 selection
Lock acquisition time	30 ms (typ)
Soft-start/stop time (independently configurable)	0.05 – 20.0 s (typical)
Low SIG HI inhibit	Firing inhibited when SIG HI < 0.49 Vdc. Remove D3 to defeat this feature
Power-on inhibit	Automatic
Instant/soft inhibit/enable inputs	Dry contact
Gate pulse burst frequency	256 times line frequency
Initial gate pulse open circuit voltage	15 V (30 Vdc supply)
Sustaining gate pulse open circuit voltage	7.0 V (30 Vdc supply)
Peak gate drive short circuit current	1.5 A (30 Vdc supply, 1.0 Ω gate load)
Sustaining gate drive short circuit current	0.5 A (30 Vdc supply, 1.0 Ω gate load)
Short-circuit gate drive current rise time	1.0 A/ μs (30 Vdc supply, 1.0 Ω gate load)
Board dimensions	137 x 114 x 35 mm (L x W x D)
Minimum creepage distance to ac mains	13 mm
Conformal coating	per MIL-1-46058, Type UR

Document Revision History			
Revision	Date	Notes	Approval
NC	02/2011	Initial release—update from 05/02/1996	JTM
A	05/2011	Additional datasheet information, DDFO information	JTM
B	06/2011	Correct Figure 1 annotation	JTM
C	06/2011	Correct phase detector annotation sec 5.0	JTM