



## **DCR3650Y28**

# **Phase Control Thyristor**

Replaces DS5875-3 DS5875-4 November 2021 (LN41359)

### **FEATURES**

- Double Side Cooling
- High Surge Capability

### **APPLICATIONS**

- High Power Drives
- High Voltage Power Supplies
- Static Switches

### **VOLTAGE RATINGS**

Part and Ordering Number	Repetitive Peak Voltages VDRM and VRRM (V)	Conditions
DCR3650Y28 DCR3650Y26 DCR3650Y24	2800 2600 2400	$T_{Vj} = -40 ^{\circ} C \text{ to } 125 ^{\circ} C,$ $IDRM = IRRM = 200 mA,$ $VDRM, VRRM t_{P} = 10 ms$ $VDSM \& VRSM =$ $VDRM \& VRRM + 100 V$ $respectively$

Lower voltage grades available.

### **ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

### DCR3650Y28

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

### **KEY PARAMETERS**

$\mathbf{V}_{DRM}$	2800V
IT(AV)	3620A
Ітѕм	50200A
dV/dt*	1500V/µs
dl/dt	300A/μs

<sup>\*</sup> Higher dV/dt selections are available on request

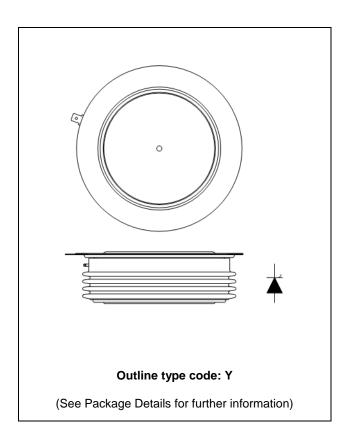


Fig. 1 Package outline

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## **CURRENT RATINGS**

## T<sub>case</sub> = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
İT(AV)	Mean on-state current	Half wave resistive load	3620	А
It(RMS)	RMS value	S value -		А
lτ	Continuous (direct) on-state current	-	5070	Α

## **SURGE RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
Ітѕм	Surge (non-repetitive) on-state current	10ms half sine, T <sub>case</sub> = 125°C	50.2	kA
l²t	I2t for fusing	V <sub>R</sub> = 0	12.6	MA <sup>2</sup> s

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
		Double side cooled	DC	-	8.4	°C/kW
Rth(j-c)	Thermal resistance - junction to case	Cinale side socied	Anode DC	-	13.4	°C/kW
		Single side cooled	Cathode DC	-	23.1	°C/kW
D	Thermal resistance - case to heatsink	Clamping force 54kN	Double side	-	2.0	°C/kW
Rth(c-h)		(with mounting compound)	Single side	-	4.0	°C/kW
Tvj	Virtual junction temperature	Blocking Vdrm / Vrrm		-	125	°C
Tstg	Storage temperature range			-55	125	°C
Fm	Clamping force			48	59	kN

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# **DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Condition	ıs	Min.	Max.	Units
IRRM/IDRM	Peak reverse and off-state current	At VRRM/VDRM, Tcase = 125°C	;	-	200	mA
Vтм	Instantaneous forward voltage	At 4000A peak, Tj = 125°C		1.25	1.40	V
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V <sub>DRM</sub> , T <sub>j</sub> = 125°C, g	ate open	-	1500	V/µs
dl/dt	Rate of rise of on-state current	From 67% V <sub>DRM</sub> to 2x I <sub>T(AV)</sub> Gate source 30V, 10Ω	Repetitive 50Hz	-	150	A/µs
di/dt	ivate of fise of off-state current	tr < 0.5µs, Tj = 125°C	Non-repetitive	-	300	A/µs
Varan	Threshold voltage - Low level	500A to 2700A at Tcase = 125°C		-	0.81	٧
<b>V</b> т(то)	Threshold voltage - High level	2700A to 7000A at Tcase = 125°C		-	0.97	V
_	On-state slope resistance - low level	500A to 2700A at Tcase = 125°C		-	0.17	mΩ
ľτ	On-state slope resistance - High level	2700A to 7000A at Tcase = 1	2700A to 7000A at Tcase = 125°C		0.11	mΩ
tgd	Delay time	$V_D = 67\% \; V_{DRM}, \; gate \; source \; 30V, \; 10\Omega$ $t_T = 0.5 \mu s, \; T_J = 25 ^{\circ} C$		1	3	μs
tq	Turn-off time	T <sub>j</sub> = 125°C, V <sub>R</sub> = 200V, dI/dt = 1A/μs, dV <sub>DR</sub> /dt = 20V/μs linear		100	250	μs
Qs	Stored charge	I <sub>T</sub> = 2000A, T <sub>j</sub> = 125°C, dI/dt = 1A/μs V <sub>R(peak)</sub> ~ 1700V, V <sub>RM</sub> ~ 1100V		630	1810	μC
IRR	Reverse recovery current			21	34	А
lι	Latching current	Tj = 25°C, VD = 5V		-	3	Α
Ін	Holding current	Tj = 25°C, Rg-к = ∞, Iтм = 50	0A, Ιτ = 5A	-	300	mA

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### **GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
<b>V</b> GT	Gate trigger voltage	VDRM = 5V, Tcase = 25°C	1.5	V
<b>V</b> GD	Gate non-trigger voltage	At 50% VDRM, Tcase = 125°C	0.4	V
lgт	Gate trigger current VDRM = 5V, Tcase = 25°C		250	mA
Igp	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	15	mA

### **CURVES**

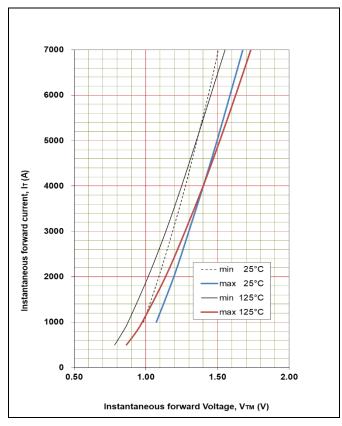


Fig. 2 Maximum & minimum on state characteristics

## **VTM EQUATION**

 $V_{TM} = A + B.ln(I_T) + C.I_T + D.\sqrt{I_T}$ 

Where A = 0.582097

B = 0.018183

C = 0.000063

D = 0.006577

These values are valid for  $T_j = 125^{\circ}C$  for  $I_{T}$  500A to 7000A

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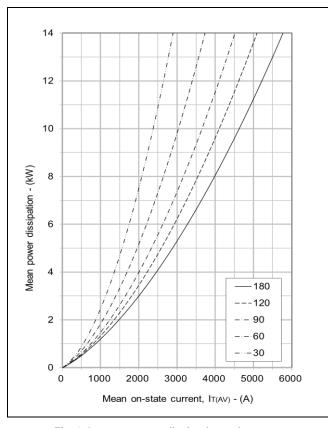


Fig. 3 On-state power dissipation - sine wave

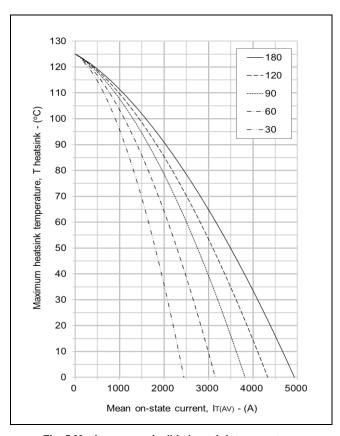


Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave

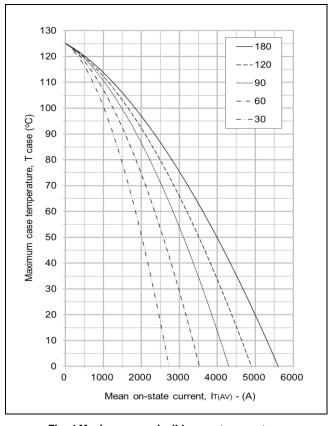


Fig. 4 Maximum permissible case temperature, double side cooled - sine wave

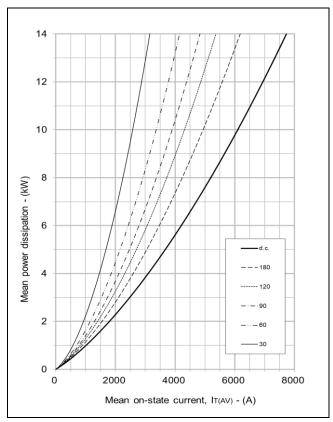


Fig. 6 On-state power dissipation - rectangular wave

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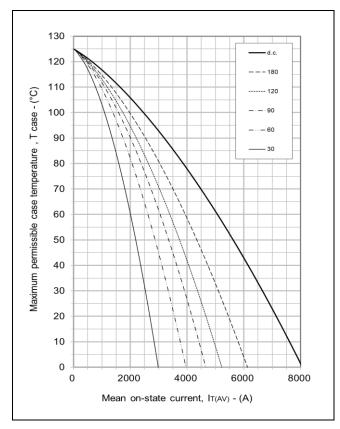
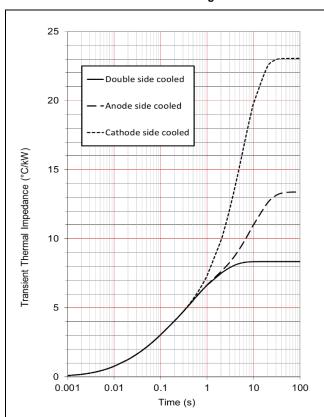


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave



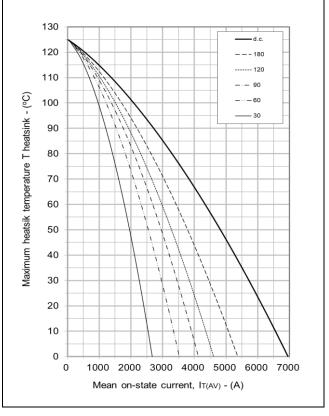


Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave

		1	2	3	4
Double side	Ri(°C/kW)	0.612	1.772	3.105	2.861
cooled	Ti(s)	0.010	0.056	0.333	1.632
Anode side	Ri(°C/kW)	0.701	1.939	3.610	7.138
cooled	Ti(s)	0.011	0.066	0.420	9.061
Cathode side	Ri(°C/kW)	0.673	2.017	1.731	18.639
cooled	Ti(s)	0.011	0.066	0.304	5.727

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

 $\Delta R_{\text{th(j-c)}}$  Conduction

Tables show the increments of thermal resistance  $R_{\text{th}(j\text{-c})}$  when the device operates at conduction angles other than d.c.

Double side cooling						
	$\Delta Z_{th}$	(Z)				
θ°	sine.	rect.				
180	0.94	0.65				
120	1.09	0.92				
90	1.24	1.07				
60	1.38	1.23				
30	1.49	1.40				
15	1.54	1 10				

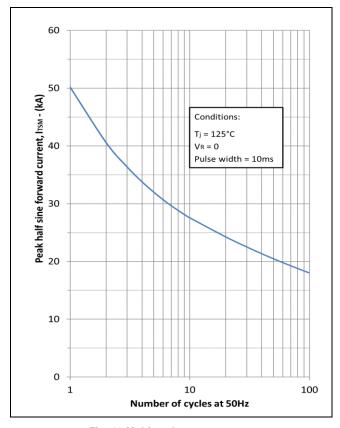
Ar	node Side Cooling						
	$\Delta Z_t$	ΔZ <sub>th</sub> (Z)					
θ°	sine.	rect.					
180	0.94	0.64					
120	1.08	0.91					
90	1.23	1.06					
60	1.37	1.22					
30	1.47	1.38					

Aı	Anode Side Cooling			Cathode Sided Cooling			
	$\Delta Z_{th}$ (Z)				$\Delta Z_t$	h (Z)	
θ°	sine.	rect.		θ°	sine.	rect.	
180	0.94	0.64		180	0.94	0.64	
120	1.08	0.91		120	1.08	0.91	
90	1.23	1.06		90	1.24	1.06	
60	1.37	1.22		60	1.37	1.22	
30	1.47	1.38		30	1.48	1.39	
15	1.52	1.47		15	1.53	1.48	

Fig. 9 Maximum (limit) transient thermal impedance - junction to case (degC/kW)

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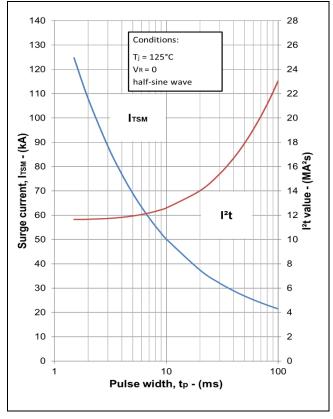


Fig. 10 Multi-cycle surge current

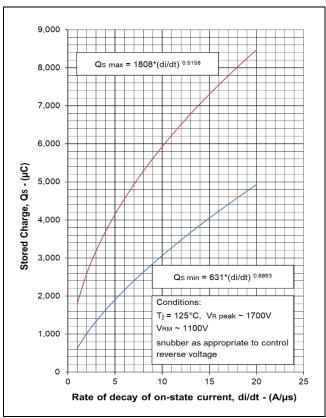


Fig. 12 Stored charge

Fig. 11 Single-cycle surge current

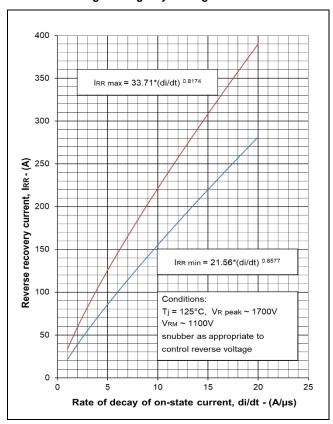


Fig. 13 Reverse recovery current

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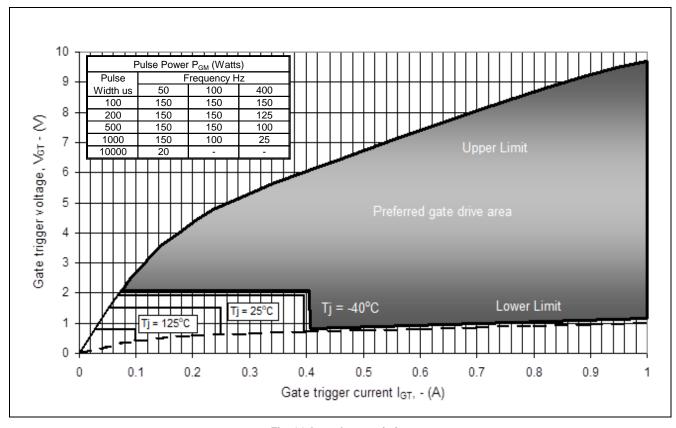


Fig. 14 Gate characteristics

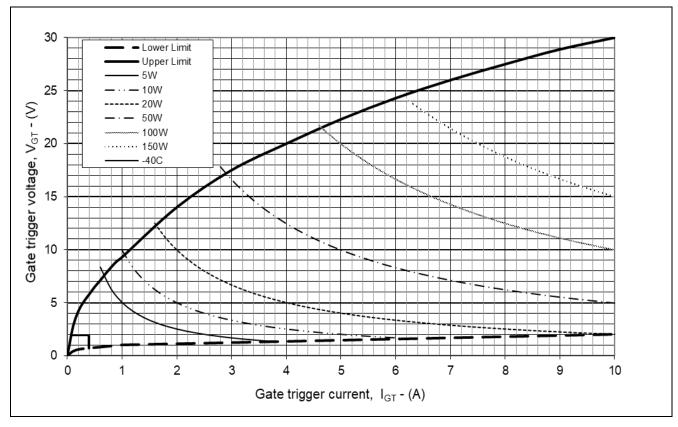


Fig. 15 Gate characteristics

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### **PACKAGE DETAILS**

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

### DO NOT SCALE

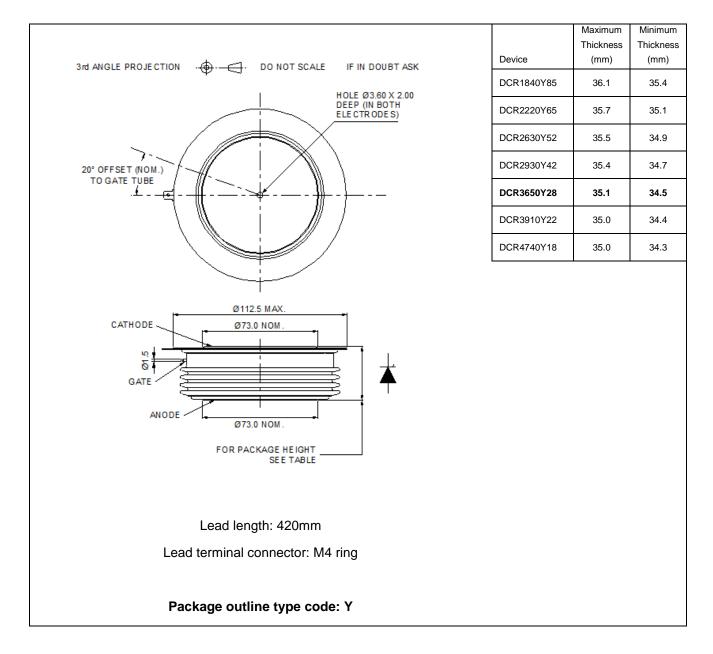


Fig. 16 Package outline

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